INA828 50µV 偏移、7nV/√Hz 噪声低功耗精密仪表放大器

1 特性

- 精密仪表放大器演变：
  - 第二代：INA828
  - 第一代：INA128
- 低失调电压：最大值为 50µV
- 增益漂移：5ppm/°C (G = 1)，50ppm/°C (G > 1)
- 噪声：7nV/√Hz
- 带宽：2MHz (G = 1)、260kHz (G = 100)
- 与 1nF 电容负载一起工作时保持稳定
- 输入保护电压高达 ±40V
- 共模抑制：
  - 最小值为 110dB (G = 10)
- 电源抑制：最小值为 100dB (G = 1)
- 电源电流：最大值为 650 µA
- 电源范围：
  - 单电源：4.5V 至 36V
  - 双电源：±2.25V 至 ±18V
- 额定温度范围：
  –40°C 至 +125°C
- 封装：8 引脚 SOIC

2 应用

- 工业过程控制
- 断路器
- 电池检测仪
- 心电图 (ECG) 放大器
- 电力自动化
- 医疗仪表
- 便携式仪表

3 说明

INA828 是一款高精度仪表放大器，此放大器提供低功耗并且可在极宽的单电源或双电源范围内工作。可通过单个外部电阻器在 1 到 1000 范围内设置增益。由于采用新的超 β 输入晶体管（这些晶体管可提供极低的输入失调电压、失调电压漂移、输入偏置电流以及输入电压和电流噪声），该器件可提供出色的精度。附加电路可以为输入提供高达 ±40V 的过压保护。

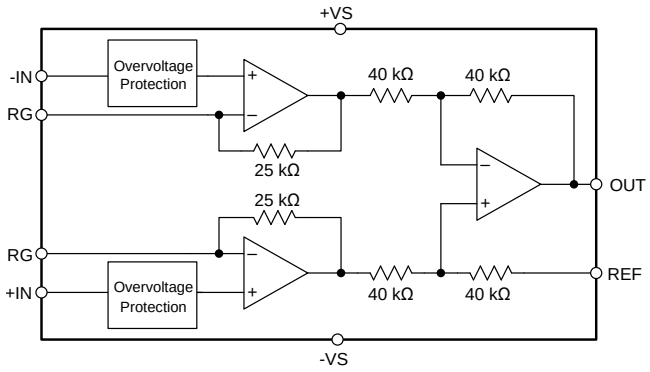
INA828 经过优化，可提供出色的共模抑制比。当 G = 1 时，整个输入共模范围内共模抑制比超过 90dB。该器件非常适用于通过 5V 单电源和高达 ±18V 的双电源供电的低电压运行。最后，INA828 采用 8 引脚 SOIC 封装，额定温度范围为 –40°C 至 +125°C。

Device Information(1)

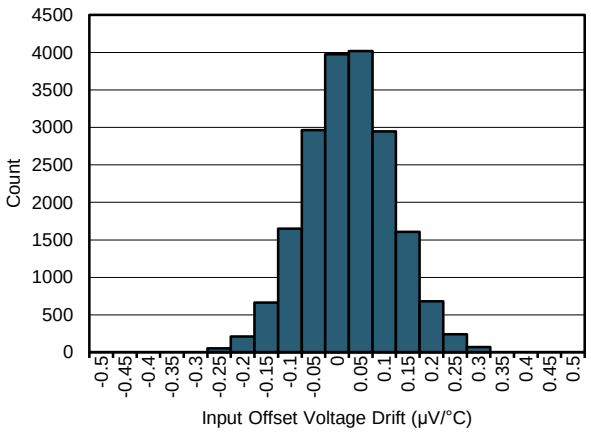
PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA828	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

INA828 简化内部原理图



输入失调电压漂移的典型分布



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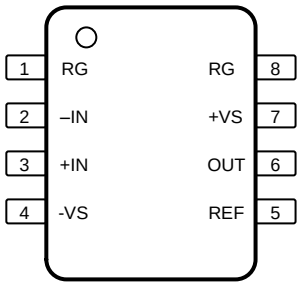
4 修订历史记录

Changes from Original (August 2017) to Revision A **Page**

- Changed MAX value for G = 1 in "GE" row from "±0.020%" to "±0.025%" ... 5

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
RG	1	—	Gain setting pin. Place a gain resistor between pin 1 and pin 8.
	8		
–IN	2	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
–VS	4	—	Negative supply
REF	5	I	Reference input. This pin must be driven by a low impedance source.
OUT	6	O	Output
+VS	7	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–18	18	V
Signal input pins	Voltage	–40	40	V
	REF pin	–18	18	
Output short-circuit(2)		Continuous		
Temperature	Operating, T_A	–50	150	°C
	Junction, T_J		175	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	Single supply	4.5	36	V
	Dual supply	±2.25	±18	
Specified temperature		–40	125	°C
Operating temperature		–50	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA828 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input stage offset voltage(1)(2)	G = 100, RTI		20	50	µV
		T_A = –40°C to +125°C(3)			90	µV
		vs temperature, T_A = –40°C to +125°C			0.5	µV/°C
V_{OSO}	Output stage offset voltage(1)(2)	G = 1, RTI		50	250	µV
		T_A = –40°C to +125°C(3)			500	µV
		vs temperature, T_A = –40°C to +125°C			5	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI	110	120		dB
		G = 10, RTI	114	130		
		G = 100, RTI	130	135		
		G = 1000, RTI	136	140		
z_{id}	Differential impedance			100 || 1		GΩ || pF
z_{ic}	Common-mode impedance			100 || 10		GΩ || pF
	RFI filter, –3-dB frequency			53		MHz
V_{CM}	Operating input range(4)		(V–) + 2		(V+) – 2	V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C	See Figure 48 to Figure 51			
	Input overvoltage range	T_A = –40°C to +125°C			±40	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1	90	100		dB
		At dc to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 10	110	120		
		At dc to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 100	130	140		
		At dc to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1000	140	145		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		0.15	0.6	nA
		T_A = –40°C to +125°C			2	
I_{OS}	Input offset current	V_{CM} = V_S / 2		0.15	0.6	nA
		T_A = –40°C to +125°C			2	
NOISE VOLTAGE						
e_{NI}	Input stage voltage noise(5)	f = 1 kHz, G = 100, R_S = 0 Ω		7		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		0.14		$µV_{PP}$
e_{NO}	Output stage voltage noise(5)	f = 1 kHz, R_S = 0 Ω		90		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		7.7		$µV_{PP}$
I_n	Noise current	f = 1 kHz		170		fA/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100		4.7		pA_{PP}
GAIN						
G	Gain equation			1 + (50 kΩ / R_G)		V/V
	Range of gain		1		1000	V/V
GE	Gain error	G = 1, V_O = ±10 V		±0.005%	±0.025%	
		G = 10, V_O = ±10 V		±0.025%	±0.15%	
		G = 100, V_O = ±10 V		±0.025%	±0.15%	
		G = 1000, V_O = ±10 V		±0.05%		
	Gain vs temperature(6)	G = 1, T_A = –40°C to +125°C			±5	ppm/°C
		G > 1, T_A = –40°C to +125°C			±50	

(1) Total offset, referred-to-input (RTI): V_{OS} = (V_{OSI}) + (V_{OSO} / G).
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Specified by characterization.
(4) Input voltage range of the INA828 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves 图 48 through 图 51 for more information.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$
(6) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.

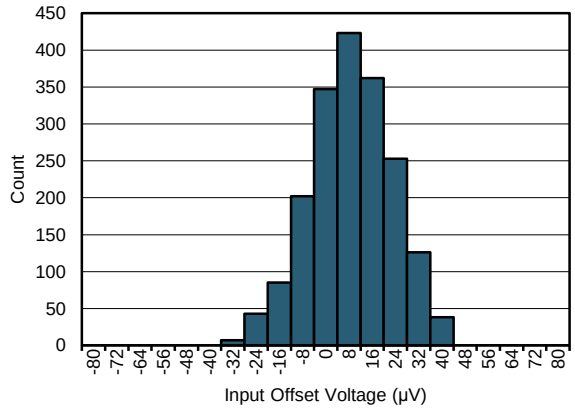
Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain nonlinearity	G = 1 to 10, V_O = –10 V to +10 V, R_L = 10 kΩ		1	10	ppm
		G = 100, V_O = –10 V to +10 V, R_L = 10 kΩ			15	
		G = 1000, V_O = –10 V to +10 V, R_L = 10 kΩ			20	
		G = 1 to 100, V_O = –10 V to +10 V, R_L = 2 kΩ		30		
OUTPUT						
	Voltage swing		(V–) + 0.15		(V+) – 0.15	V
	Load capacitance stability			1000		pF
Z_O	Closed-loop output impedance	f = 10 kHz		1.3		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±18		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		2.0		MHz
		G = 10		640		kHz
		G = 100		260		
		G = 1000		33		
SR	Slew rate	G = 1, V_O = ±10 V		1.2		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 10 V		12		µs
		0.01%, G = 1000, V_{STEP} = 10 V		40		
		0.001%, G = 1 to 100, V_{STEP} = 10 V		16		
		0.001%, G = 1000, V_{STEP} = 10 V		50		
REFERENCE INPUT						
R_{IN}	Input impedance			40		kΩ
	Voltage range		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
V_S	Power-supply voltage	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
I_Q	Quiescent current	V_{IN} = 0 V		600	650	µA
		vs temperature, T_A = –40°C to +125°C			850	

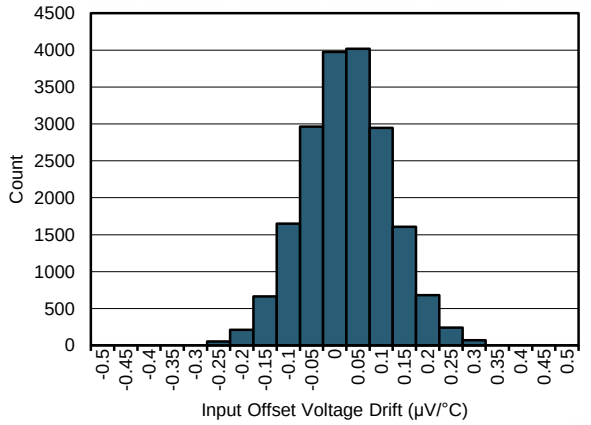
6.6 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



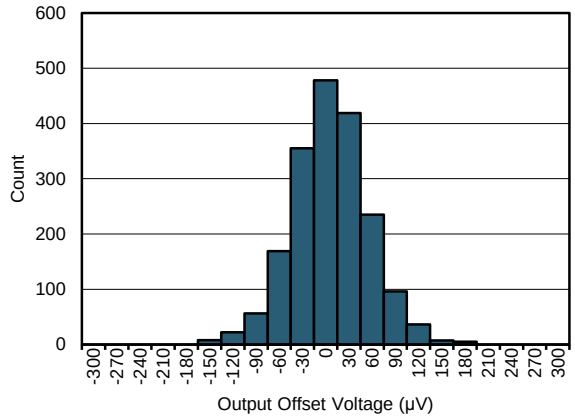
N = 1886 Mean = 4.73 µV
Std. Dev. = 13.98 µV

图 1. Typical Distribution of Input Offset Voltage



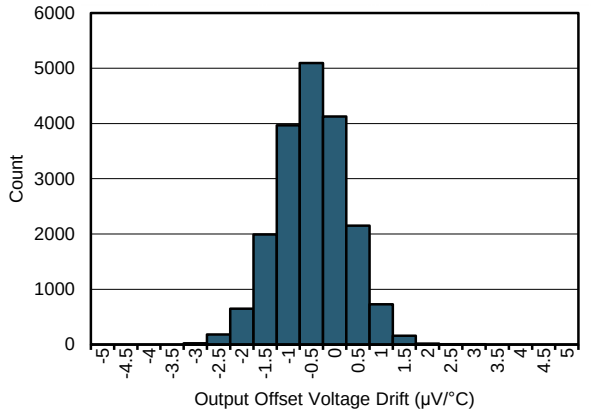
N = 19081 Mean = 0.16 nV/°C
Std. Dev. = 0.09 µV/°C

图 2. Typical Distribution of Input Offset Voltage Drift



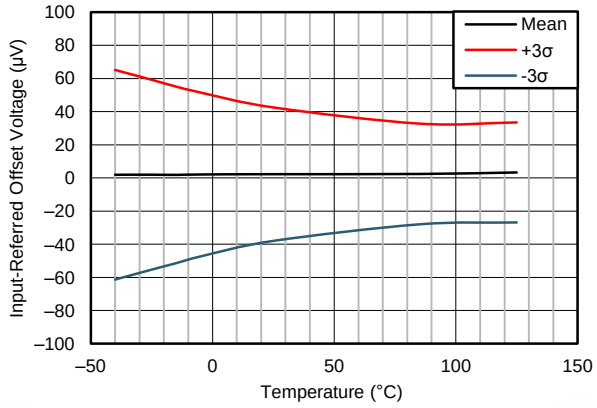
N = 1886 Mean = –8.71 µV
Std. Dev. = 48.57 µV

图 3. Typical Distribution of Output Offset Voltage



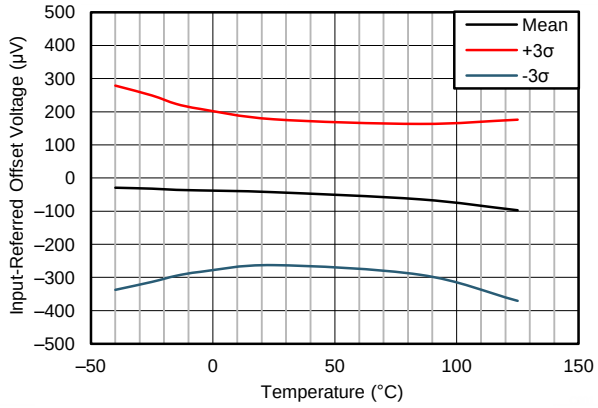
N = 19081 Mean = –0.73 µV/°C
Std. Dev. = 0.74 µV/°C

图 4. Typical Distribution of Output Offset Voltage Drift



G = 100
88 units, 3 wafer lots

图 5. Input-Referred Offset Voltage vs Temperature

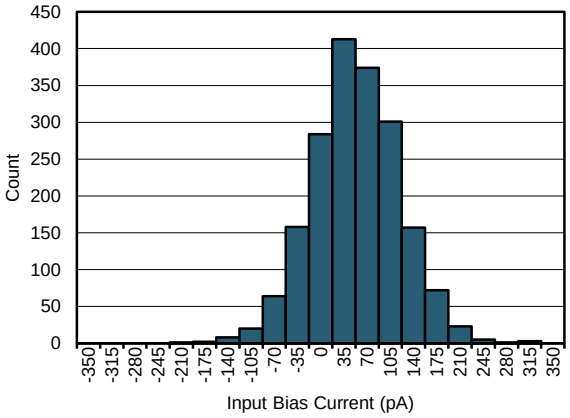


G = 1
88 units, 3 wafer lots

图 6. Input-Referred Offset Voltage vs Temperature

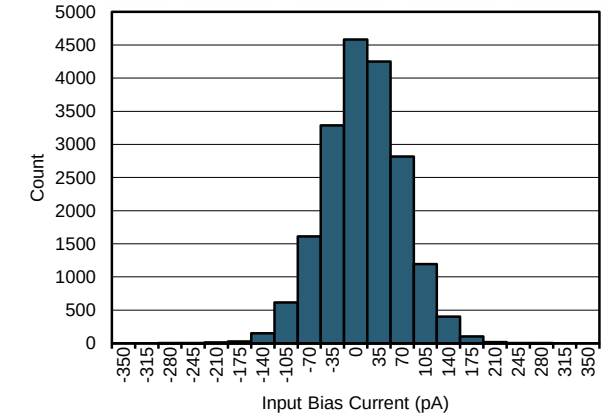
Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



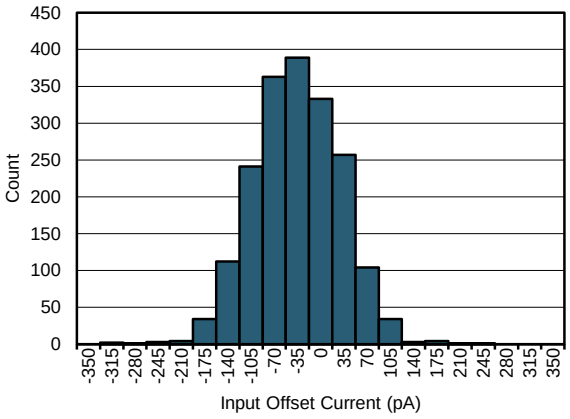
N = 1886 Mean = 36.25 pA
Std. Dev. = 65.31 pA

图 7. Typical Distribution of Input Bias Current (25°C)



N = 19081 Mean = –5.32 pA
Std. Dev. = 57.46 pA

图 8. Typical Distribution of Input Bias Current (90°C)



N = 1886 Mean = –52.64 pA
Std. Dev. = 63.86 pA

图 9. Typical Distribution of Input Offset Current

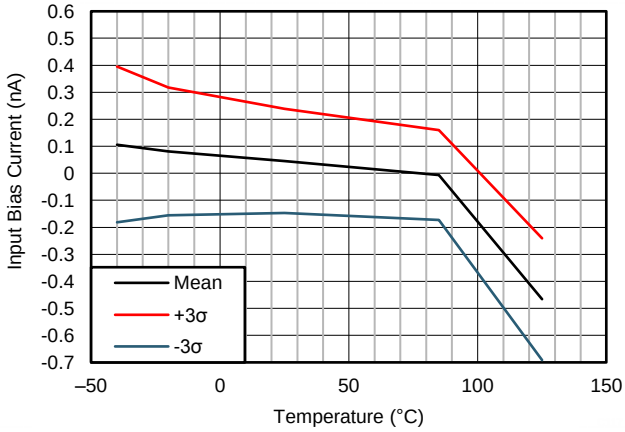


图 10. Input Bias Current vs Temperature

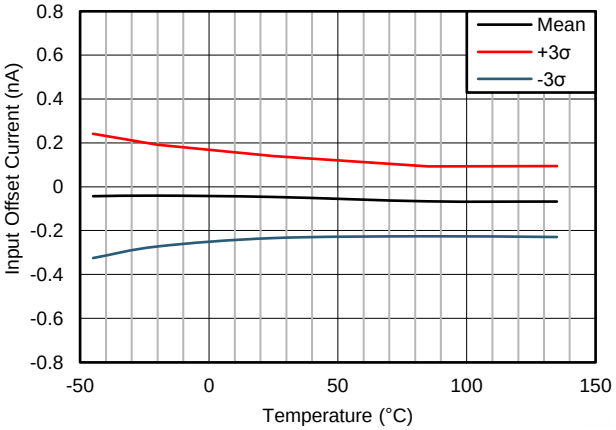
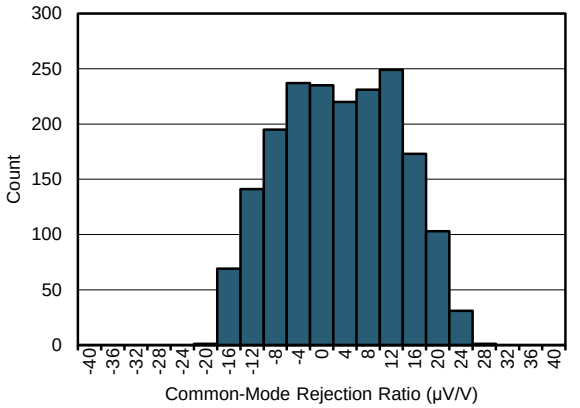


图 11. Input Offset Current vs Temperature



N = 1886 Mean = 1.18 µV/V
Std. Dev. = 10.04 µV/V

图 12. Typical CMRR Distribution (G = 1)

Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

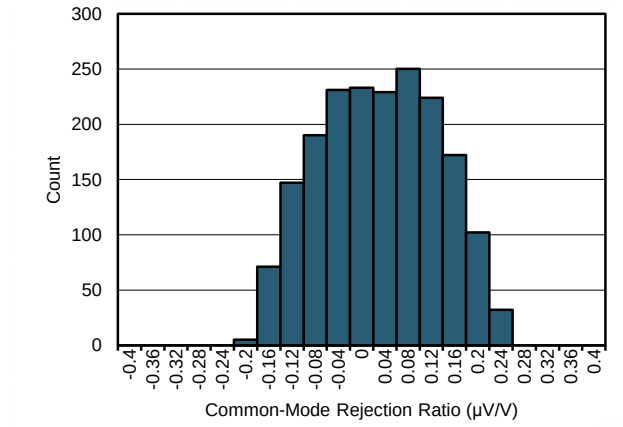


图 13. Typical CMRR Distribution (G = 100)

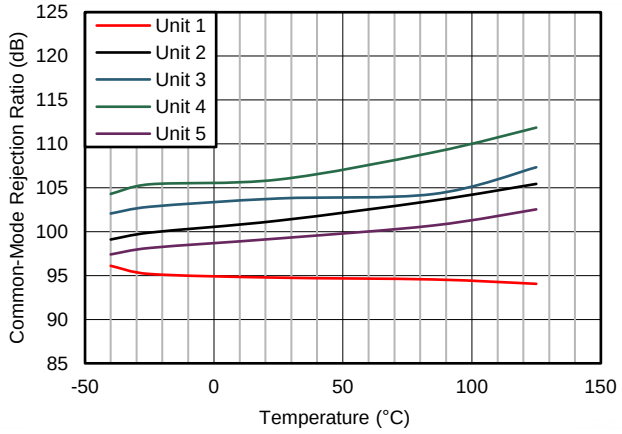


图 14. CMRR vs Temperature (G = 1)

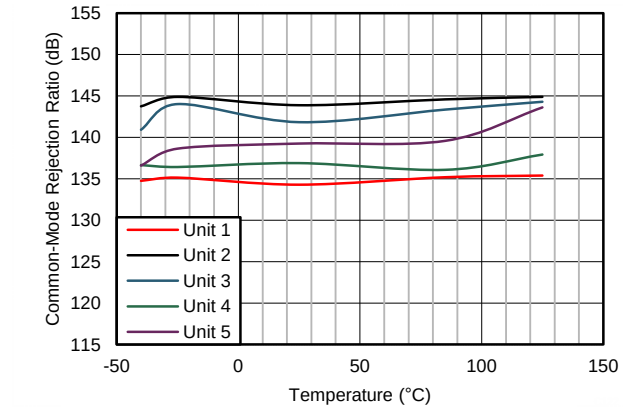


图 15. CMRR vs Temperature (G = 100)

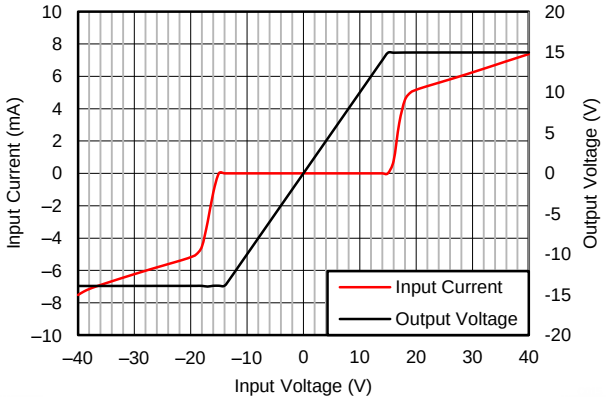


图 16. Input Current vs Input Overvoltage

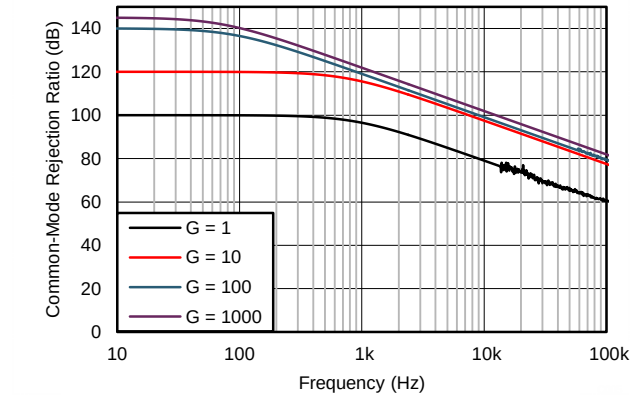


图 17. CMRR vs Frequency (RTI)

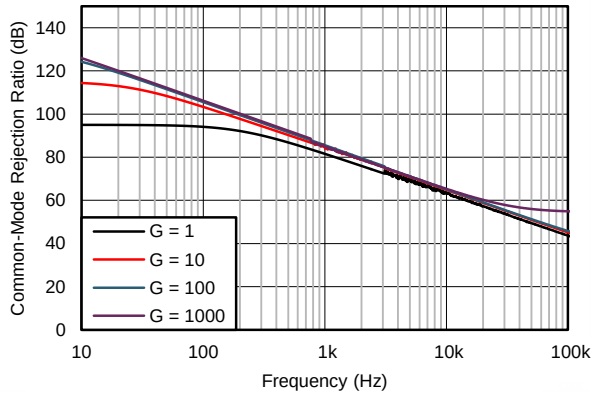


图 18. CMRR vs Frequency (RTI, 1-kΩ Source Imbalance)

Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

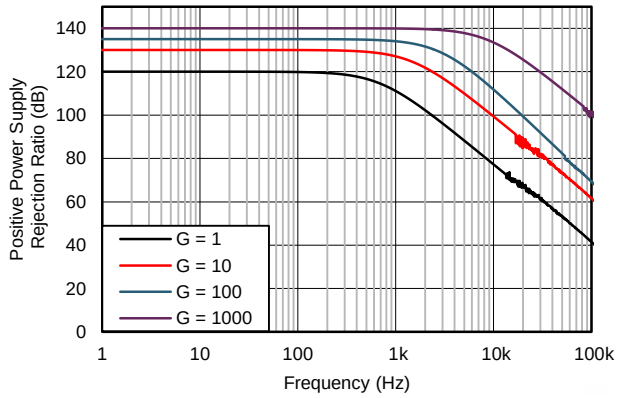


图 19. Positive PSRR vs Frequency (RTI)

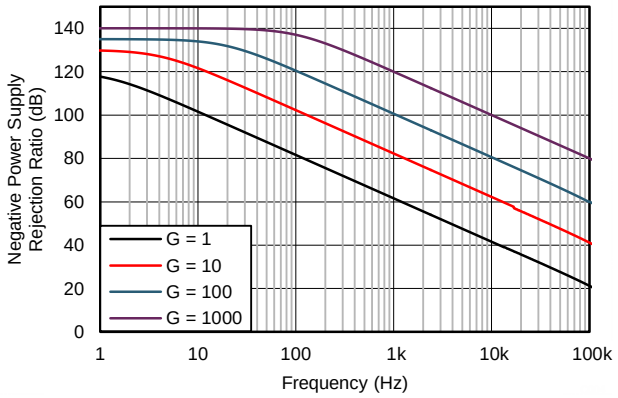


图 20. Negative PSRR vs Frequency (RTI)

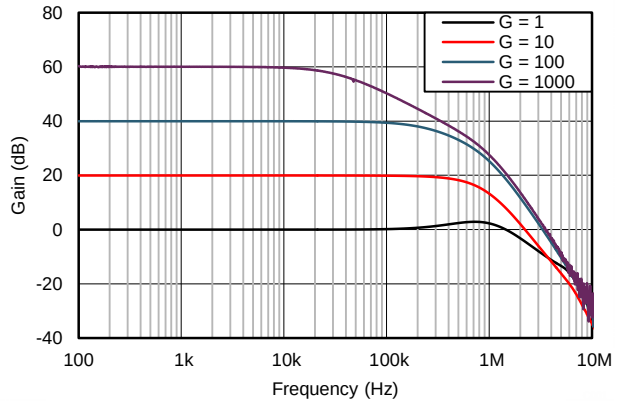


图 21. Gain vs Frequency

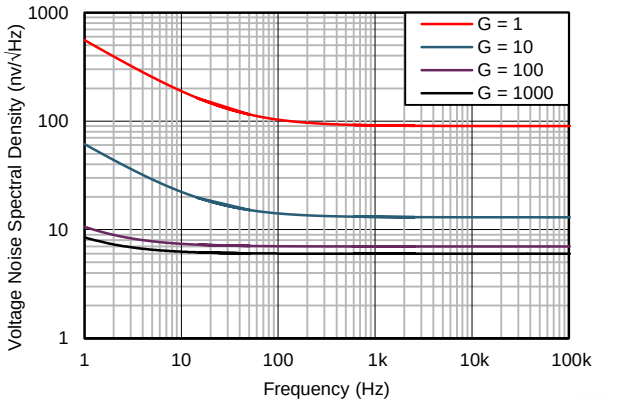


图 22. Voltage Noise Spectral Density vs Frequency (RTI)

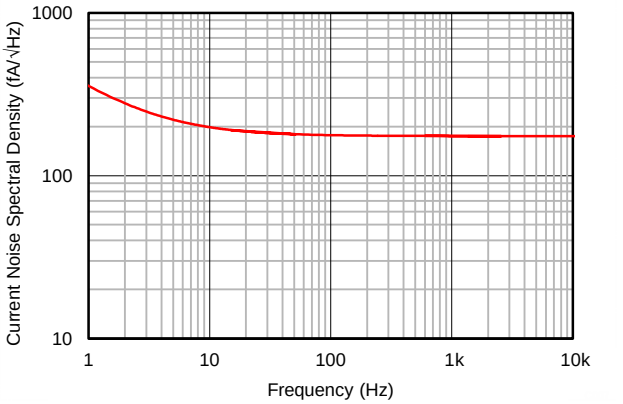


图 23. Current Noise Spectral Density vs Frequency (RTI)

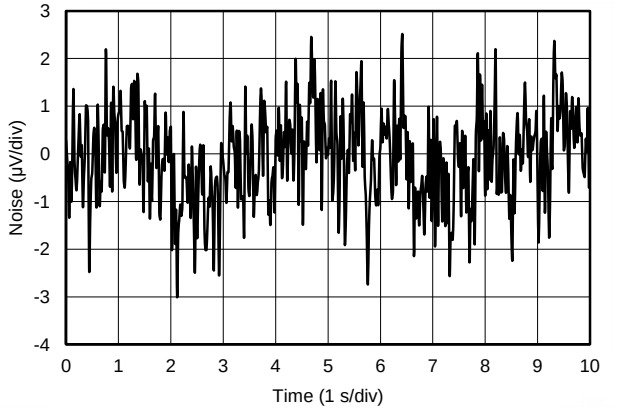


图 24. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1)

Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

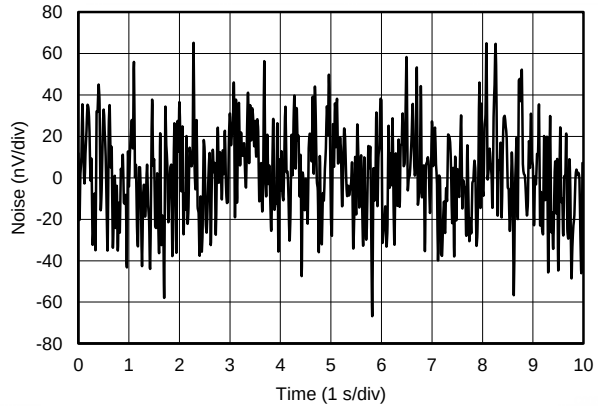


图 25. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1000)

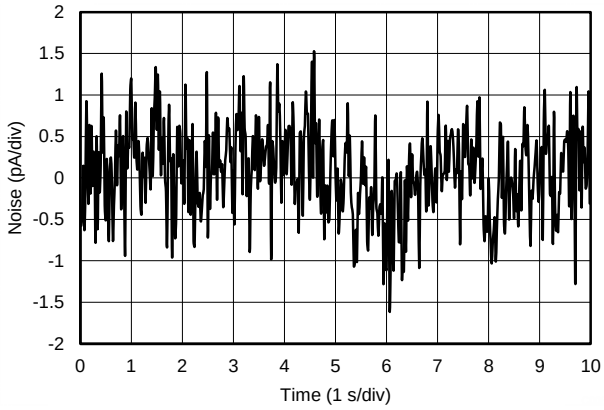
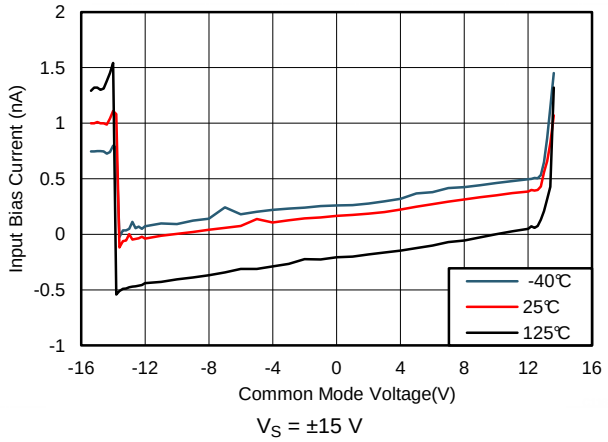


图 26. 0.1-Hz to 10-Hz RTI Current Noise



V_S = ±15 V

图 27. Input Bias Current vs Common-Mode Voltage

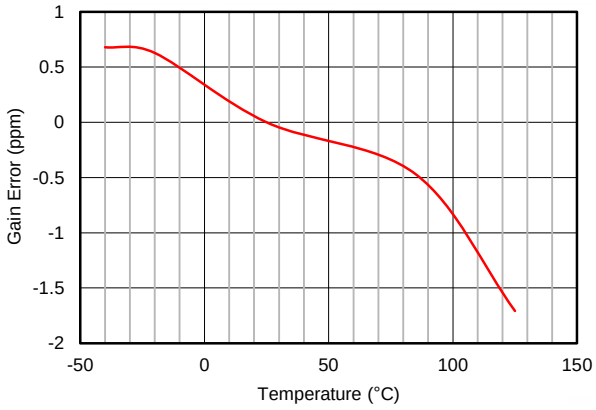


图 28. Gain Error vs Temperature (G = 1)

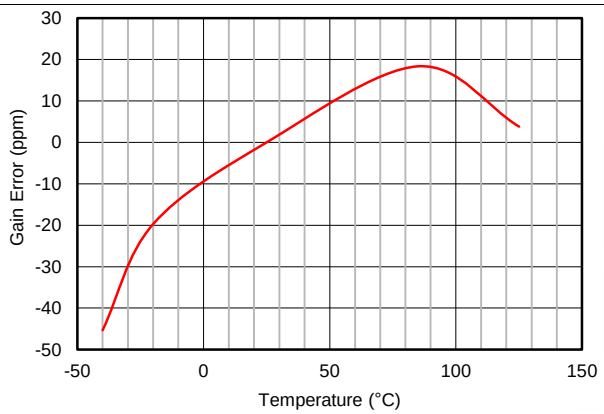


图 29. Gain Error vs Temperature (G = 100)

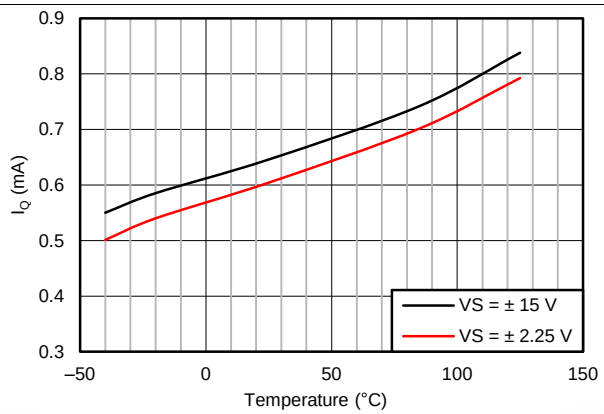


图 30. Supply Current vs Temperature

Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

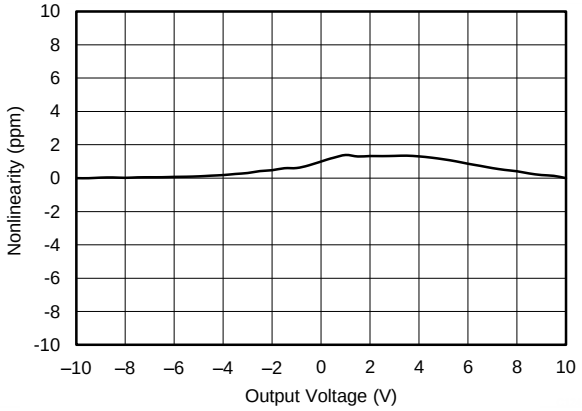


图 31. Gain Nonlinearity (G = 1)

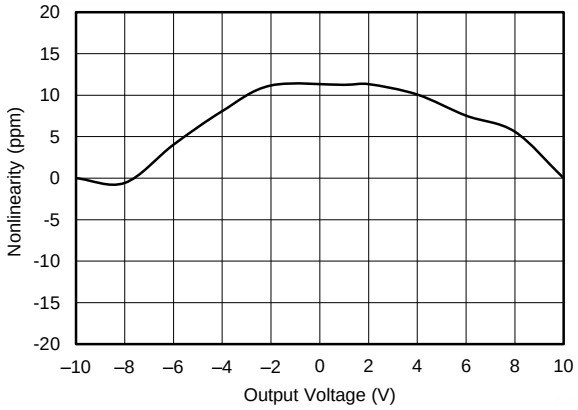


图 32. Gain Nonlinearity (G = 100)

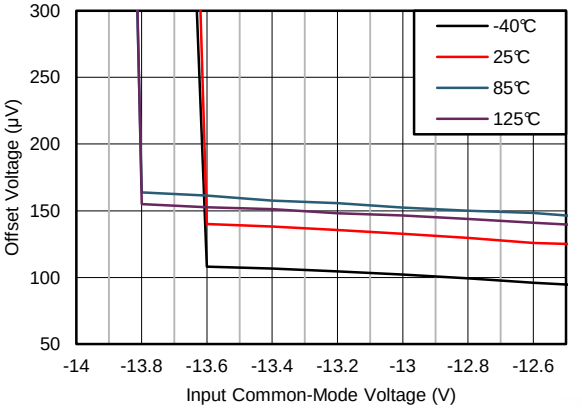


图 33. Offset Voltage vs Negative Common-Mode Voltage

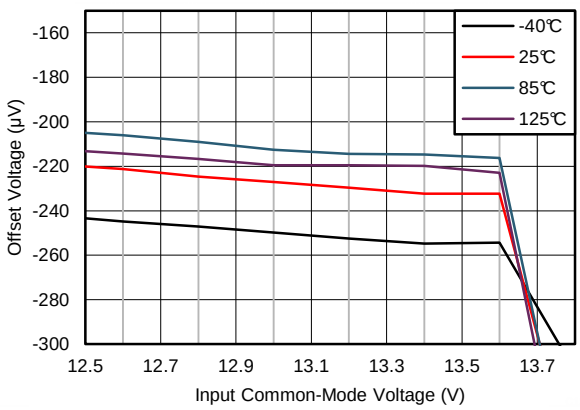


图 34. Offset Voltage vs Positive Common-Mode Voltage

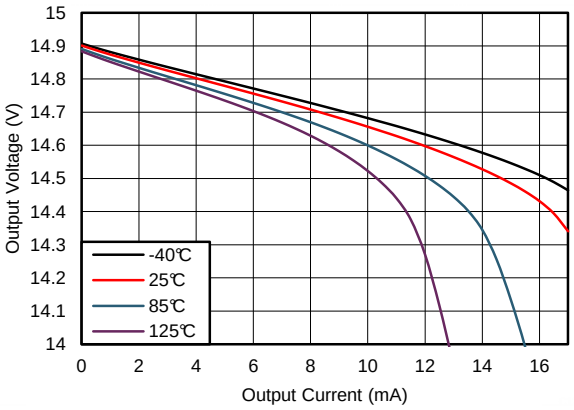


图 35. Positive Output Voltage Swing vs Output Current

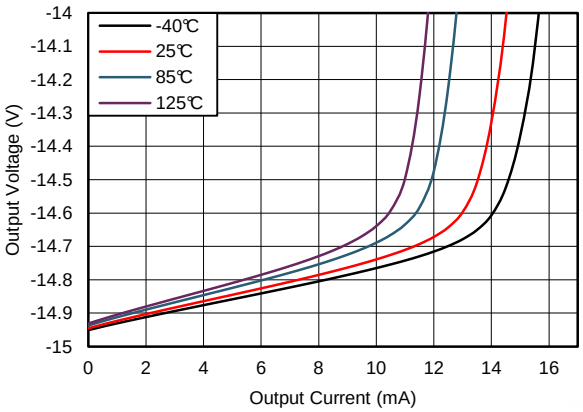


图 36. Negative Output Voltage Swing vs Output Current

Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

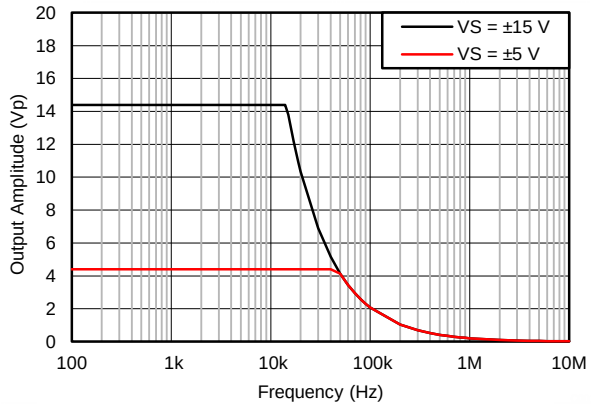
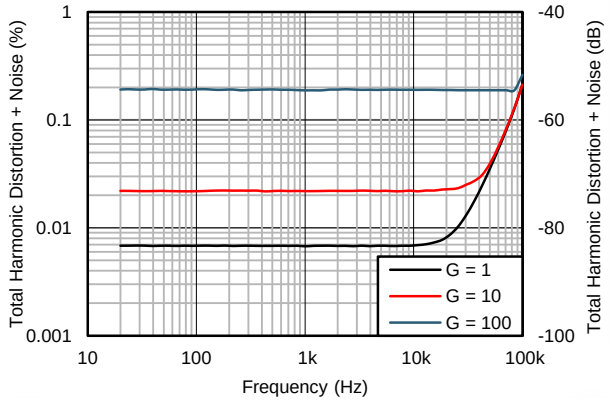


图 37. Large-Signal Frequency Response



500-kHz Measurement bandwidth
100-kΩ Load
1-V_{RMS} Output voltage

图 38. THD+N vs Frequency

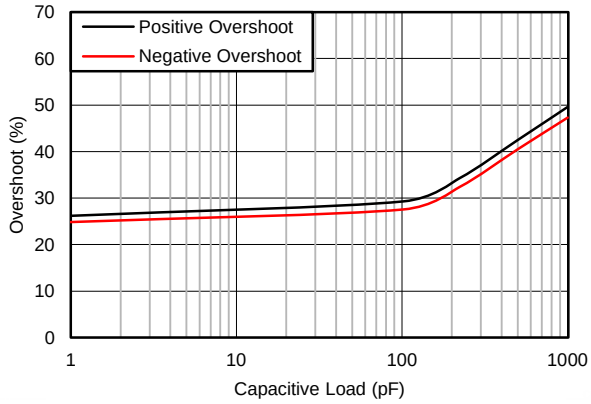
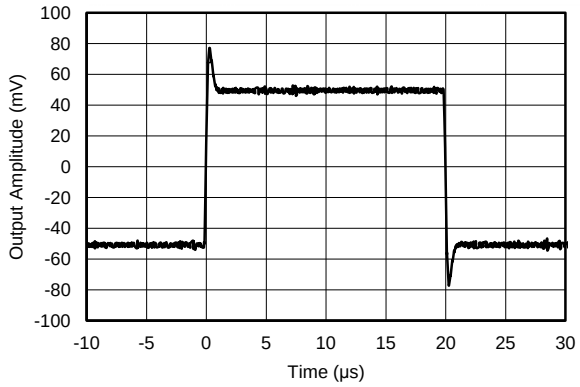
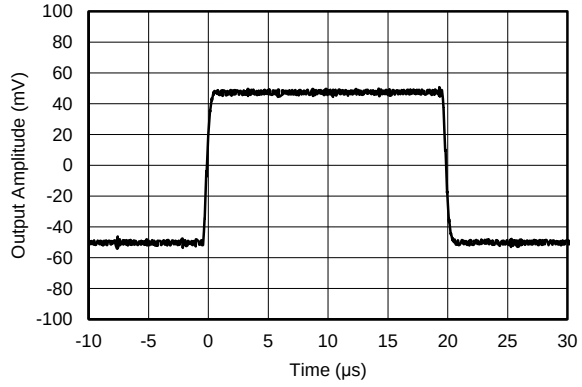


图 39. Overshoot vs Capacitive Loads



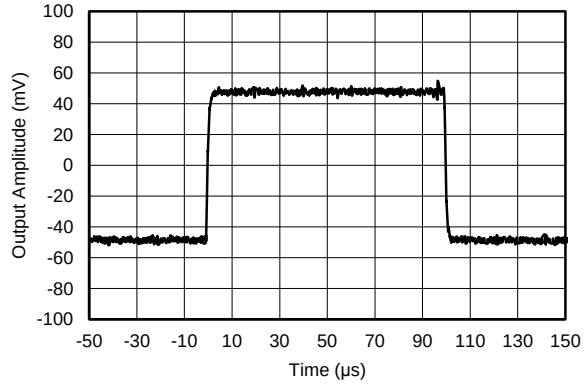
G = 1, R_L = 10 kΩ, C_L = 100 pF

图 40. Small-Signal Response



G = 10, R_L = 10 kΩ, C_L = 100 pF

图 41. Small-Signal Response

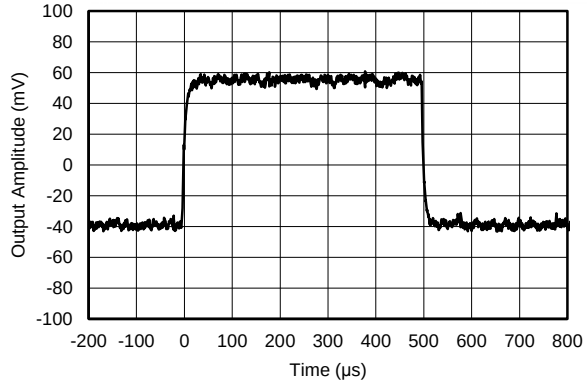


G = 100, R_L = 10 kΩ, C_L = 100 pF

图 42. Small-Signal Response

Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 1000, R_L = 10 kΩ, C_L = 100 pF

图 43. Small-Signal Response

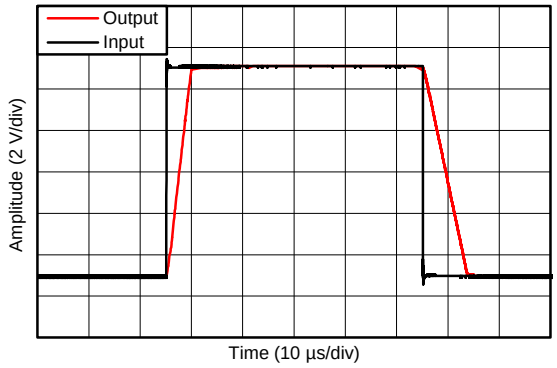


图 44. Large Signal Step Response

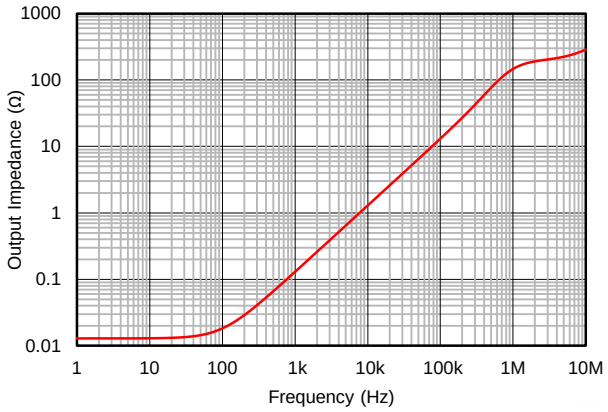


图 45. Closed-Loop Output Impedance

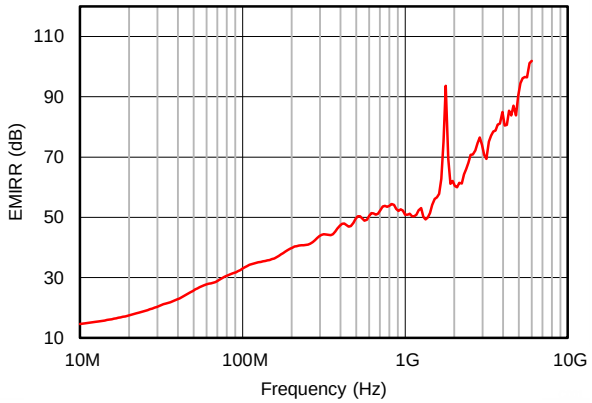


图 46. Differential-Mode EMI Rejection Ratio

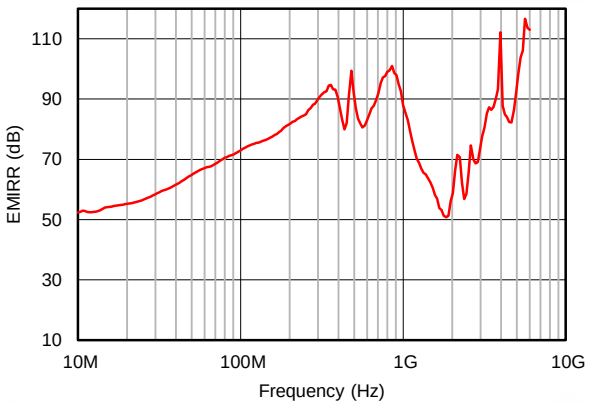
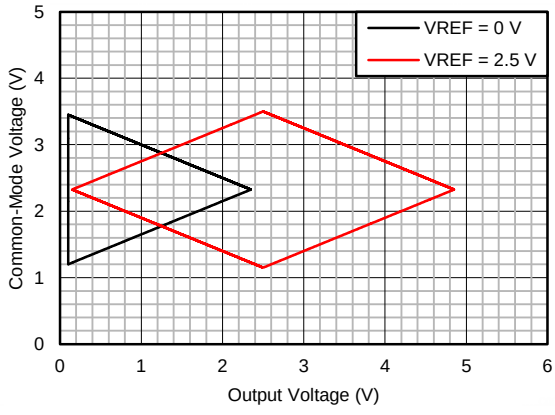


图 47. Common-Mode EMI Rejection Ratio

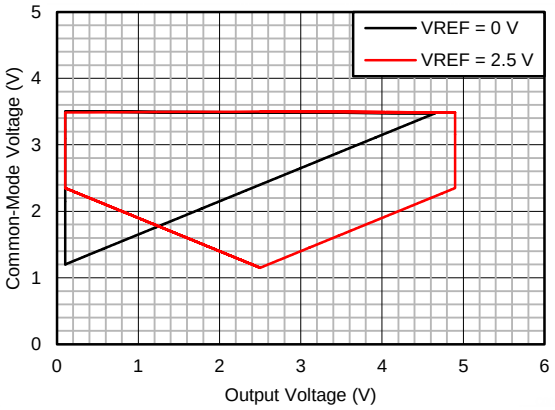


V_S = 5 V, G = 1

图 48. Input Common-Mode Voltage vs Output Voltage

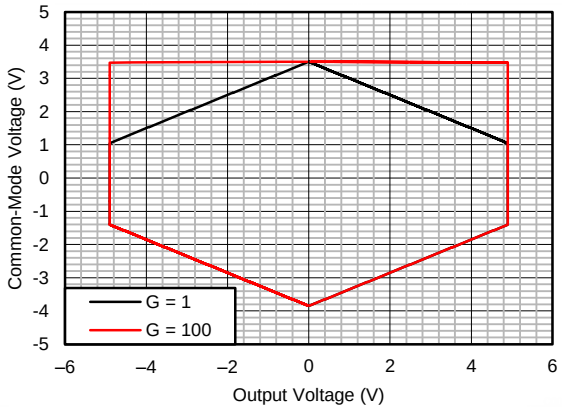
Typical Characteristics (接下页)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



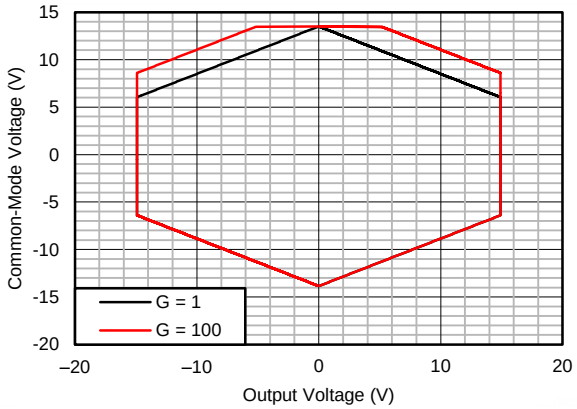
V_S = 5 V, G = 100

图 49. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V, V_{REF} = 0 V

图 50. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V, V_{REF} = 0 V

图 51. Input Common-Mode Voltage vs Output Voltage

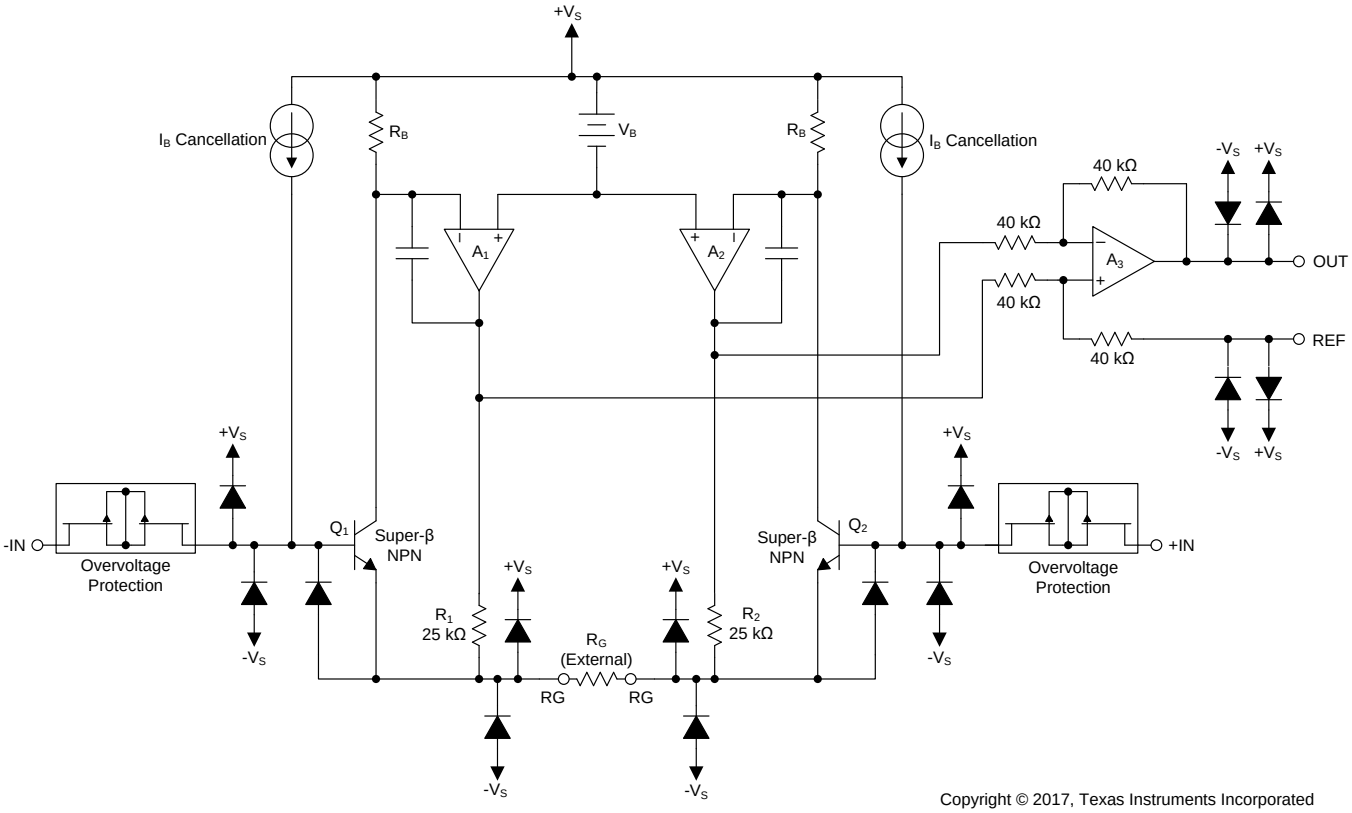
7 Detailed Description

7.1 Overview

The INA828 is a monolithic precision instrumentation amplifier incorporating a current-feedback input stage and a 4-resistor difference amplifier output stage. The differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF terminal. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Setting the Gain

图 52 shows that the gain of the INA828 is set by a single external resistor, R_G, connected between the RG pins (pins 1 and 8).

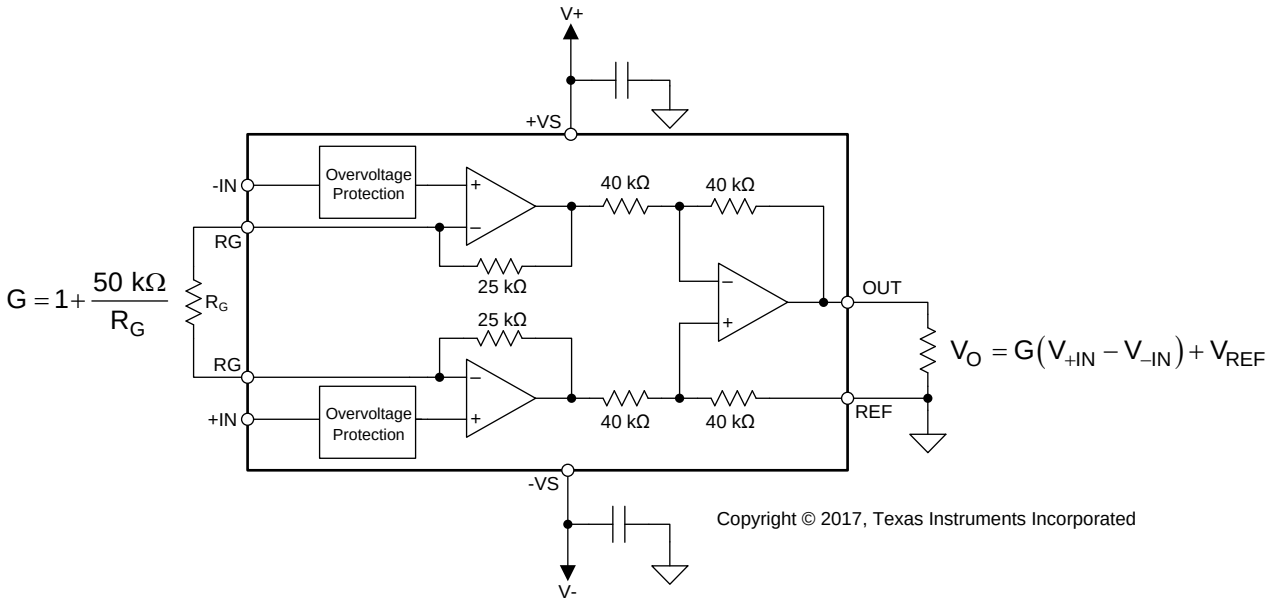


图 52. Simplified Diagram of the INA828 With Gain and Output Equations

The value of R_G is selected according to:

$$G = 1 + \frac{50\ k\Omega}{R_G} \quad (1)$$

表 1 lists several commonly-used gains and resistor values. The 50-kΩ term in 公式 1 comes from the sum of the two internal 25-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA828.

表 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50 k	49.9 k
5	12.5 k	12.4 k
10	5.556 k	5.49 k
20	2.632 k	2.61 k
50	1.02 k	1.02 k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9

7.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be determined from 公式 1.

The best gain drift of 5 ppm/℃ (maximum) can be achieved when the INA828 uses G = 1 without R_G connected. In this case, gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 40-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor R_G. The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To assure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see *Typical Characteristics,* 图 17.

7.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA828 to reject EMI. The offset resulting from an input EMI signal can be calculated using 公式 2:

$$\Delta V_{OS} = \left(\frac{V_{RF\_PEAK}^2}{100\ mV_P} \right) \cdot 10^{-\left(\frac{EMIRR\ (dB)}{20} \right)} \quad (2)$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal.

图 53 and 图 54 show the INA828 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. 表 2 shows the EMIRR values for the INA828 at frequencies commonly encountered in real-world applications. Applications listed in 表 2 can be centered on or operated near the particular frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing.

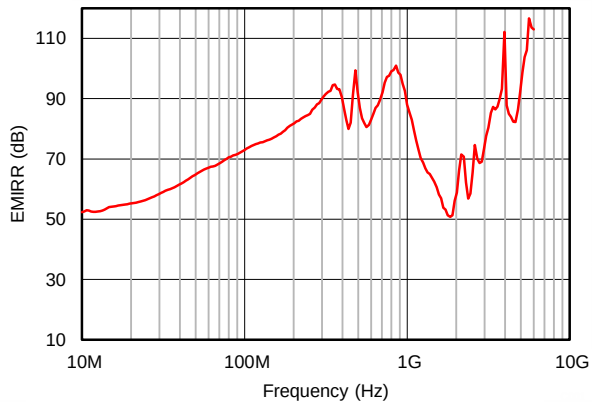


图 53. Common-Mode EMIRR Testing

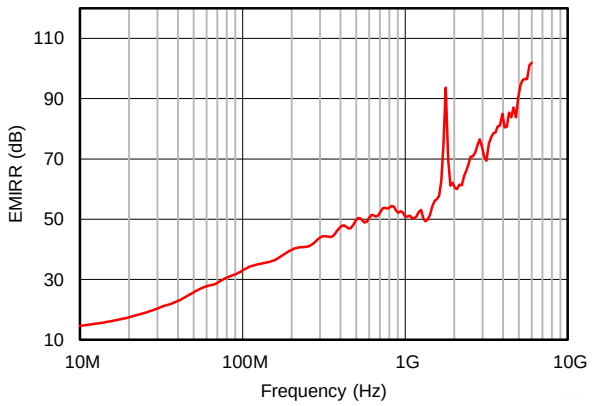


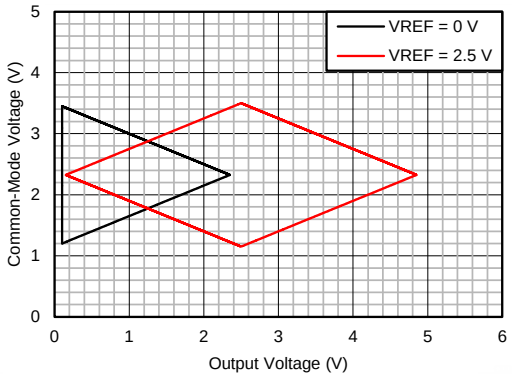
图 54. Differential Mode EMIRR Testing

表 2. INA828 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	48 dB	87 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52 dB	98 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	94 dB	51 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	66 dB	57 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	79 dB	87 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	90 dB	92 dB

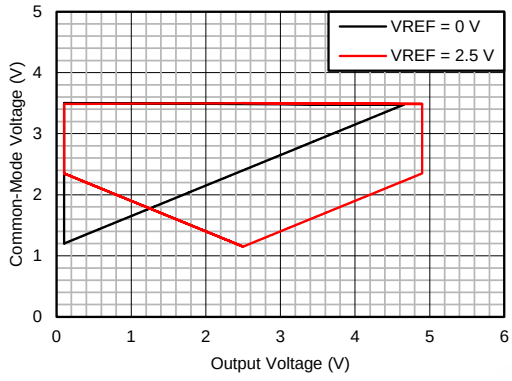
7.3.3 Input Common-Mode Range

The linear input voltage range of the INA828 input circuitry extends within 2 Volts of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in 图 55, 图 50, and 图 51. The common-mode range for other operating conditions is best calculated using the *INA common-mode range calculating tool*. The INA828 device can operate over a wide range of power supplies and VREF configurations, thus providing a comprehensive guide to common-mode range limits for all possible conditions is impractical.



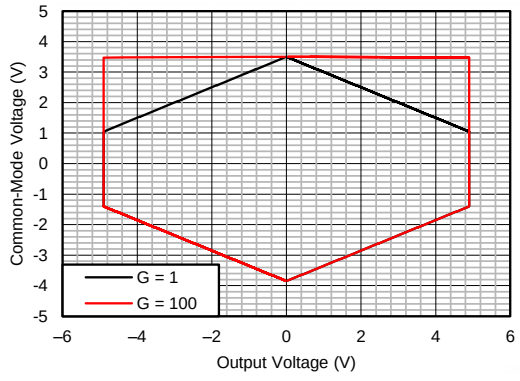
V_S = 5 V, G = 1

图 55. Input Common-Mode Voltage vs Output Voltage



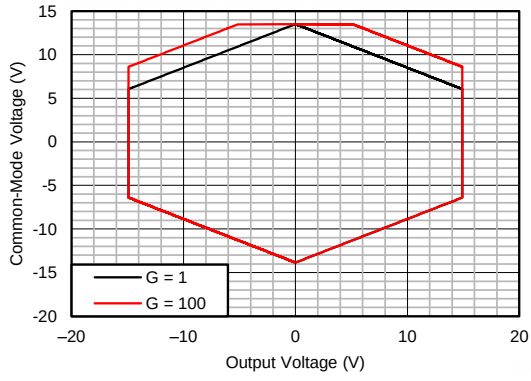
V_S = 5 V, G = 100

图 56. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V, V_{REF} = 0 V

图 57. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V, V_{REF} = 0 V

图 58. Input Common-Mode Voltage vs Output Voltage

7.3.4 Input Protection

The inputs of the INA828 device are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and 40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

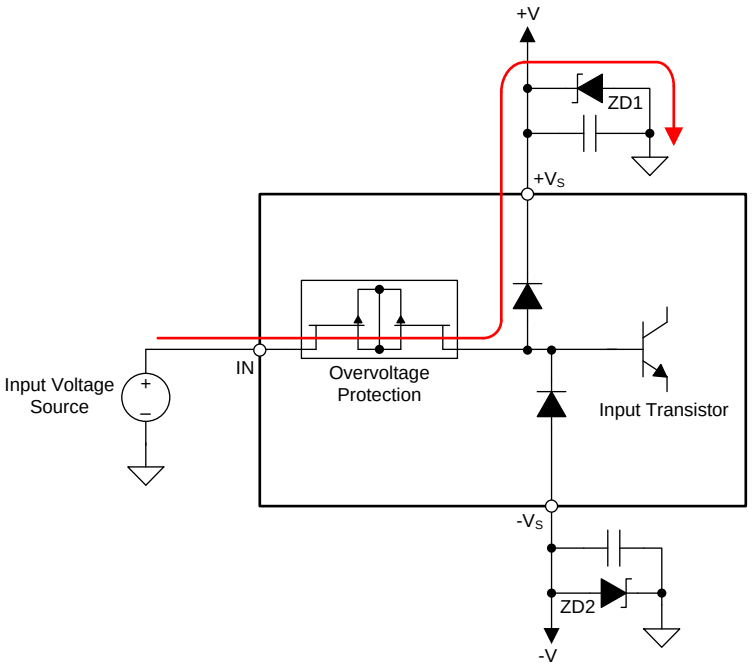


图 59. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, see 图 59. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in 图 59) must be placed on the power supplies to provide a current pathway to ground. 图 60 illustrates the input current for input voltages from –40 V to +40 V when the INA828 is powered by ±15-V supplies.

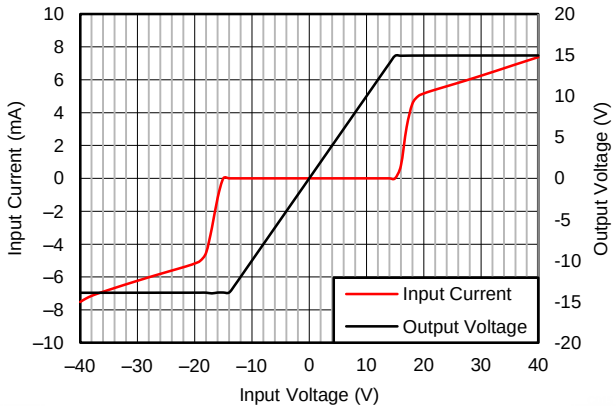


图 60. Input Current vs Input Overvoltage

7.3.5 Operating Voltage

The INA828 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

7.4 Device Functional Modes

The INA828 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA828 is 36 V (±18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Reference Terminal

The output voltage of the INA828 is developed with respect to the voltage on the reference terminal, REF. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise mid-supply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA828 can drive a single-supply ADC.

The voltage source applied to the reference terminal must have a low output impedance. As illustrated in 图 61, any resistance at the reference terminal (shown as R_{REF} in 图 61) is in series with one of the internal 40-kΩ resistors.

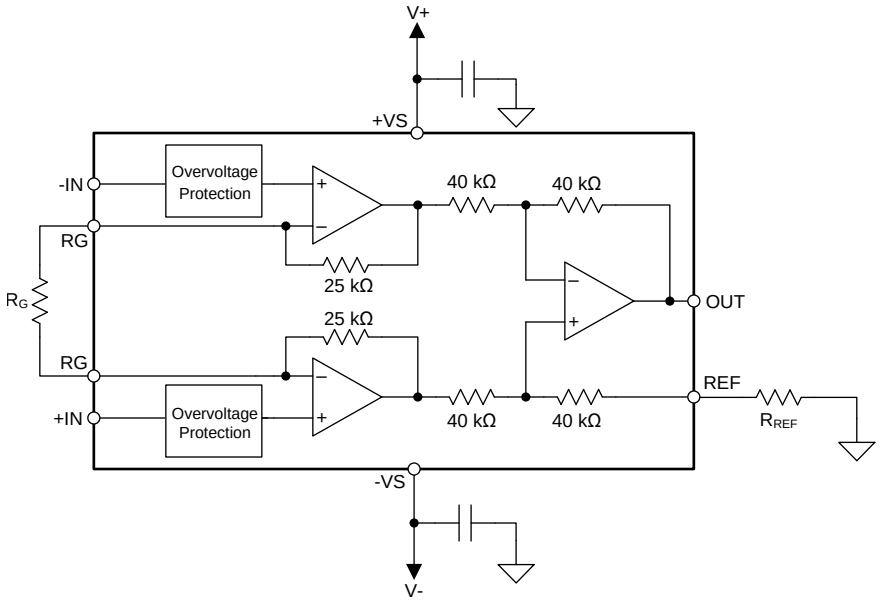


图 61. Parasitic Resistance Shown at the Reference Terminal

The parasitic resistance at the reference terminal, R_{REF}, creates an imbalance in the 4 resistors of the internal difference amplifier, resulting in degraded common-mode rejection ratio (CMRR). 图 62 shows the degradation in CMRR of the INA828 for increasing resistance at the reference terminal. For the best performance, keep the source impedance to the REF terminal, R_{REF}, below 5 Ω.

Reference Terminal (接下页)

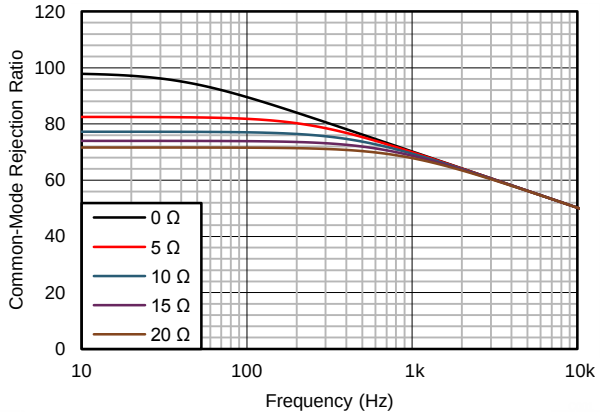


图 62. The Effect of Increasing Resistance at the Reference Terminal

Voltage reference ICs are an excellent option for providing a low-impedance voltage source for the reference terminal. However, if a resistor voltage divider is used to generate a reference voltage, it must be buffered by an op amp as shown in 图 63 to avoid CMRR degradation.

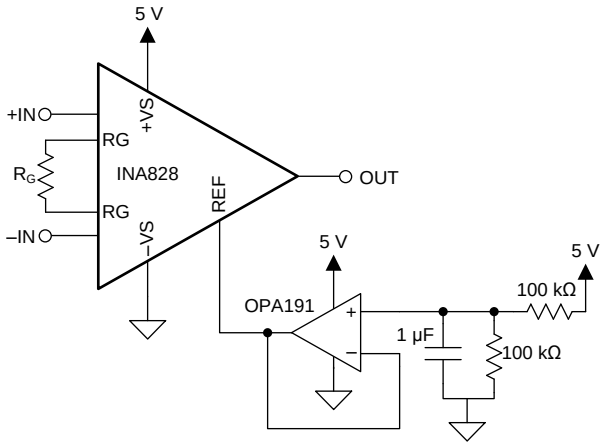


图 63. Using an Op Amp to Buffer Reference Voltages

8.2 Input Bias Current Return Path

The input impedance of the INA828 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 64 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA828, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in 图 64). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

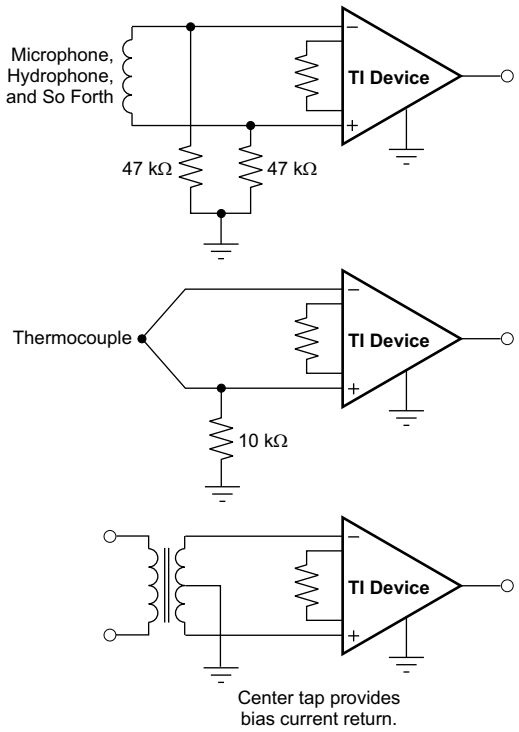


图 64. Providing an Input Common-Mode Current Path

8.3 PCB Assembly Effects on Precision

The printed-circuit board (PCB) assembly process, including reflow soldering, imparts thermal stresses on the INA828 which can degrade the precision of the device and must be considered in the development of very-high-precision systems. Baking the PCBs after the assembly process can restore the precision of the device to pre-assembly values. 图 65, 图 66, and 图 67 illustrate the effect of reflow soldering on the typical distribution of input offset voltage of the INA828. 图 65 shows the distribution of input offset voltage for a set of INA828 devices prior to the PCB assembly process. Exposing the INA828 to a JEDEC-standard thermal profile for reflow soldering produces the histogram shown in 图 66 on another set of INA828 devices. The standard deviation of input offset voltage has almost doubled due to the thermal stress imparted to the INA828 from the reflow process. However, baking INA828 units for 30 minutes at 125°C after the reflow soldering process produced the distribution given in 图 67. The post-reflow bake restored the standard deviation of the input offset voltage to pre-assembly levels.

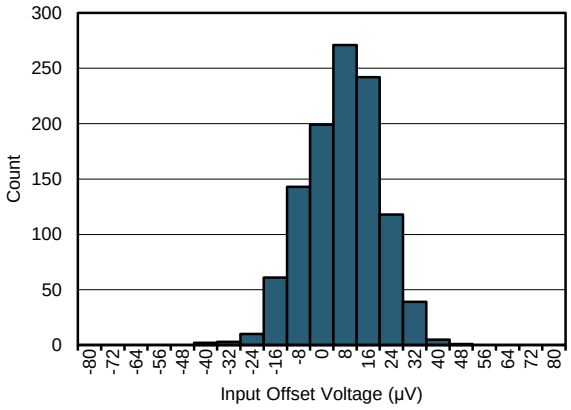


图 65. Typical Distribution of INA828 Input Offset Voltage Prior to Reflow Soldering

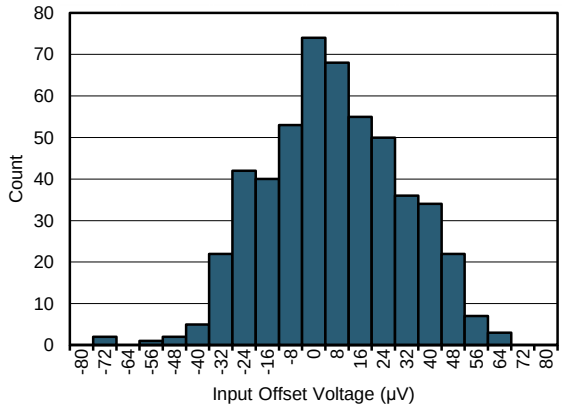


图 66. Typical Distribution of INA828 Input Offset Voltage After Reflow Soldering

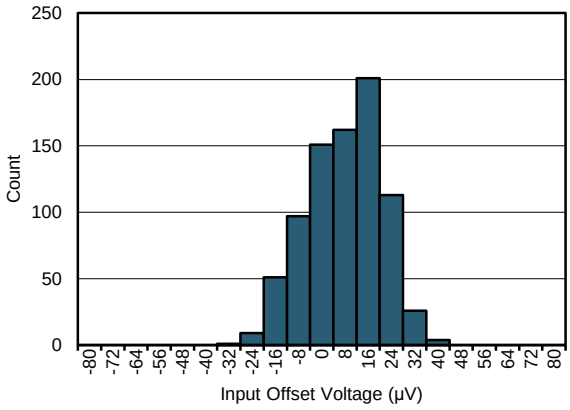


图 67. Typical Distribution of Post-Reflow INA828 Units Baked at 125°C for 30 Minutes

8.4 Typical Application

图 68 shows a three-terminal programmable-logic controller (PLC) design for the INA828. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

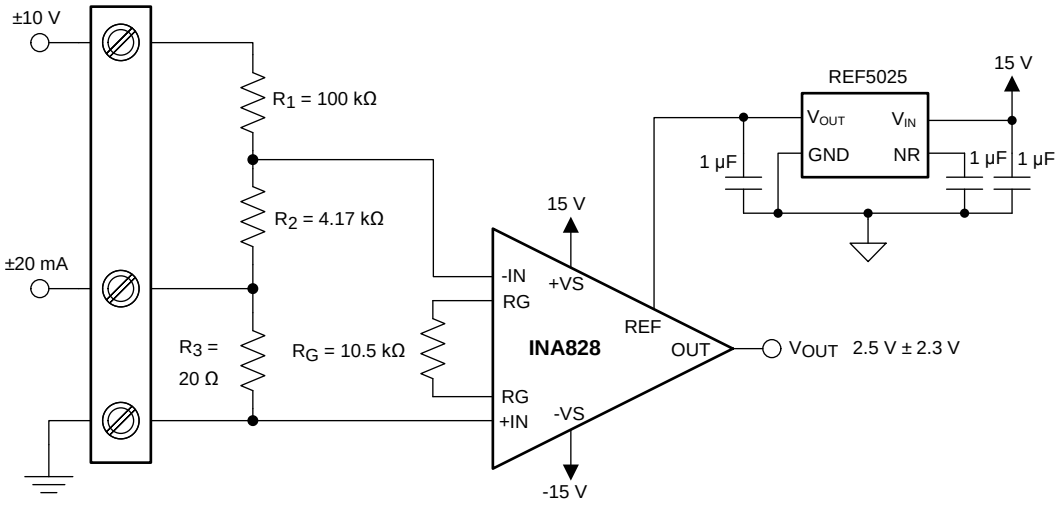


图 68. PLC Input (±10 V, 4 mA to 20 mA)

8.4.1 Design Requirements

For this application, the design requirements are:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20-mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

8.4.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 图 68: current input and voltage input. This design requires R_1 >> R_2 >> R_3. Given this relationship, 公式 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \quad (3)$$

where

- G represents the gain of the instrumentation amplifier
- V_D represents the differential voltage at the INA828 inputs
- V_{REF} is the voltage at the INA828 REF pin
- I_{IN} is the input current

公式 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \quad (4)$$

where

- V_{IN} is the input voltage

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Typical Application (接下页)

Use 公式 5 to calculate R_2 given V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \quad (5)$$

The value obtained from 公式 5 is not a standard 0.1% value, so 4.17 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

Use 公式 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \quad (6)$$

公式 7 calculates the gain-setting resistor value using the INA828 gain equation, 公式 1.

$$R_G = \frac{50\ k\Omega}{G - 1} = \frac{50\ k\Omega}{5.75 - 1} = 10.5\ k\Omega \quad (7)$$

10.5 kΩ is a standard 0.1% resistor value that can be used in this design.

8.4.3 Application Curves

图 69 and 图 70 show typical characteristic curves for the circuit in 图 68.

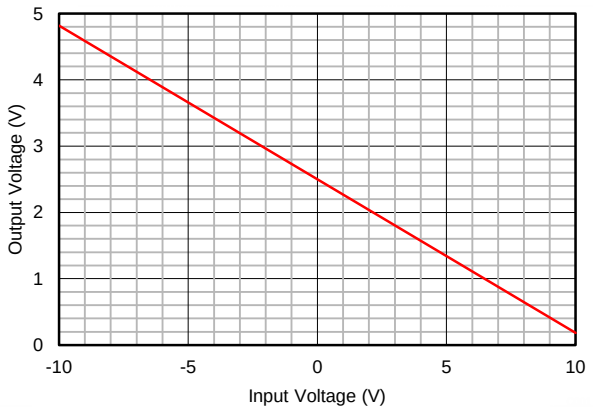


图 69. PLC Output Voltage vs Input Voltage

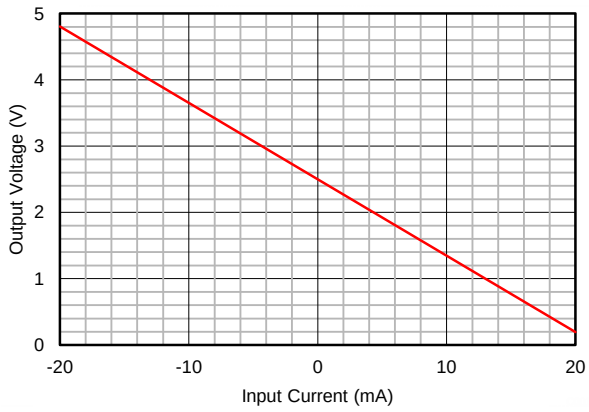


图 70. PLC Output Voltage vs Input Current

8.5 Other Application Examples

8.5.1 Resistance Temperature Detector Interface

图 71 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 to 5 V. The linearization technique employed is described in *Analog linearization of resistance temperature detectors*. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.

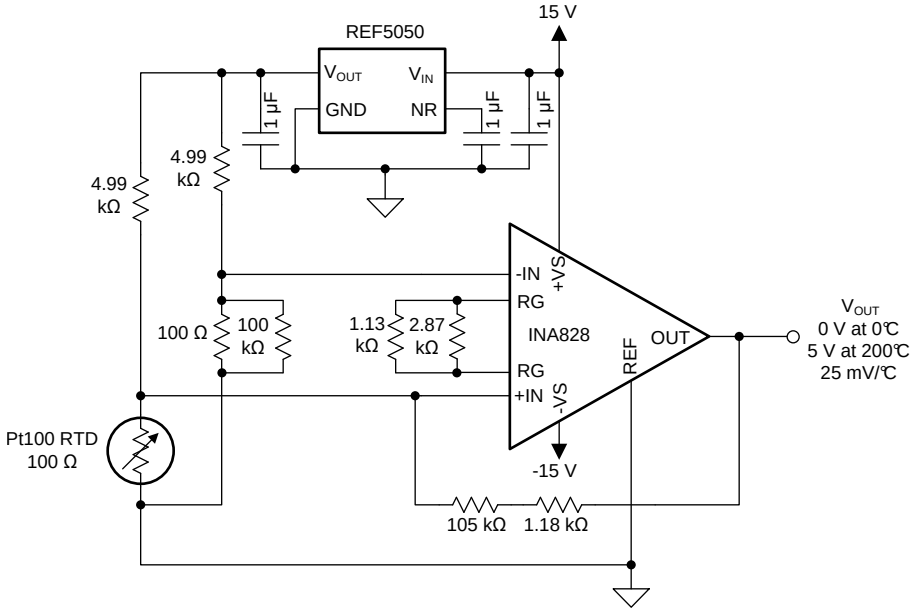


图 71. A 3-Wire Interface for RTDs With Analog Linearization

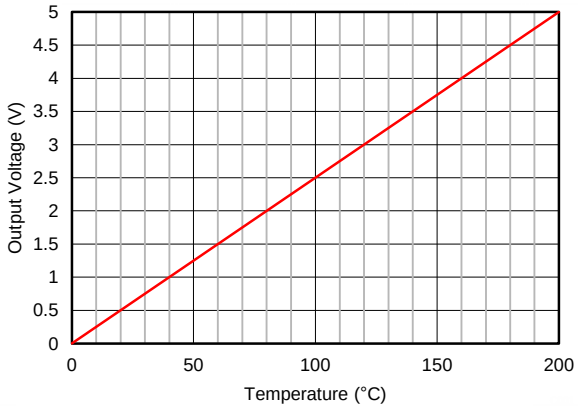


图 72. Transfer Function of 3-Wire RTD Interface

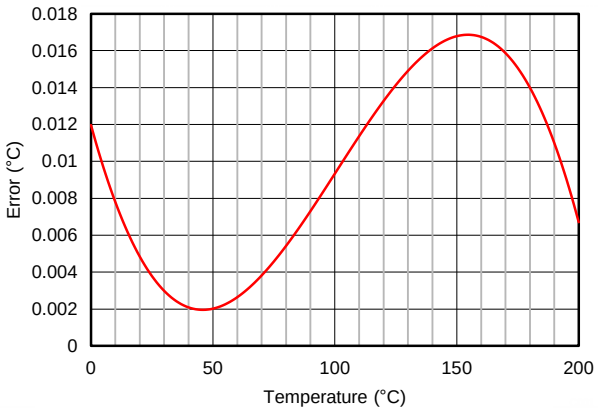


图 73. Temperature Error Over Full Temperature Range

9 Power Supply Recommendations

The nominal performance of the INA828 is specified with a supply voltage of ±15 V and mid-supply reference voltage. The device can also be operated using power supplies from ±1.5 V (3 V) to ±18 V (36 V) and non mid-supply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are illustrated in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Care must be taken to assure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 74, keeping R_G close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

10.2 Layout Example

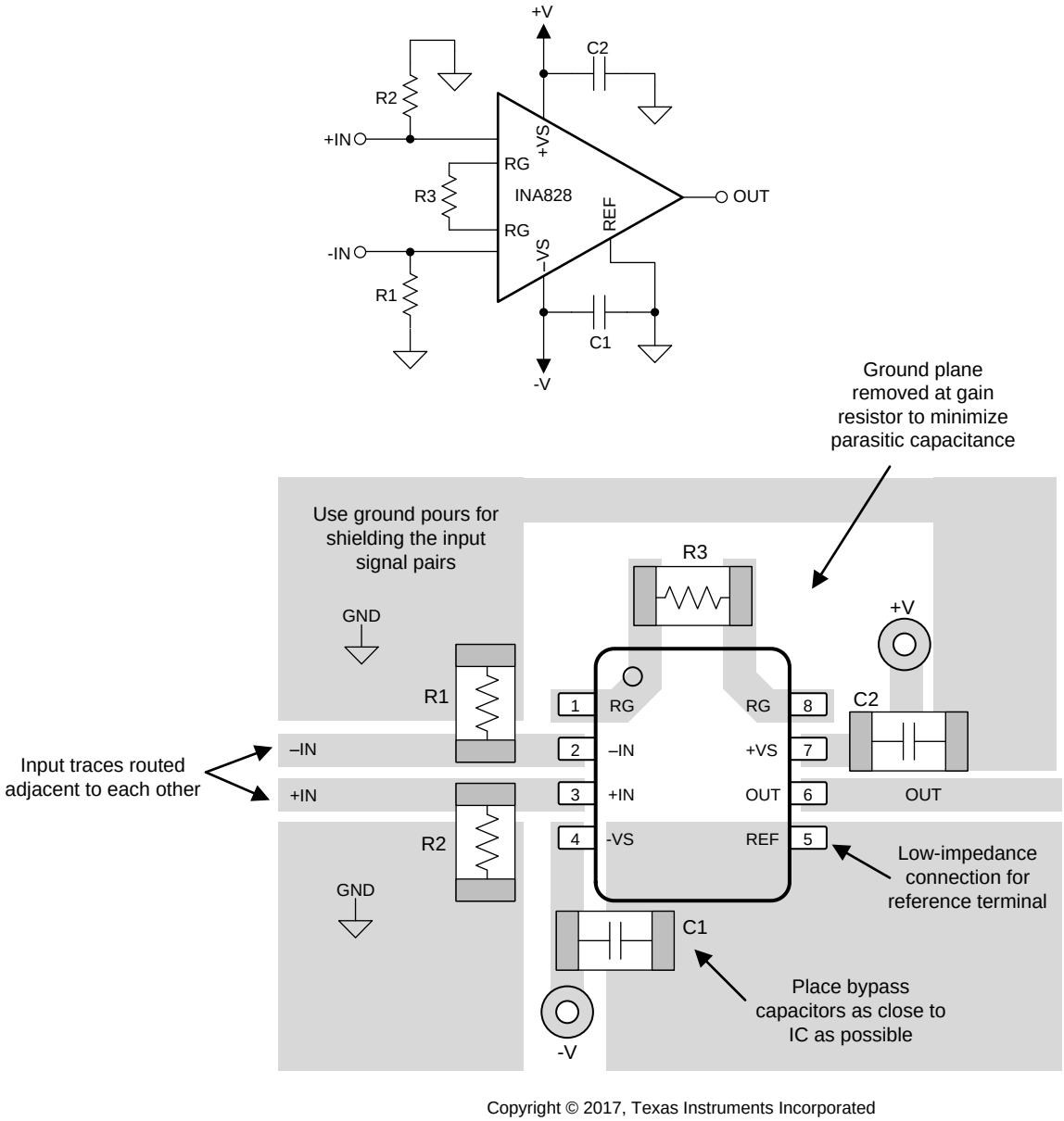


图 74. Example Schematic and Associated PCB Layout

11 器件和文档支持

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- 《*REF50xx 低噪声、极低漂移、高精度电压基准*》
- *OPA191 低功耗精密 36V e-trim CMOS 放大器*
- TINA-TI 软件文件夹
- INA 共模范围计算器

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA828ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

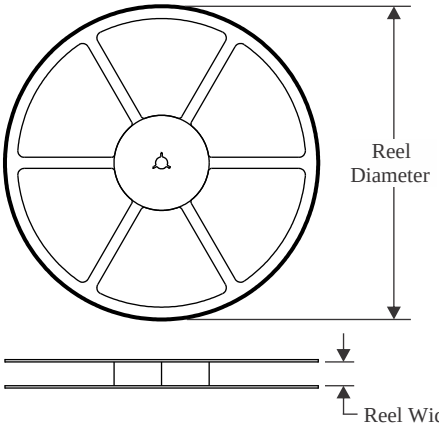
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

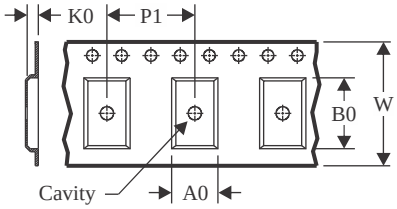
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

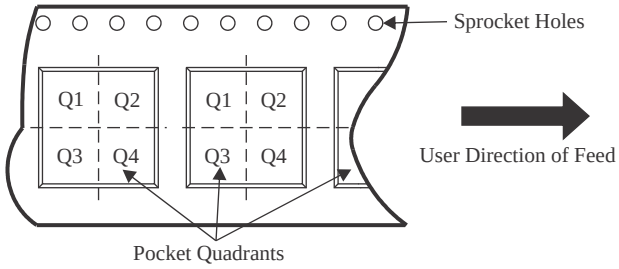


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

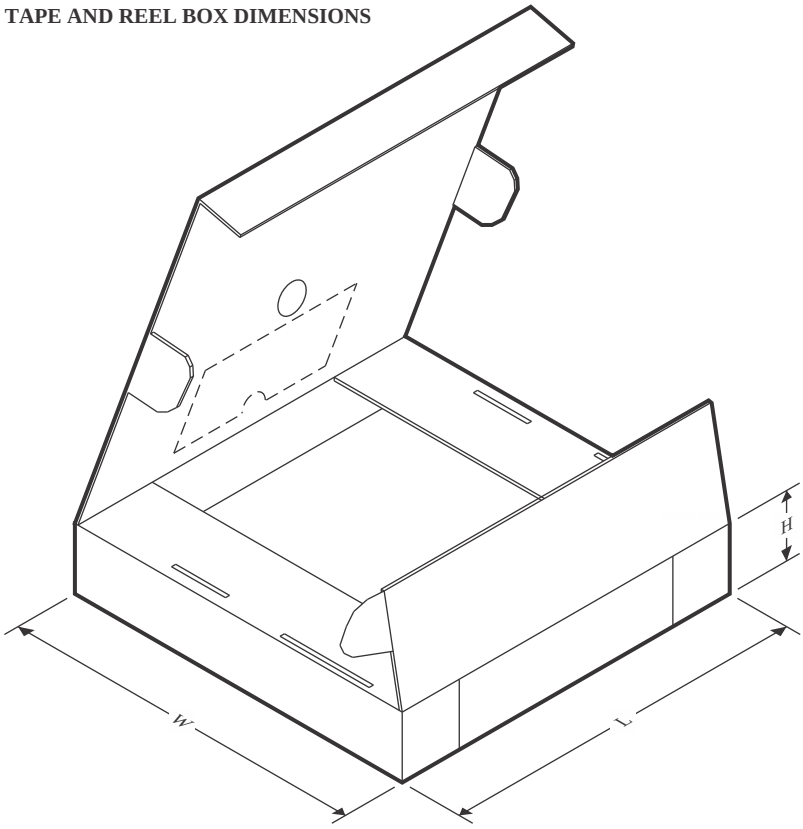
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA828IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

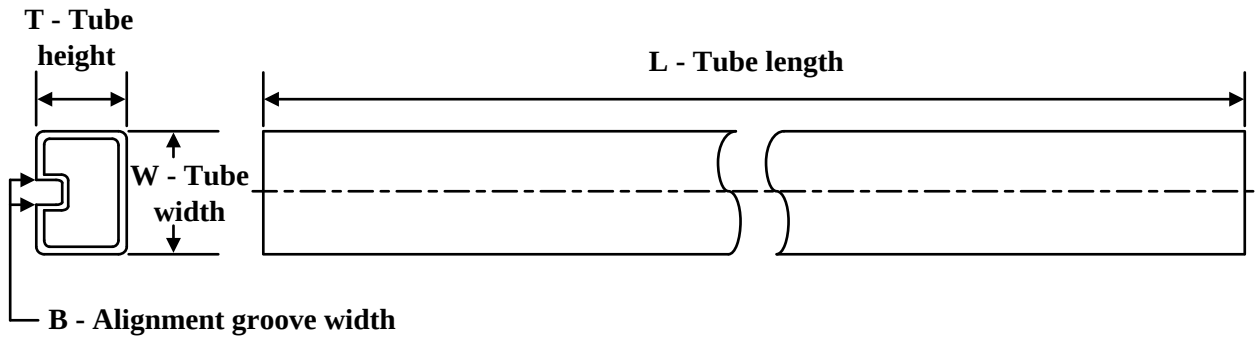
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

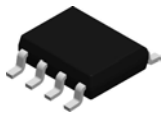
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA828IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA828ID	D	SOIC	8	75	506.6	8	3940	4.32

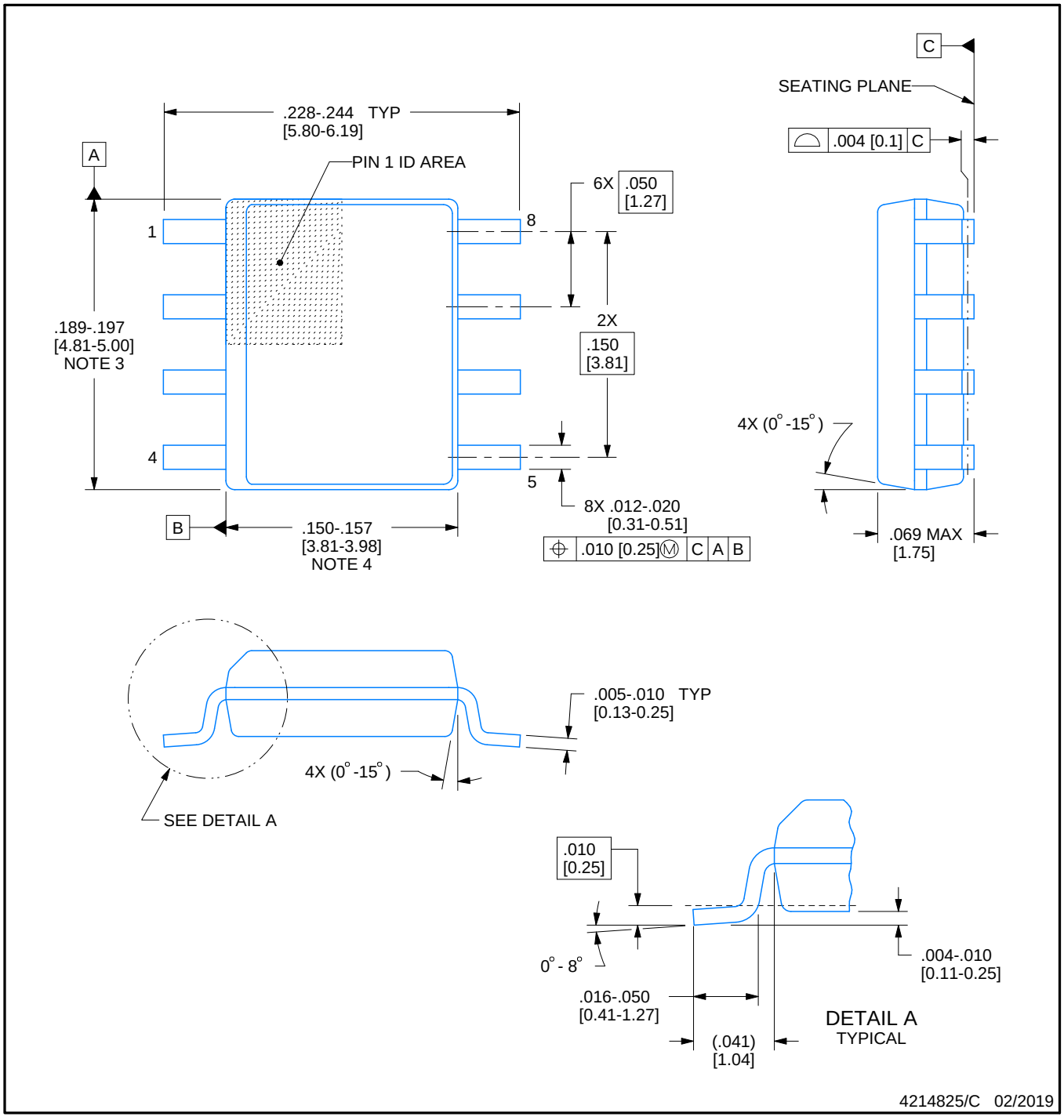


PACKAGE OUTLINE

D0008A

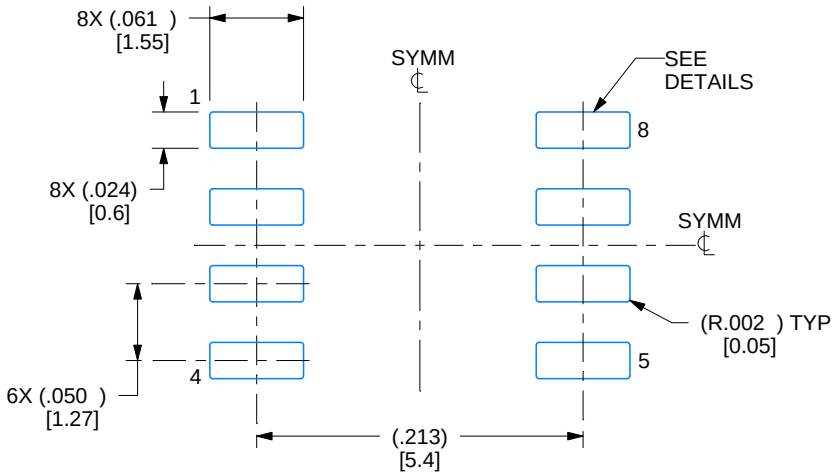
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

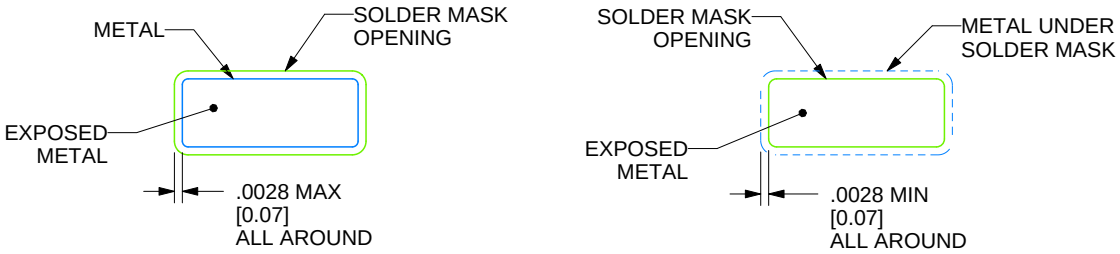


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

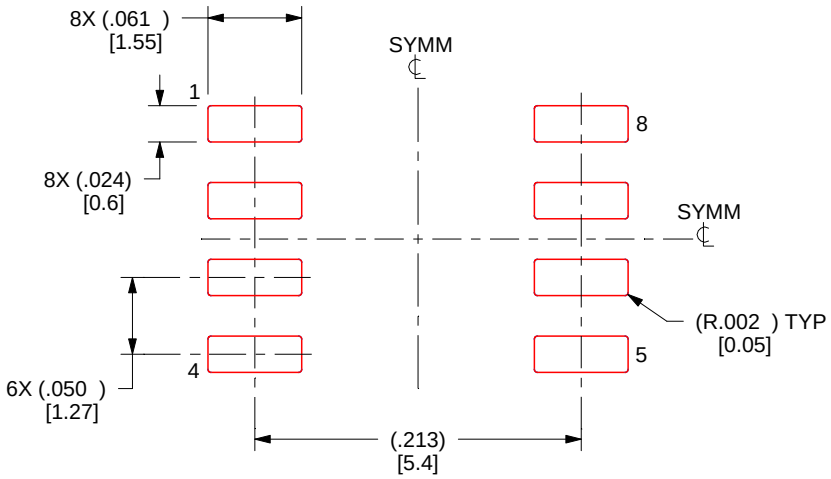
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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