1.2-MSPS/240-KSPS, ULTRA LOW POWER, 10-BIT, MINIATURE ANALOG-TO-DIGITAL CONVERTER WITH SERIAL INTERFACE

FEATURES

- Low power (XC7867 typical):
  0.42mW (3.3V，240KSPS)
  0.12mW (1.8V，240KSPS)
- Specified for V_{DD} of 1.5V to 4.5V
- High throughput:
  -1.2 MSPS for 10-Bit V_{DD}≥ 3 V
  -240 KSPS for 10-Bit V_{DD}≥ 1.5 V
- Automatic power-down
- ±0.5LSB INL, ±0.5LSB DNL
- No pipeline delays
- SPI Compatible serial interface
- Second-Source for ADS7867
- 6-Pin SOT-23 Package

APPLICATIONS

- Battery-powered systems
- Medical instruments
- Remote data acquisition
- Isolated data acquisition
- Automatic test equipment

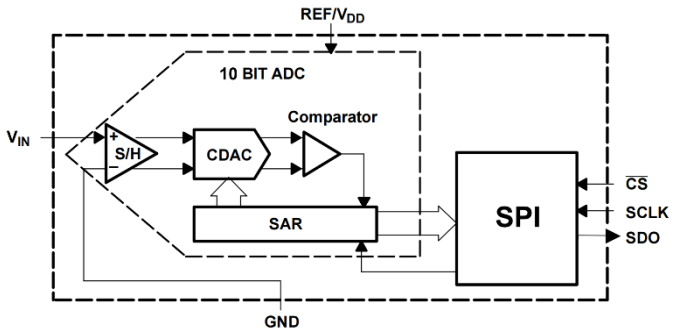


Figure 1. Functional Block Diagram

DESCRIPTION

The XC7867 is a 10-bit ADC (Analog-to-Digital Converter) chip that features ultra-low power, small size, unipolar, and single-ended input. The product operates from a single 1.5V - 4.5V power supply. Adopting advanced technology and design, it has a wide voltage working range: when powered by a single 1.5V - 3V power supply, the sampling rate can reach up to 240-KSPS; When powered by a single 3V - 4.5V power supply, the sampling rate can reach up to 1.2-MSPS.The XC7867 is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The XC7867 is second-source for the ADS7867 and consumes only one third dynamic power of their counterpart.

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 240 KSPS and f_{SCLK} = 3.4 MHz if 1.5 V ≤ V_{DD} ≤ 3.0 V; f_{SAMPLE} = 1200 KSPS and f_{SCLK} = 16.6 MHz if 3.0 V ≤ V_{DD} < 4.5 V. (unless otherwise noted)

PARAMETER	TEST CONDITIONS	XC7866			XC7867			XC7868			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			**12**			**10**			**8**		Bits
No missing codes		**12**			**10**			**8**			Bits
Integral linearity		**-1.5**		**1.5**	**-0.5**		**0.5**	**-0.5**		**0.5**	LSB
Differential linearity		**-1.5**		**1.5**	**-0.5**		**0.5**	**-0.5**		**0.5**	LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 3.4 MHz, 1.5 V ≤ V_{DD} ≤ 3.0 V			**200**			**240**			**280**	KSPS
	f_{SCLK} = 16.6 MHz, 3.0 V ≤ V_{DD} ≤ 4.5 V			**1000**			**1200**			**1400**	KSPS
SNR	f_{IN} = 30 kHz, 1.5 V ≤ V_{DD} < 4.5 V		**71.25**			**61.5**			**49.5**		dB
THD	f_{IN} = 30 kHz, 1.5 V ≤ V_{DD} < 4.5 V		**-84**			**-73**			**-70**		dB

XC7867

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.3 V		**125**	**180**	μA
		f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 2.5 V		**105**	**125**	
		f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		**67**	**100**	
		f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.3 V		**65**	**78**	μA
		f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 2.5 V		**42**	**48**	
		f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		**34**	**41**	
		f_{SAMPLE} = 120 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 3.3 V		**110**	**132**	μA
		f_{SAMPLE} = 120 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 2.5 V		**69**	**77**	
		f_{SAMPLE} = 120 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.8 V		**57**	**65**	
		f_{SAMPLE} = 50 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 3.3 V		**48**	**59**	μA
		f_{SAMPLE} = 50 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 2.5 V		**28**	**31**	
		f_{SAMPLE} = 50 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.8 V		**23**	**28**	
POWER DISSIPATION, XC7867						
Normal operation		f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.3 V		**0.42**	**0.60**	mW
		f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		**0.12**	**0.18**	mW
		f_{SAMPLE} = 120 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.8 V			**0.11**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

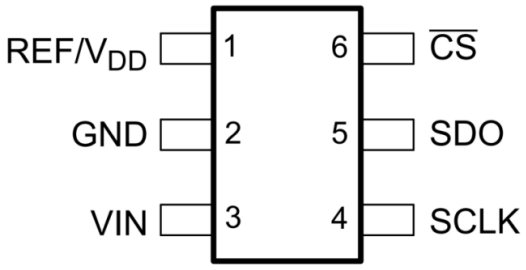


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
REF/V_{DD}	1	External reference input and power supply.
GND	2	Analog Ground. All analog input signals should be referred to this GND voltage.
VIN	3	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
SCLK	4	Serial clock input. This clock is used for clocking data out, and it is the source of conversion clock.
SDO	5	This is the serial data output of the conversion result. The serial stream comes with MSB first.
$\overline{CS}$	6	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the devices and frames the serial data transfer.

TIMING DIAGRAM

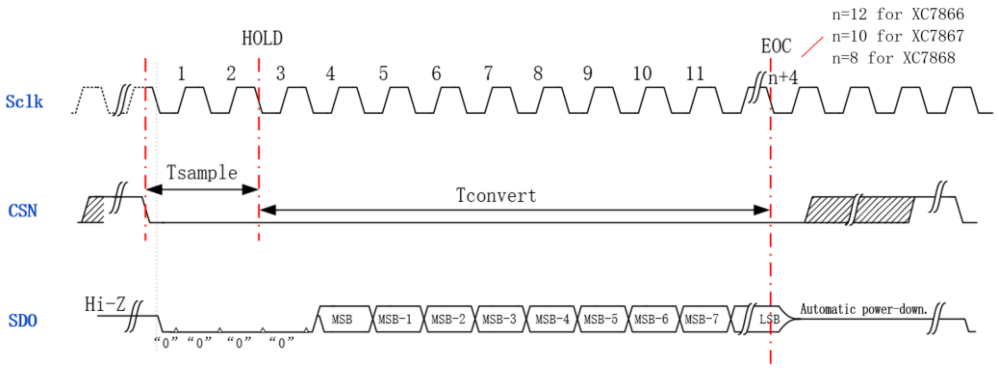


Figure 3. Timing Diagram

On the $\overline{CS}$ falling edge, the part begins to power up and the track-and-hold, which was in hold while the part was in power-down, goes into track mode. The conversion is also initiated at this point. On the third SCLK falling edge after the $\overline{CS}$ falling edge, the track and-hold returns to hold mode. Although $\overline{CS}$ can idle high or low between conversions, bringing $\overline{CS}$ high once the conversion is complete is recommended to save power. At 14 falling edges of the SCLK, the SDO enters three-state and the conversion cycle ends.

TYPICAL CONNECTION

For a typical connection circuit for the XC7867 see Figure 4. The 1.8 V supply should come from a stable power supply such as an LDO. A 1-µF and a 10-nF decoupling capacitor are required between the V_{DD} and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter.

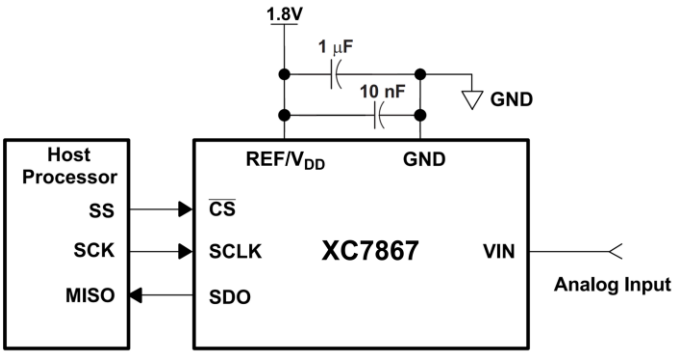


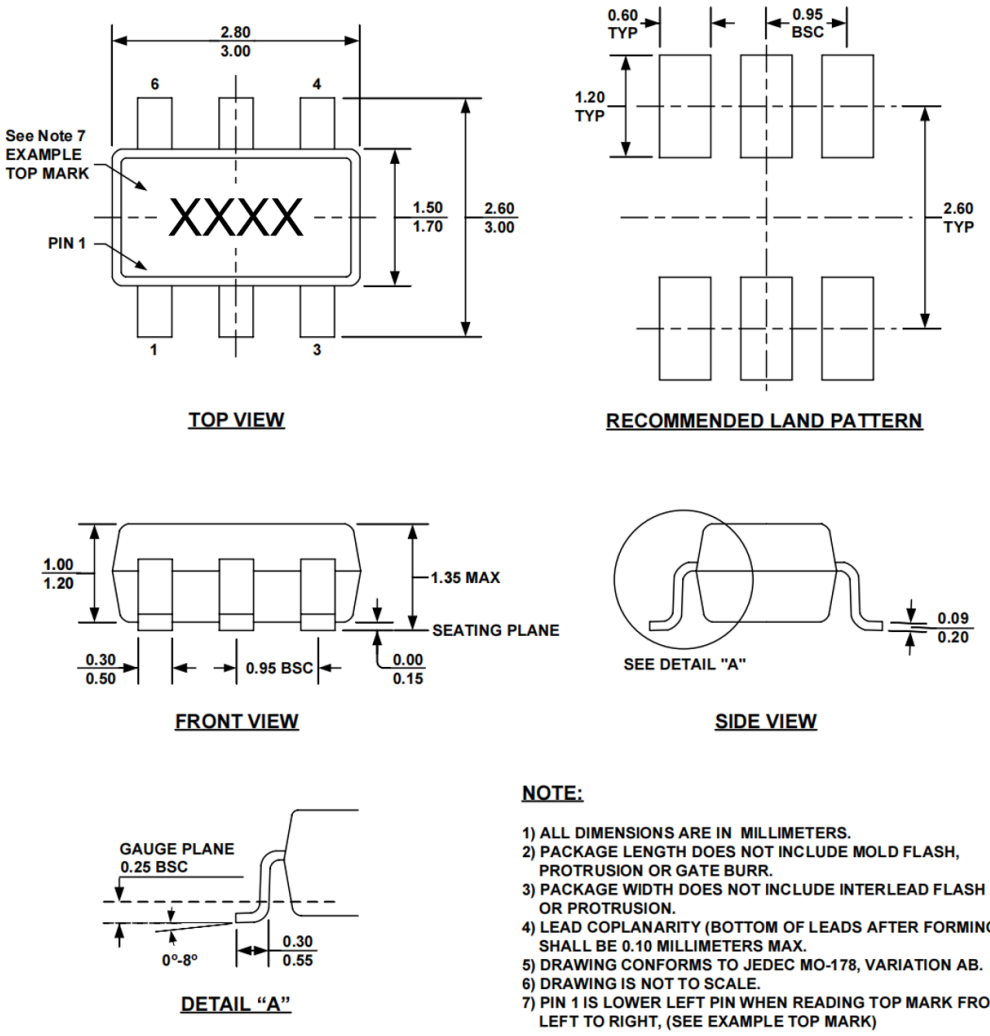
Figure 4. Typical Circuit Configuration

CONVERSION RESULTS

DESCRIPTION	ANALOG INPUT VOLTAGE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
XC7867（10bit）			
Least Significant Bit (LSB)	V_{DD}/1024		
Full Scale	V_{DD} – 1LSB	11 1111 1111	3FF
Mid Scale	V_{DD}/2	10 0000 0000	200
Mid Scale – 1LSB	V_{DD}/2 – 1LSB	01 1111 1111	1FF
Zero	0V	00 0000 0000	000

The MSB of the converted result follows 4 leading zeros. When supplies are first applied to the devices, a dummy conversion should be performed to ensure that the parts are in power-down mode, the track-and-hold is in hold mode, and SDO is in three-state. Once a data transfer is complete (SDO has returned to three-state), another conversion can be initiated after the quiet time, has elapsed, by bringing $\overline{CS}$ low again.

OUTLINE DIMENTIONS



NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.