Brückewell

MSH80N087

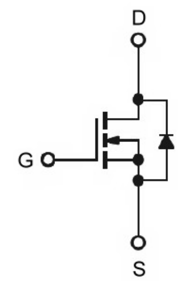
N-Channel 80-V (D-S) MOSFET

Description

The device is using trench DMOS technology. This advanced technology has been especially tailored to minimize $R_{DS(ON)}$, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Graphic Symbol



Features

- $R_{DS(ON)}$ =8.7mΩ @ V_{GS} =10V
- Super Low Gate Charge
- Excellent dv/dt Capability
- 100% EAS Guaranteed
- Green Device Available

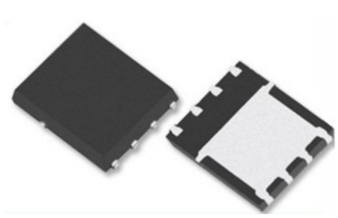
Typical Applications

- Networking
- Load Switch
- Synchronous Rectifier
- Quick Charger

Package type：PDFN 5X6

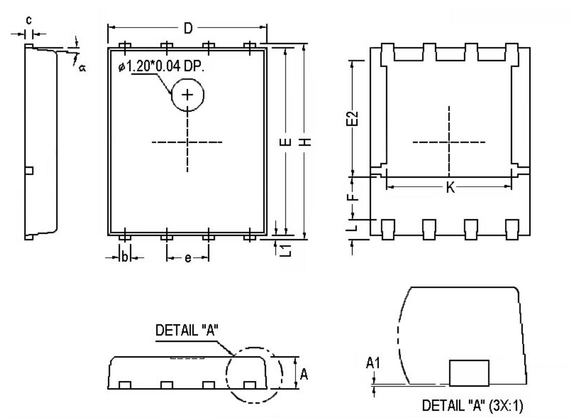
Packing & Order Information

3,000/Reel



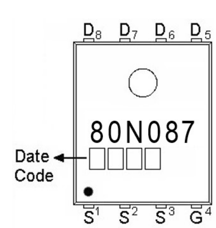
RoHS Compliant

Package Dimension



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.85	1.00	1.15	E	5.70	-	5.90
A1	0.00	-	0.10	e	-	1.27	-
b	0.30	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	L	-	0.60	-
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.10 Ref.			α	0°	-	12°
E2	3.50 Ref.			K	3.70	3.90	4.10

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	60	A
	Continuous Drain Current[1] (T_C =100°C)	38	A
I_{DM}	Pulsed Drain Current[1,2]	170	A
I_{AS}	Single Pulse Avalanche Current, L =0.1mH[3]	30	A
E_{AS}	Single Pulse Avalanche Energy, L =0.1mH[3]	45	mJ
P_D	Power Dissipation[4] (T_C =25°C)	52	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to 150	°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	65	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case[1]	2.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	1.2	-	2.3	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	80	-	-	V
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =64V, V_{GS} =0V, T_J =25°C	-	-	1	μA
		V_{DS} =64V, V_{GS} =0V, T_J =55°C			5	
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =10V, I_D =10A	-	7.2	8.7	mΩ
		V_{GS} =4.5V, I_D =10A	-	10.5	13	
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =50V, L =0.1mH, I_{AS} =15A	11	-	-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =1A, V_{GS} =0V, T_J =25°C	-	-	1.2	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	30	A
I_{SM}	Pulsed Source Current[2,6]		-	-	60	

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=50, V_{GS}=10V, L=0.1mH, I_{AS}=30A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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Dynamic						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Q_g	Total Gate Charge[2]	V_{DS} =40V I_D =10A V_{GS} =10V	--	29	--	nC
Q_{gs}	Gate-Source Charge		--	7.7	--	
Q_{gd}	Gate-Drain Charge		--	5.3	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DS} =40V I_D =10A V_{GS} =10V R_G =3.3Ω	--	6.2	--	ns
t_r	Rise Time		--	19	--	
$t_{d(off)}$	Turn-Off Delay Time		--	9.4	--	
t_f	Fall Time		--	36	--	
C_{ISS}	Input Capacitance	V_{DS} =40V V_{GS} =0V f =1.0MHz	--	1738	--	pF
C_{OSS}	Output Capacitance		--	317	--	
C_{RSS}	Reverse Transfer Capacitance		--	12	--	
trr	Reverse Recovery Time	I_F=10A, dI/dt=100A/µs, Tj=25°C		35		nS
Qrr	Reverse Recovery Charge			62		nC
Rg	Gate Resistance	V_{DS} =0V, V_{GS} =0V, f =1.0MHz		1.5		Ω

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- **Typical Electrical Characteristics**

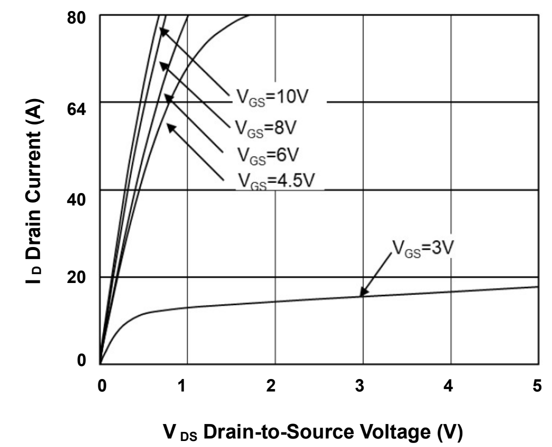

FIG.1-Typical Output Characteristics

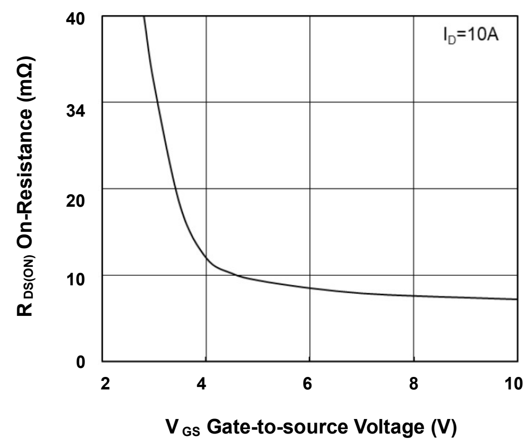

FIG.2-On-Resistance vs. G-S Voltage

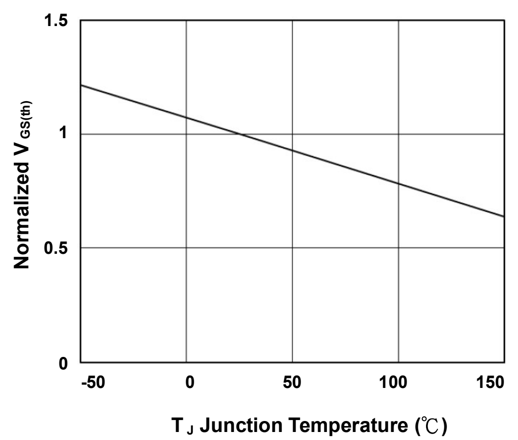

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

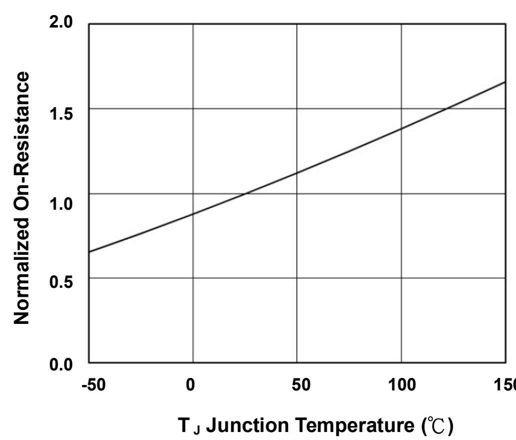

FIG.4-Normalized R_{DSON} vs. T_J

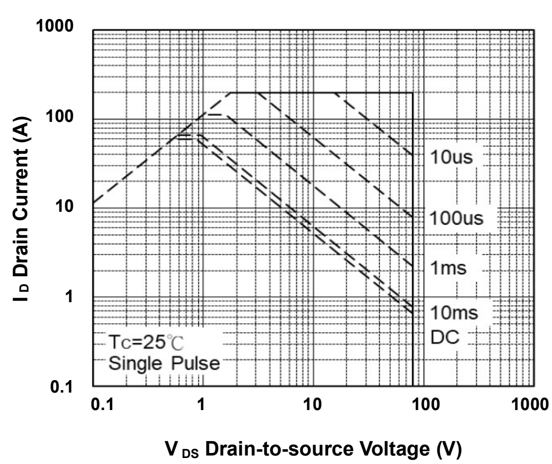

FIG.5-Safe Operating Area

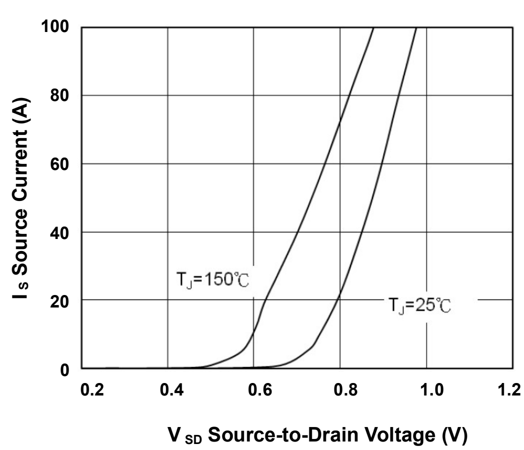

FIG.6-Source Drain Forward Characteristics

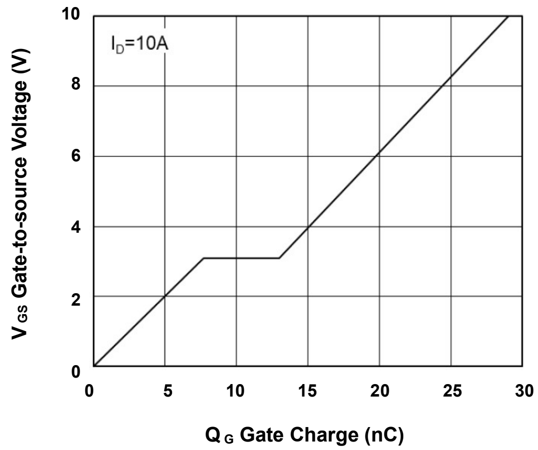

FIG.7-Gate Charge Characteristics

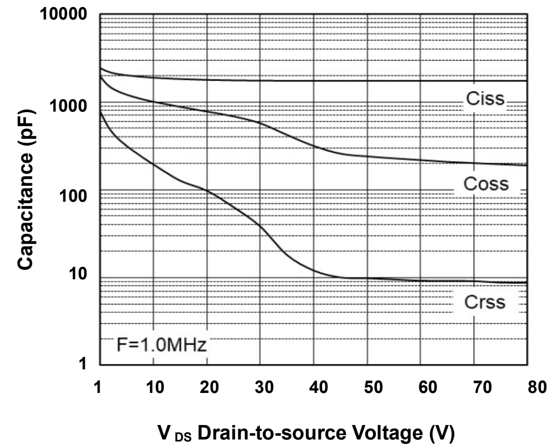

FIG.8-Capacitance Characteristics

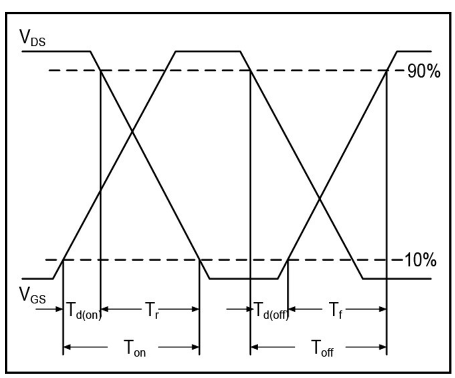

FIG.9-Switching Time Waveform

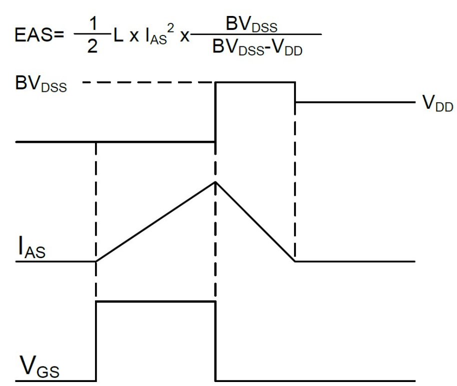

FIG.10-Unclamped Inductive Switching Waveform

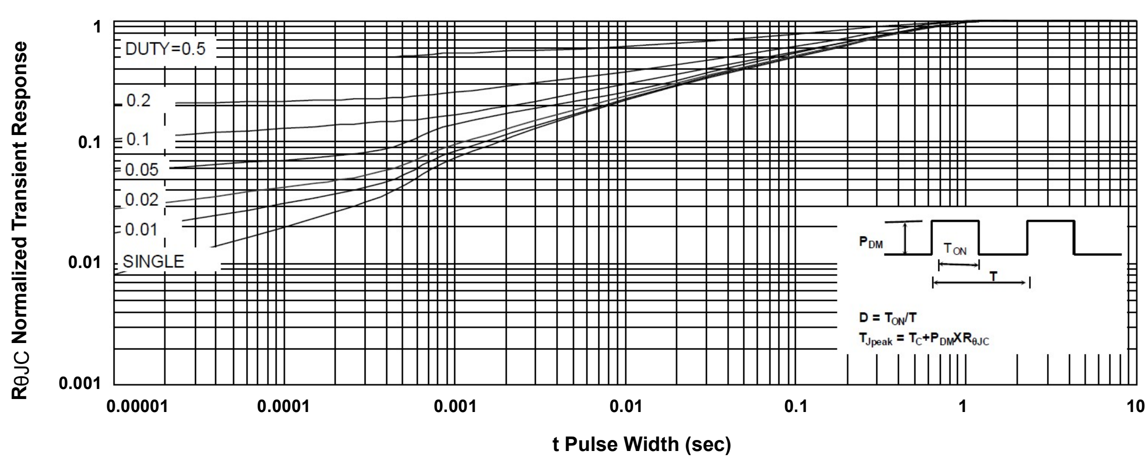

FIG.11-Normalized Maximum Transient Thermal Impedance

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