



HD3SS3415 4 通道高性能差分开关

1 特性

- 兼容多种运行速率高达 12Gbps 的接口标准，包括 PCI Express Gen III 和 USB 3.0
- 3dB 差分带宽宽达 8GHz 以上
- 出色动态特性（4GHz 时）
 - 串扰 = -35dB
 - 断开隔离 = -19dB
 - 插入损耗 = -1.5dB
 - 回波损耗 = -11dB
- VDD 运行电压范围为 $3.3V \pm 10\%$
- 小型 3.5mm × 9mm、42 引脚 WQFN 封装
- 普遍使用的行业标准引脚布局

2 应用

- 台式机和笔记本个人电脑 (PC)
- 服务器/储存区网络
- PCI EXPRESS 背板
- 共享 I/O 端口

3 说明

HD3SS3415 是一款高速无源开关，能够切换四个差分通道，包括在 PC/服务器应用中将两条完整 PCI Express x1 信道从一个源切换到两个目标位置之一。凭借双向功能，HD3SS3415 还支持一个目标设备与两个源设备相连，例如两个平台共享一个外设。HD3SS3415 具备一个单一控制线路（SEL 引脚），可用于控制端口 A 与端口 B 或者端口 C 之间的信号路径。

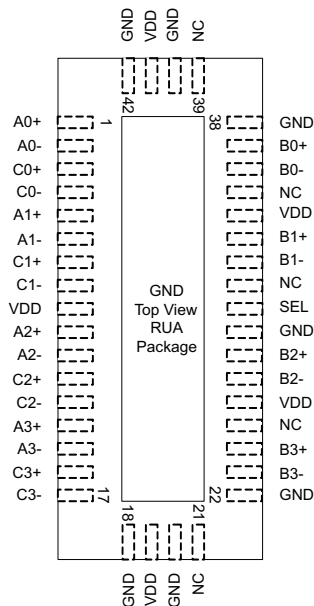
HD3SS3415 采用行业标准的 42 引脚 WQFN 封装，封装尺寸与其他几家供应商提供的器件相同。该器件在 0°C 至 70°C 的完整温度范围内由 3.3V 单电源供电运行。

器件信息⁽¹⁾

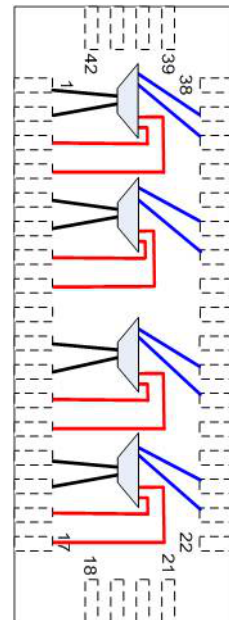
器件型号	封装	封装尺寸（标称值）
HD3SS3415	WQFN (42)	9.00mm x 3.50mm

(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。

HD3SS3415 引脚分配



HD3SS3415 开关直通布线



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2015) to Revision C	Page
• 已更改 <i>HD3SS3415</i> 引脚分配以及 <i>HD3SS3415</i> 开关直通布线图	1
• Changed temperature From: industrial temperature range of –40°C to 85°C To: industrial temperature range of 0°C to 70°C in the <i>Overview</i> section	12

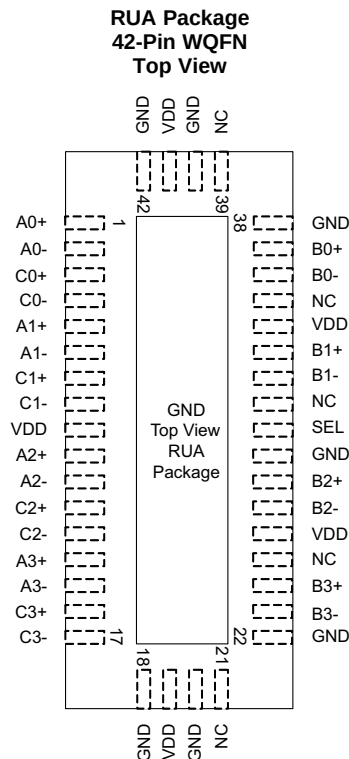
Changes from Revision A (July 2015) to Revision B	Page
• Changed the Storage temperature MIN value From: 65 To: –65 in the <i>Absolute Maximum Ratings</i> ⁽¹⁾⁽²⁾ table	6

Changes from Original (February 2012) to Revision A	Page
• 已添加 引脚配置和功能部分, <i>ESD</i> 额定值表, 特性 描述 部分, 器件功能模式, 应用和 实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及 机械、封装和可订购信息部分	1
• 已删除 说明部分中的“工业”一词。	1
• 已更改 说明第二段中的“-40 至 0”和“-85 至 70°C”	1
• Changed T _A spec values from –40°C MIN and 85°C MAX to 0°C MIN and 70°C MAX in the <i>Recommended Operating Conditions</i> table.	6

5 说明（续）

HD3SS3415 是一款通用的四通道高速复用/解复用型开关，可用于在电路板上的两个不同位置间路由高速信号。虽然 HD3SS3415 专为 PCI Express Gen III 应用而设计，不过也支持多种差分幅值 $<1800\text{ mVpp}$ 且共模电压 $<2\text{ V}$ 的其他高速数据协议，如同 USB 3.0 和 DisplayPort 1.2 一样。该器件的一个选择输入 (SEL) 引脚可通过系统内或微控制器的一个可用 GPIO 引脚轻松控制。

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCH PORT A			
A0+	1	I/O	Port A, Channel 0, High Speed Positive Signal
A0–	2		Port A, Channel 0, High Speed Negative Signal
A1+	5		Port A, Channel 1, High Speed Positive Signal
A1–	6		Port A, Channel 1, High Speed Negative Signal
A2+	10		Port A, Channel 2, High Speed Positive Signal
A2–	11		Port A, Channel 2, High Speed Negative Signal
A3+	14		Port A, Channel 3, High Speed Positive Signal
A3–	15		Port A, Channel 3, High Speed Negative Signal
SWITCH PORT B			
B0+	37	I/O	Port B, Channel 0, High Speed Positive Signal
B0–	36		IPort B, Channel 0, High Speed Negative Signal
B1+	33		Port B, Channel 1, High Speed Positive Signal
B1–	32		Port B, Channel 1, High Speed Negative Signal
B2+	28		Port B, Channel 2, High Speed Positive Signal
B2–	27		Port B, Channel 2, High Speed Negative Signal
B3+	24		Port B, Channel 3, High Speed Positive Signal
B3–	23		Port B, Channel 3, High Speed Negative Signal

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCH PORT C			
C0+	3	I/O	Port C, Channel 0, High Speed Positive Signal
C0–	4		Port C, Channel 0, High Speed Negative Signal
C1+	7		Port C, Channel 1, High Speed Positive Signal
C1–	8		Port C, Channel 1, High Speed Negative Signal
C2+	12		Port C, Channel 2, High Speed Positive Signal
C2–	13		Port C, Channel 2, High Speed Negative Signal
C3+	16		Port C, Channel 3, High Speed Positive Signal
C3–	17		Port C, Channel 3, High Speed Negative Signal
CONTROL, SUPPLY, AND NO CONNECT			
GND	18, 20, 22, 29, 38, 40, 42, Center Pad	Supply	Negative power supply voltage
NC	21, 25, 31, 35, 39	–	Electrically not connected
SEL	30	I	Select between port B or port C. Internally tied to GND via 100kΩ resistor
VDD	9, 19, 26, 34, 41	Supply	Positive power supply voltage

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage (V_{DD})	Absolute minimum/maximum supply voltage range	−0.5	4	V
Voltage	Differential I/O	−0.5	4	V
	Control pin (SEL)	−0.5	$V_{DD}+0.5$	
Storage temperature (T_{stg})		−65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values for all parameters are at $V_{DD} = 3.3V$ and $T_A = 25^{\circ}C$. (Temperature limits are specified by design)

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	Input high voltage (SEL Pin)	2.0		V_{DD}	V
V_{IL}	Input low voltage (SEL Pin)	−0.1		0.8	V
V_{I/O_Diff}	Differential voltage (differential pins)	Switch I/O diff voltage		1.8	VPP
V_{I/O_CM}	Common voltage (differential pins)	Switch I/O common mode voltage		2.0	V
T_A	Operating free-air temperature	Ambient temperature		70	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		HD3SS3415	UNIT
		TQFN (RUA)	
		42 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	27.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

 R_{SC} and $R_{LOAD} = 50\ \Omega$ and $C_L = 50\text{ pF}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input High Voltage (SEL)	$V_{DD} = 3.6\text{ V}; V_{IN} = V_{DD}$			95	μA
I_{IL}	Input Low Voltage (SEL)	$V_{DD} = 3.6\text{ V}; V_{IN} = \text{GND}$			1	μA
I_{LK}	Leakage Current (Differential I/O pins)	$V_{DD} = 3.6\text{ V}; V_{IN} = 0\text{ V}; V_{OUT} = 2\text{ V}$ (I_{LK} On OPEN outputs) [Ports B and C]			130	μA
		$V_{DD} = 3.6\text{ V}; V_{IN} = 2\text{ V}; V_{OUT} = 0\text{ V}$ (I_{LK} On OPEN outputs) [Port A]			4	
I_{DD}	Supply Current	$V_{DD} = 3.6\text{ V}; \text{SEL} = V_{DD}/\text{GND}; \text{Outputs Floating}$		4.7	6	mA
C_{ON}	Outputs ON Capacitance	$V_{IN} = 0\text{ V}; \text{Outputs Open}; \text{Switch ON}$		1.5		pF
C_{OFF}	Outputs OFF Capacitance	$V_{IN} = 0\text{ V}; \text{Outputs Open}, \text{Switch OFF}$		1		pF
R_{ON}	Output ON resistance	$V_{DD} = 3.3\text{ V}; V_{CM} = 0.5\text{ V to } 1.5\text{ V}; I_O = -8\text{ mA}$		5	8	Ω
ΔR_{ON}	On resistance match between channels	$V_{DD} = 3.3\text{ V}; -0.35\text{ V} \leq V_{IN} \leq 1.2\text{ V}; I_O = -8\text{ mA}$			2	Ω
	On resistance match between pairs of the same channel	$V_{DD} = 3.3\text{ V}; -0.35\text{ V} \leq V_{IN} \leq 1.2\text{ V}; I_O = -8\text{ mA}$			0.7	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON(MAX)} - R_{ON(MIN)}$)	$V_{DD} = 3.3\text{ V}; -0.35\text{ V} \leq V_{IN} \leq 1.2\text{ V}$			1.15	Ω
t_{PD}	Switch propagation delay	R_{SC} and $R_{LOAD} = 50\ \Omega$			85	ps
	SEL-to-switch T_{on}	R_{SC} and $R_{LOAD} = 50\ \Omega$		70	250	ns
	SEL-to-switch T_{off}			70	250	
T_{SKEW_Inter}	Inter-pair output skew (CH-CH)	R_{SC} and $R_{LOAD} = 50\ \Omega$			20	ps
T_{SKEW_Intra}	Intra-pair output skew (bit-bit)				8	ps
R_L	Differential return loss (VCM = 0 V) See Typical Characteristics	$f = 0.3\text{ MHz}$		-28		dB
		$f = 2500\text{ MHz}$		-12		
		$f = 4000\text{ MHz}$		-11		
X_{TALK}	Differential Crosstalk(VCM = 0 V) See Typical Characteristics	$f = 0.3\text{ MHz}$		-90		dB
		$f = 2500\text{ MHz}$		-39		
		$f = 4000\text{ MHz}$		-35		
O_{IRR}	Differential Off-Isolation(VCM = 0 V) See Typical Characteristics	$f = 0.3\text{ MHz}$		-75		dB
		$f = 2500\text{ MHz}$		-22		
		$f = 4000\text{ MHz}$		-19		
I_L	Differential Insertion Loss (VCM = 0 V) See Typical Characteristics	$f = 0.3\text{ MHz}$		-0.5		dB
		$f = 2500\text{ MHz}$		-1.1		
		$f = 4000\text{ MHz}$		-1.5		
BW	Band Width	At -3 dB		8		GHz

7.6 Dissipation Ratings

		MIN	MAX	UNIT
P_D	Power Dissipation	15.5	21.6	mW

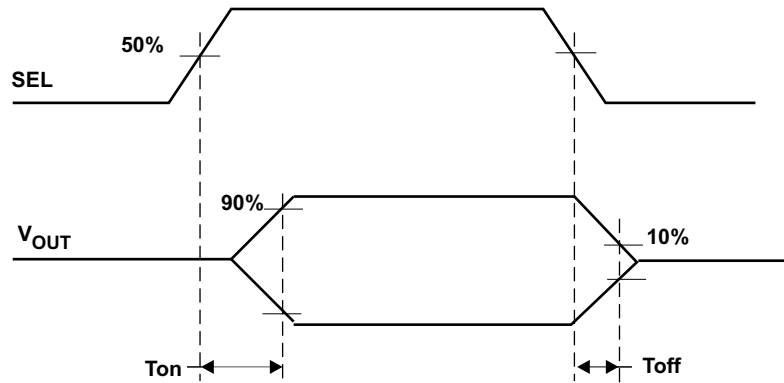
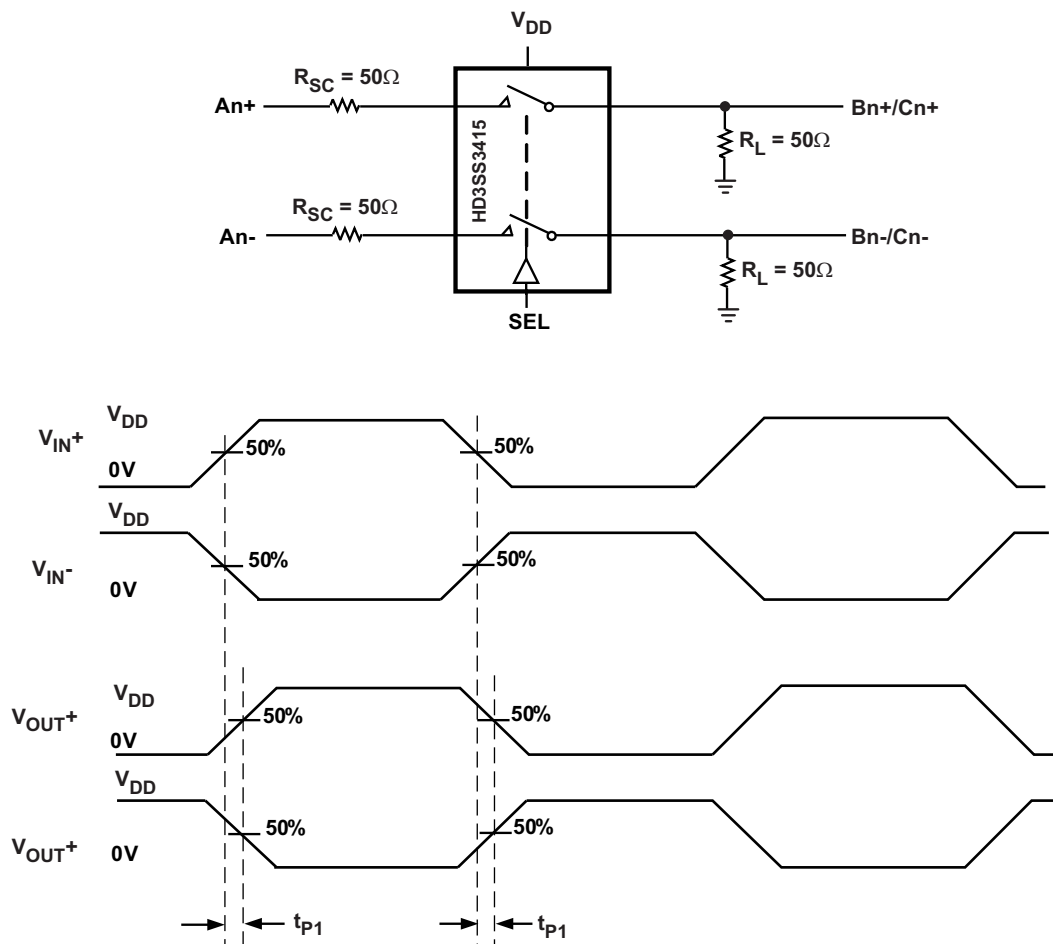


Figure 1. Select to Switch Output On (T_{ON}) and Off (T_{OFF}) Timing Diagram



$T_{SKEWinter}$ = Difference between t_{PD} for any two pairs of outputs

$T_{SKEWintra}$ = Difference between t_{P1} and t_{P2} of same pair

Figure 2. Propagation Delay Timing Diagram and Test Setup

7.7 Typical Characteristics

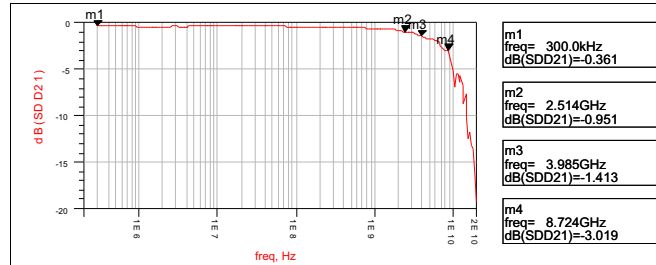


Figure 3. Differential Insertion Loss

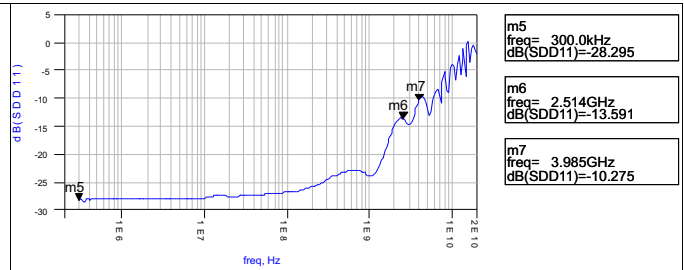


Figure 4. Differential Return Loss

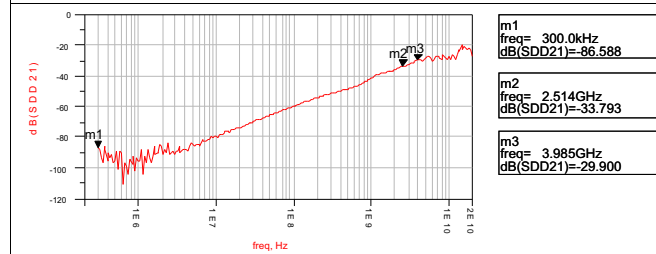


Figure 5. Differential Crosstalk

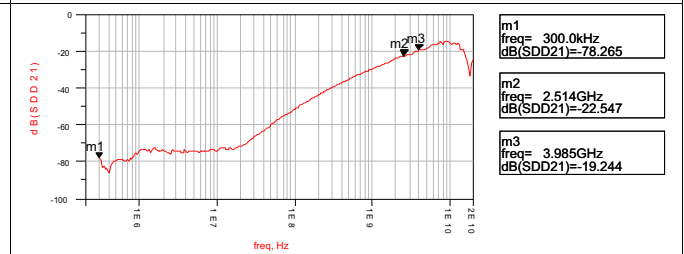


Figure 6. Differential Off Isolation

8 Parameter Measurement Information

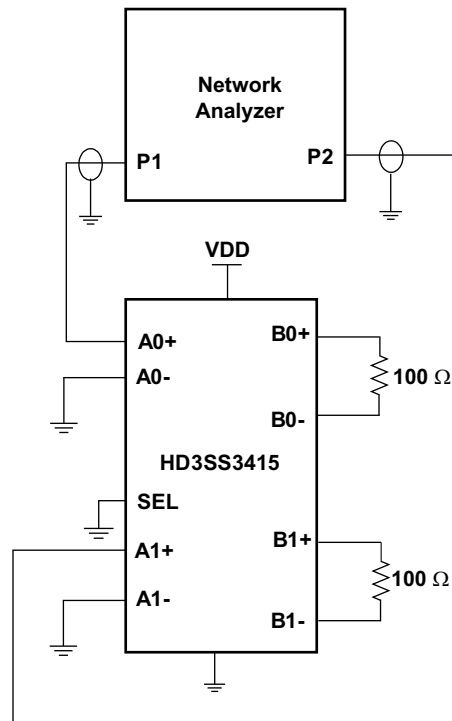


Figure 7. Cross Talk Measurement Setup

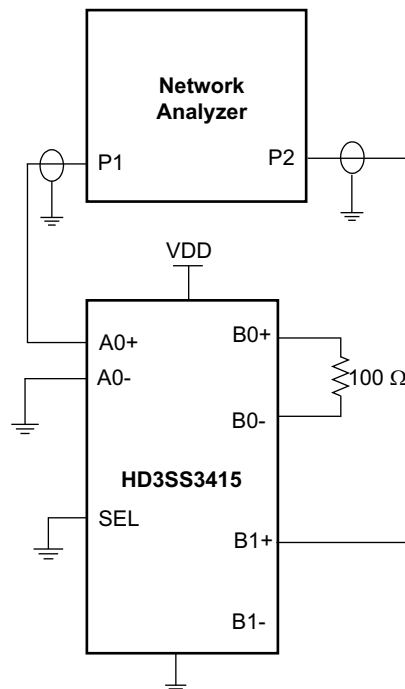


Figure 8. Off Isolation Measurement Setup

Parameter Measurement Information (continued)

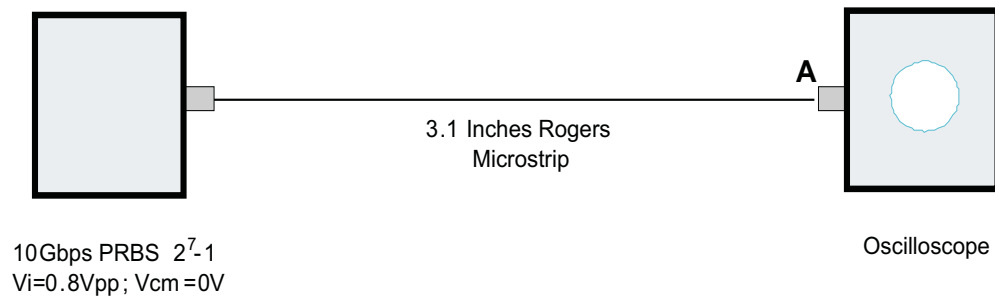


Figure 9. Source Eye Diagram Test Setup

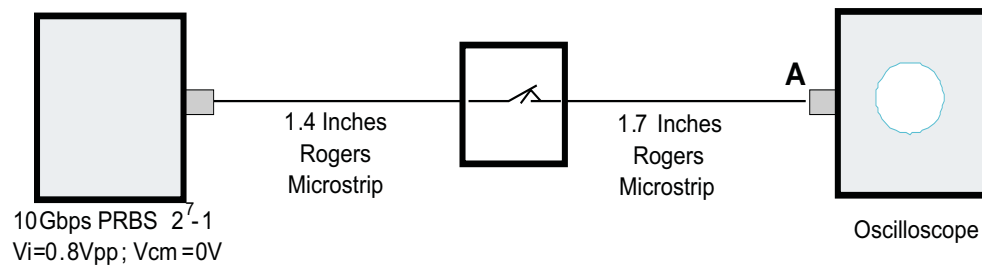


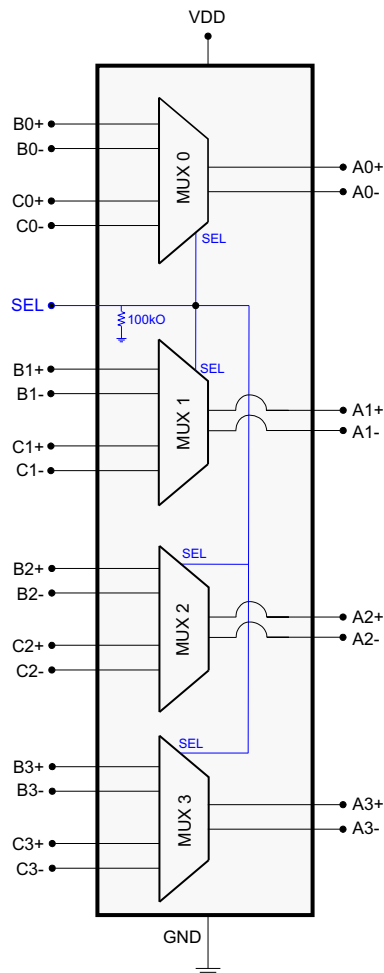
Figure 10. Output Eye Diagram Test Setup

9 Detailed Description

9.1 Overview

The HD3SS3415 is a high-speed passive switch offered in an industry standard 42-pin WQFN package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the full industrial temperature range of 0°C to 70°C. The HD3SS3415 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. Although it was designed specifically to address PCI Express Gen III applications, the HD3SS3415 will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2.0 V, as with USB 3.0 and DisplayPort 1.2.

9.2 Functional Block Diagram



9.3 Feature Description

The HD3SS3415 has a single control line (SEL Pin) which can be used to control the signal path between Port A and either Port B or Port C. The one select input (SEL) pin of the device can easily be controlled by an available GPIO pin within a system or from a microcontroller.

Table 1. MUX Pin Connections⁽¹⁾

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0+	B0+	C0+
A0–	B0–	C0–
A1+	B1+	C1+
A1–	B1–	C1–
A2+	B2+	C2+
A2–	B2–	C2–
A3+	B3+	C3+
A3–	B3–	C3–

(1) The HD3SS3415 can tolerate polarity inversions for all differential signals on Ports A, B and C. Care should be taken to ensure the same polarity is maintained on Port A vs. Port B/C.

9.4 Device Functional Modes

Table 2 lists the functional modes for the HD3SS3415.

Table 2. HD3SS3415 Control Logic

CONTROL PIN (SEL)	PORT A TO PORT B CONNECTION STATUS	PORT A TO PORT C CONNECTION STATUS
L (Default State)	Connected	Disconnected
H	Disconnected	Connected

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 AC Coupling Caps

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 μ F is best and the value should be match for the $\pm$ signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In [Figure 11](#), the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

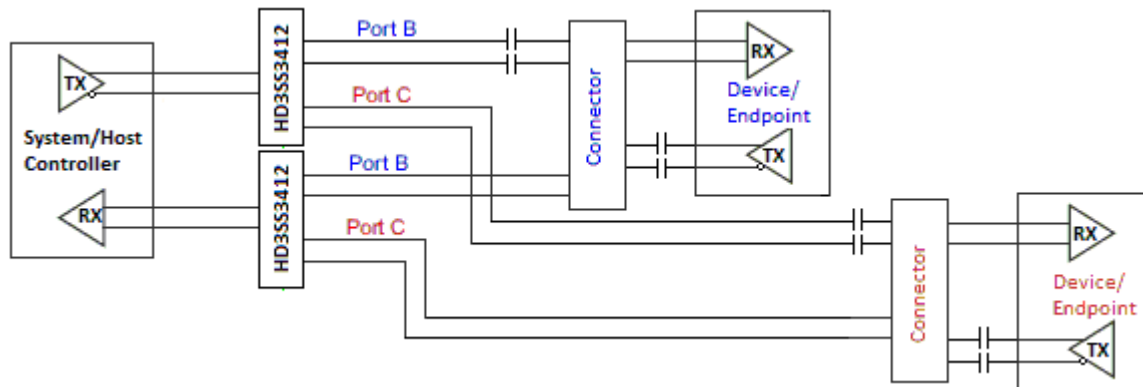


Figure 11. AC Coupling Capacitors Between Switch Tx and Endpoint Tx

In [Figure 12](#), the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

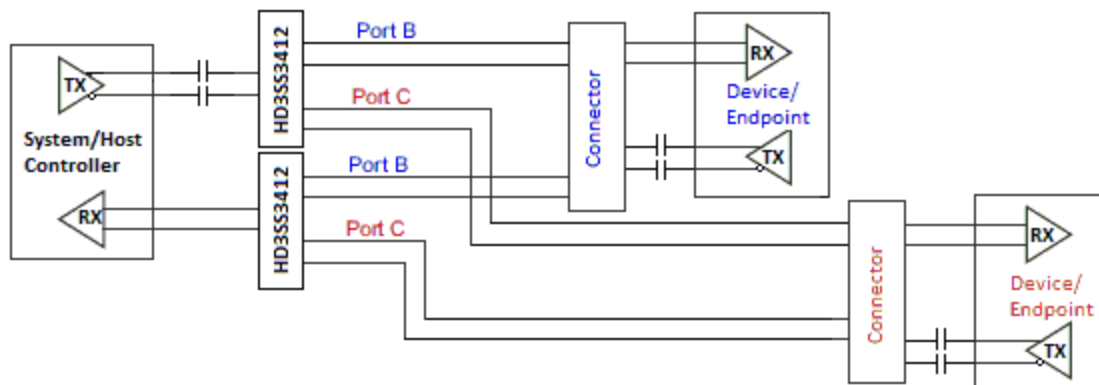


Figure 12. AC Coupling Capacitors on Host Tx and Endpoint Tx

Application Information (continued)

If the common-mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in Figure 13). A biasing voltage of less than 2 V is required in this case.

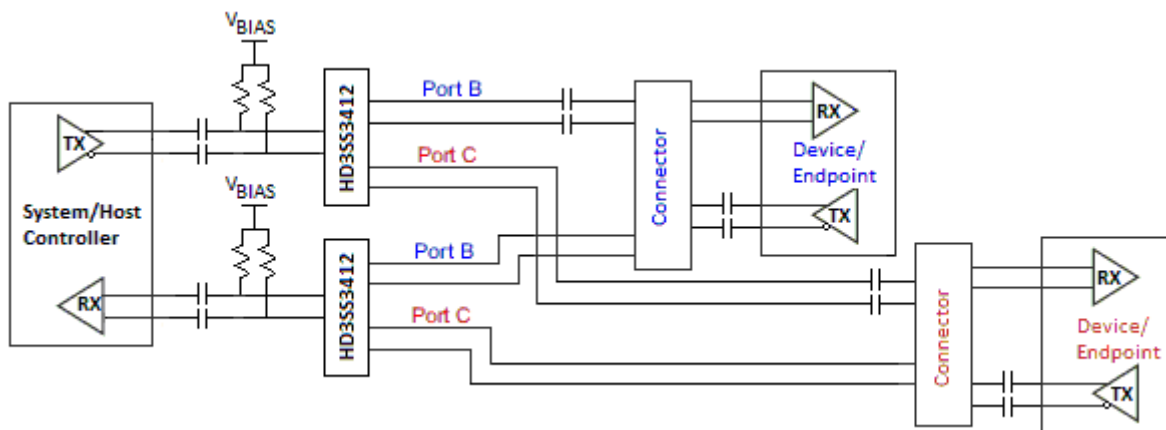


Figure 13. AC Coupling Capacitors on Both Sides of Switch

10.2 Typical Application

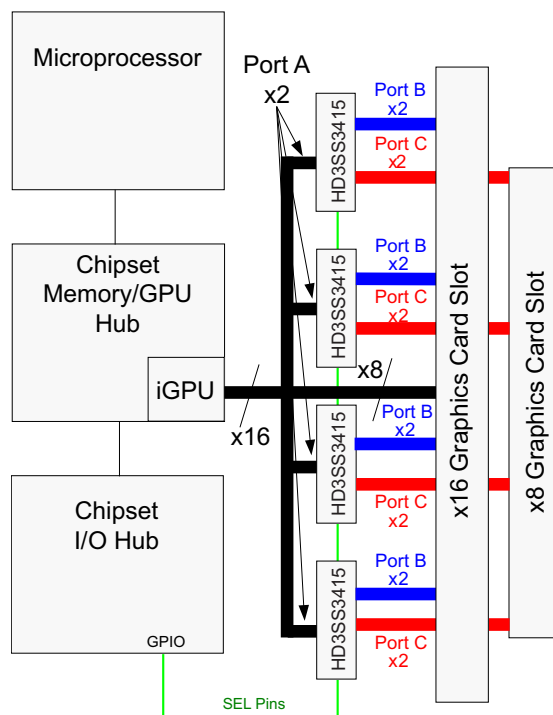


Figure 14. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

Table 3 lists the design parameters of this example.

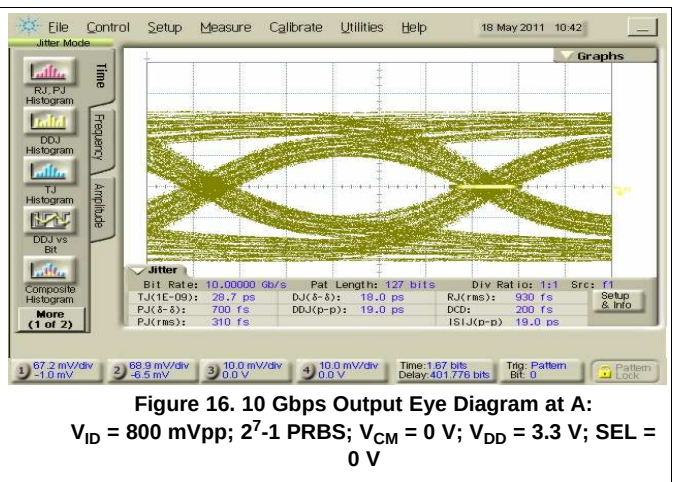
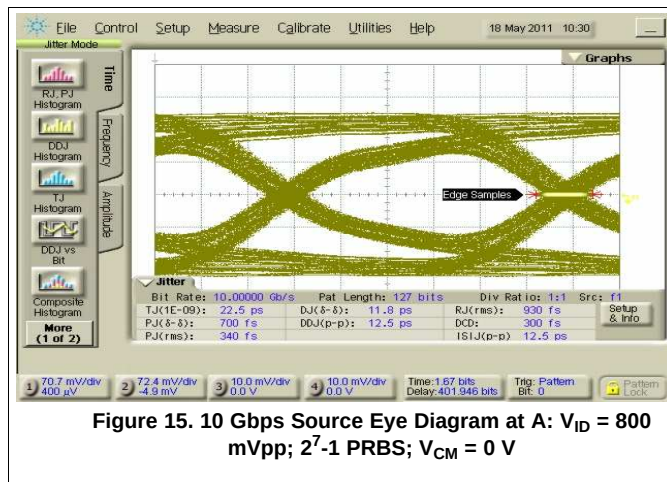
Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V
Decoupling capacitors	0.1 μ F
AC Capacitors	75 nF - 200 nF (100 nF shown) USBSS TX p and n lines require AC capacitors. Alternate mode signals may or may not require AC capacitors

10.2.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed circuit board, with a 0.1-uF bypass capacitor.
- Use +3.3-V TTL/CMOS logic level at SEL
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of <1800 mVpp and a common-mode voltage of <2 V

10.2.3 Application Curves



11 Power Supply Recommendations

The HD3SS3415 requires +3.3-V digital power sources. VDD 3.3 supply must have 0.1- μ F bypass capacitors to VSS (ground) for proper operation. TI recommends one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors such as 0.01- μ F are also recommended on the digital supply terminals.

12 Layout

12.1 Layout Guidelines

- Decoupling caps should be placed next to each power terminal on the HD3SS3415. Take care to minimize the stub length of the trace connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps.
- Place vias as close as possible to the decoupling cap solder pad.
- Widen VDD/GND planes to reduce effect of static and dynamic IR drop.
- The VBUS traces/planes must be wide enough to carry maximum of 2 A current

12.2 Layout Example

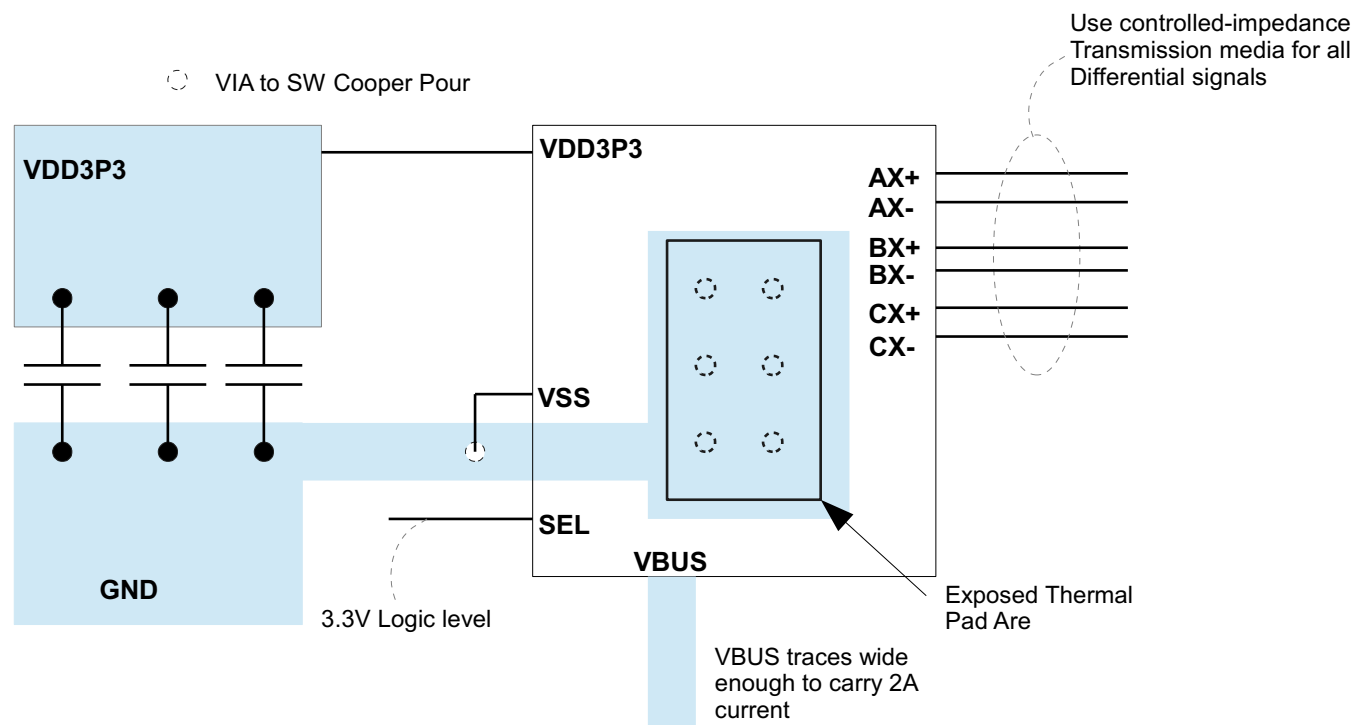


Figure 17. Layout Example

13 器件和文档支持

13.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

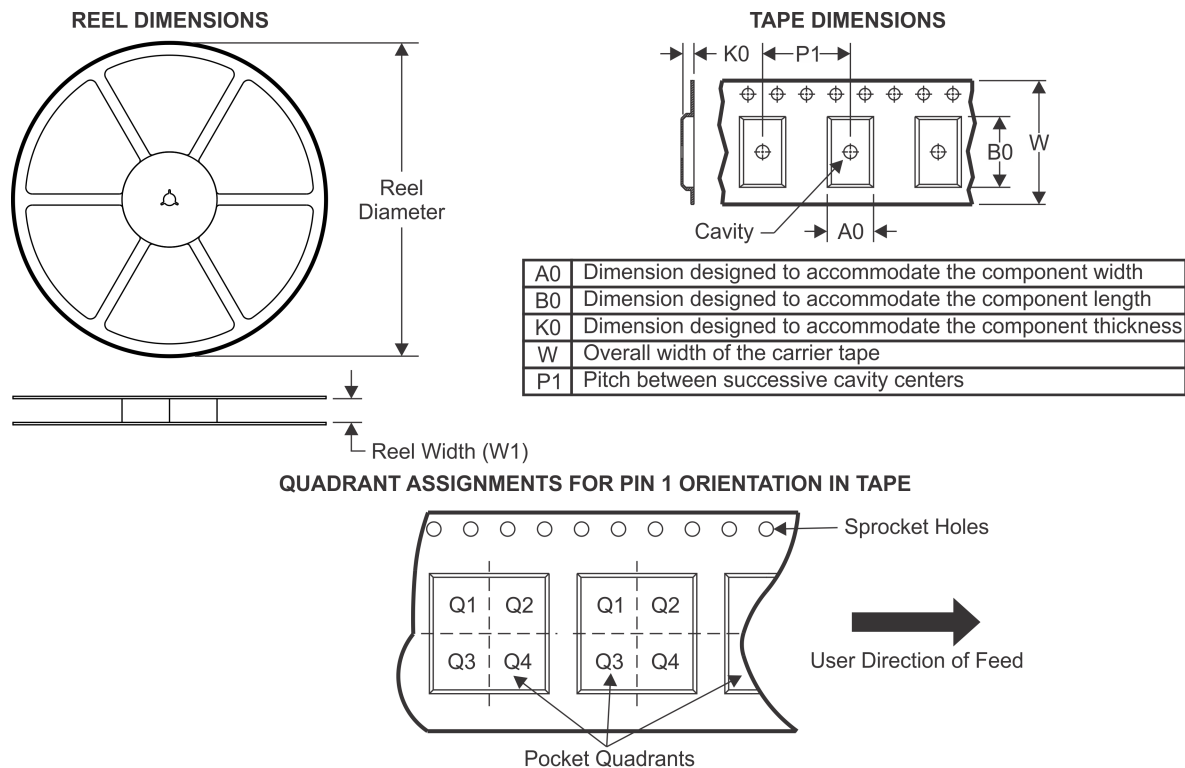
Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HD3SS3415RUAR	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3415
HD3SS3415RUAT	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3415

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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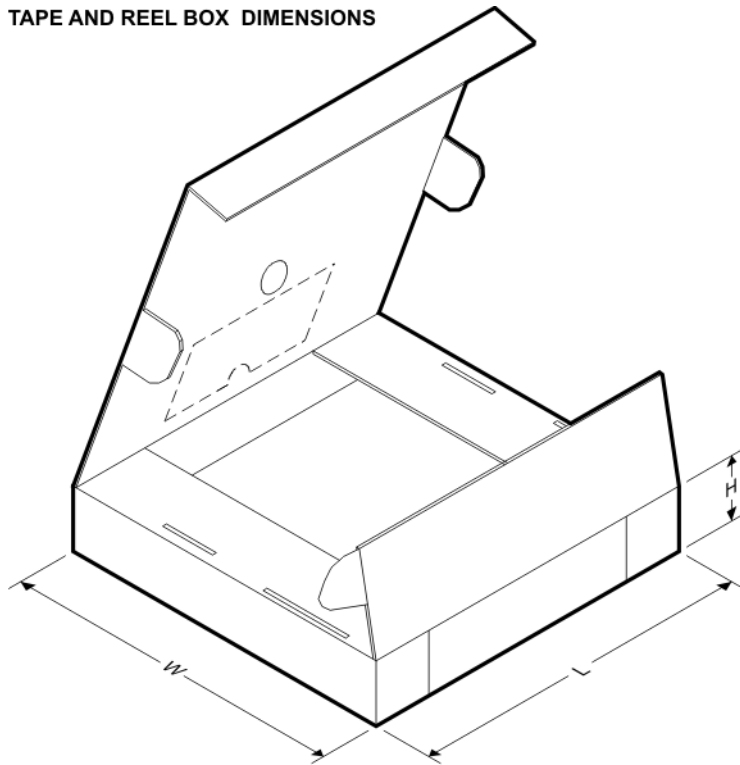
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3415RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
HD3SS3415RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3415RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0
HD3SS3415RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

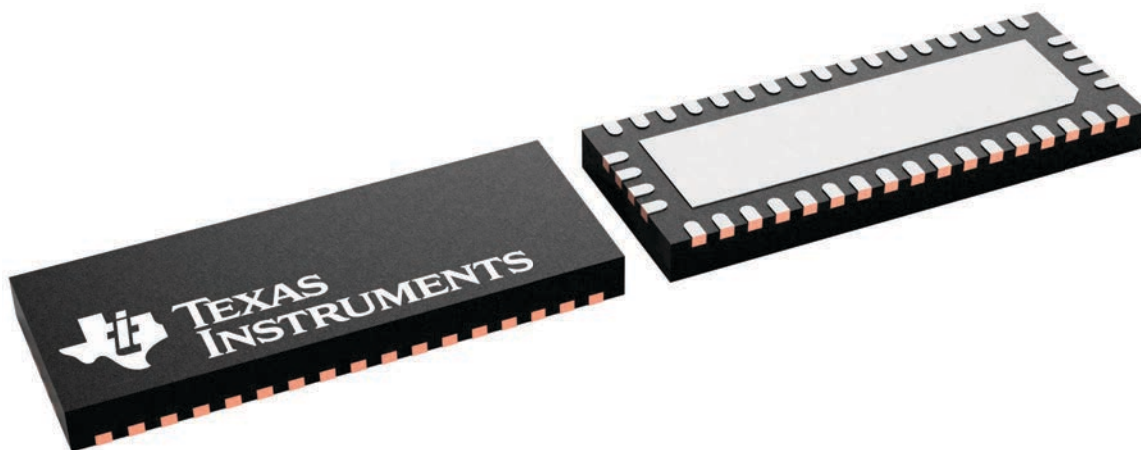
RUA 42

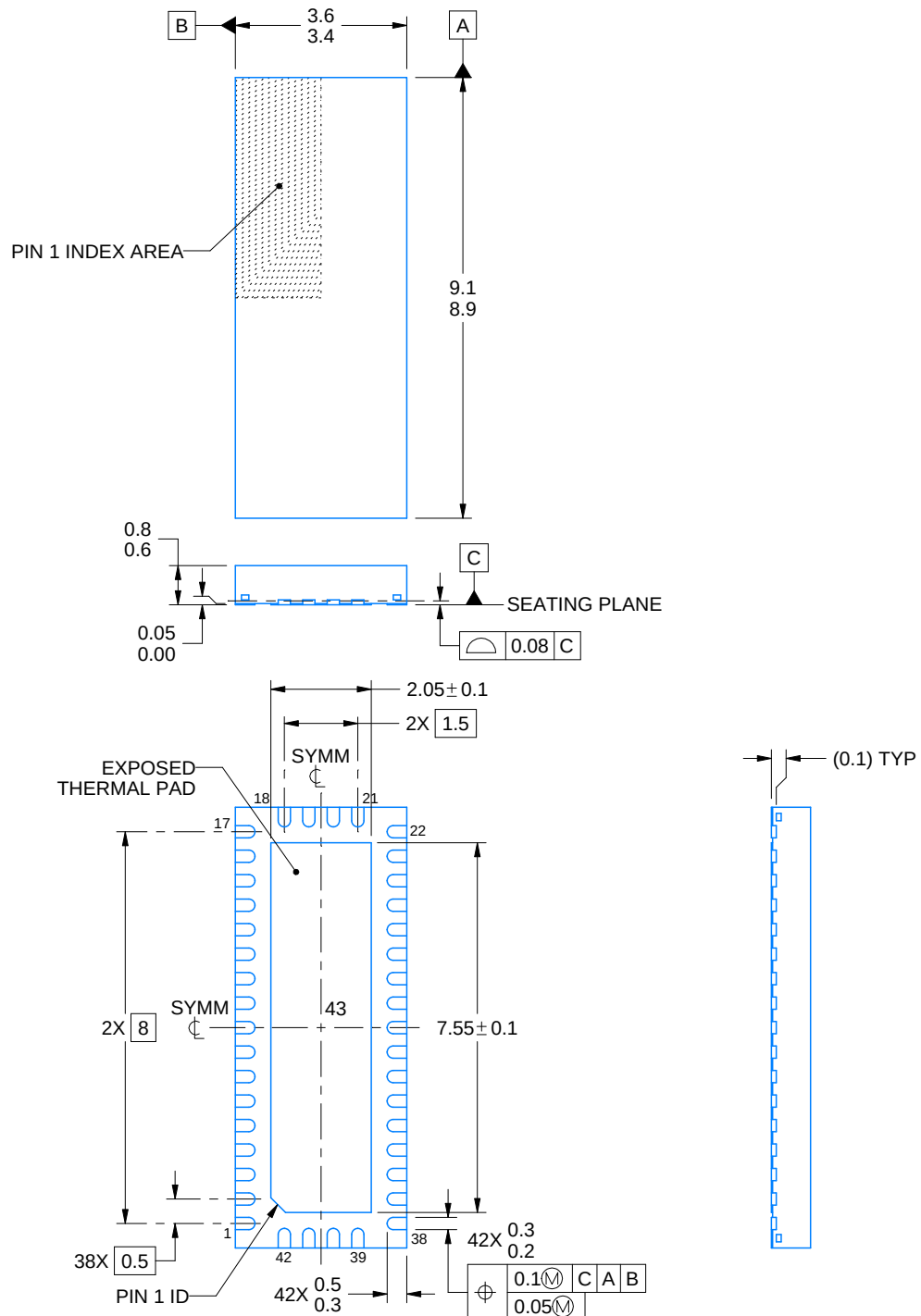
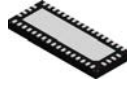
WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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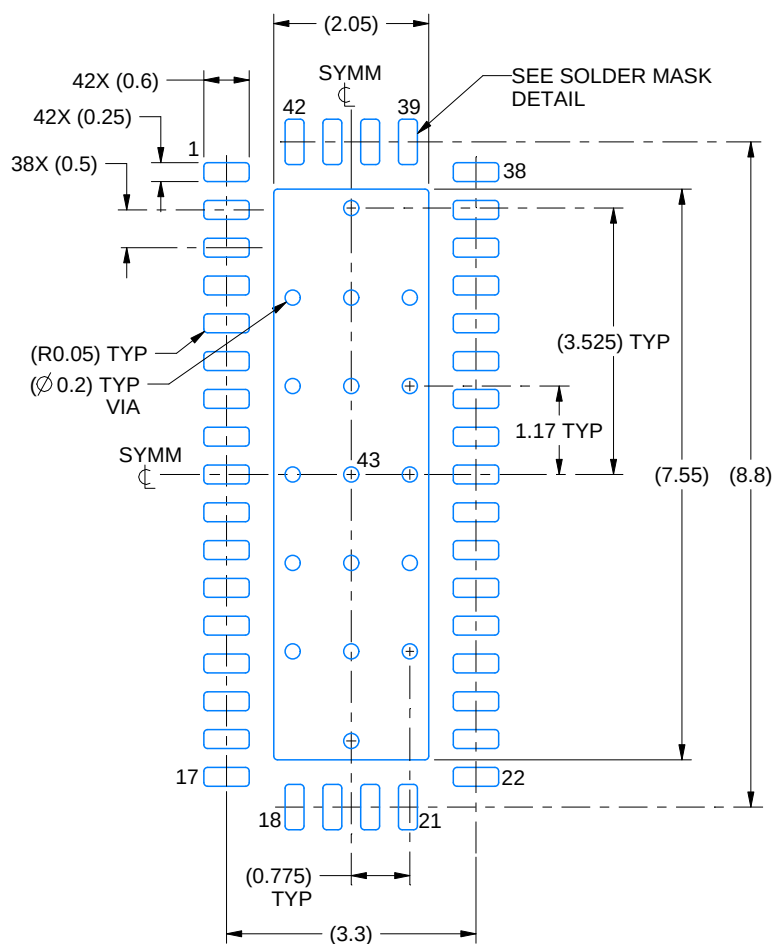
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

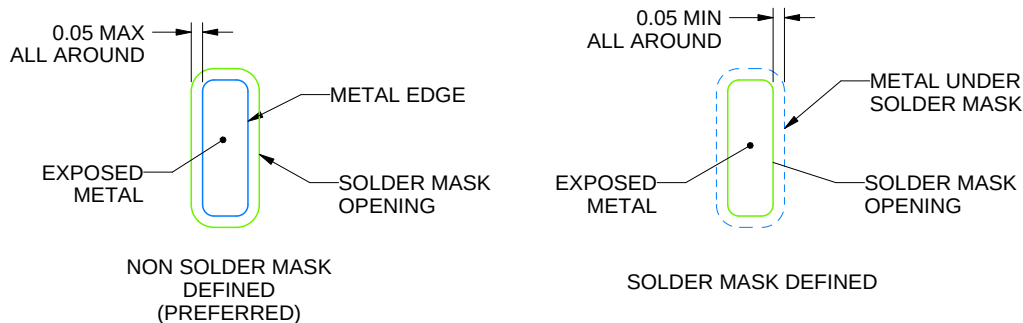
RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

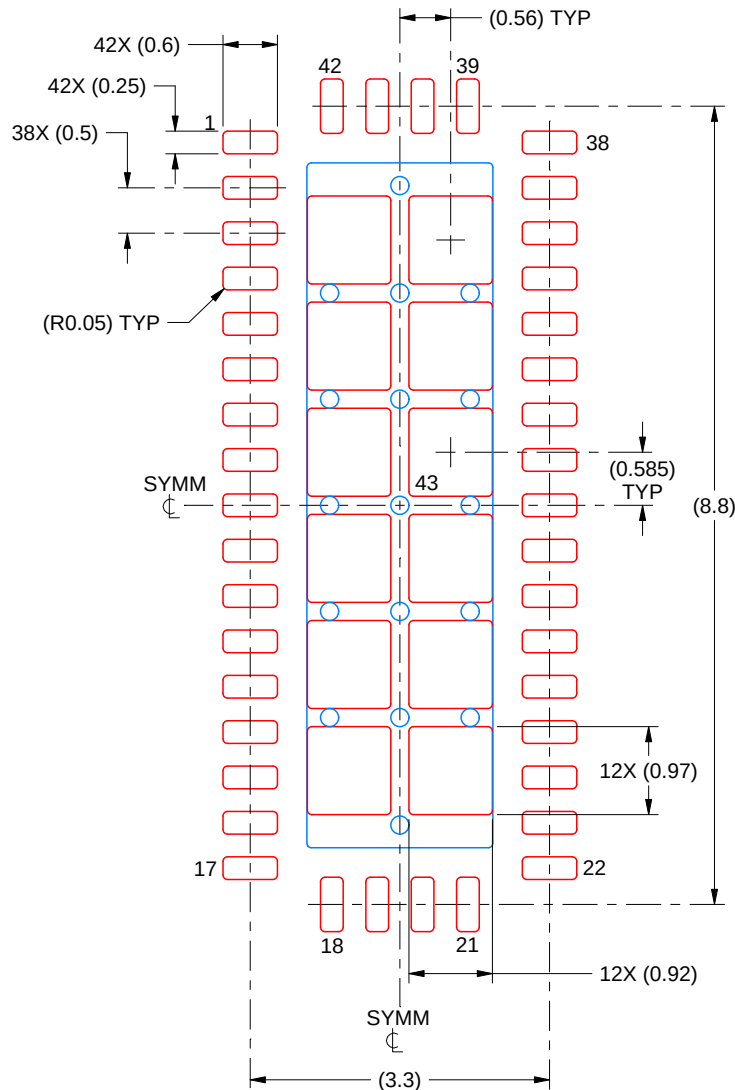
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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