1. DESCRIPTION

The XD/XL13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to- noise improvement referenced to 0.5 percent THD. Con-trolled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

2. FEATURES

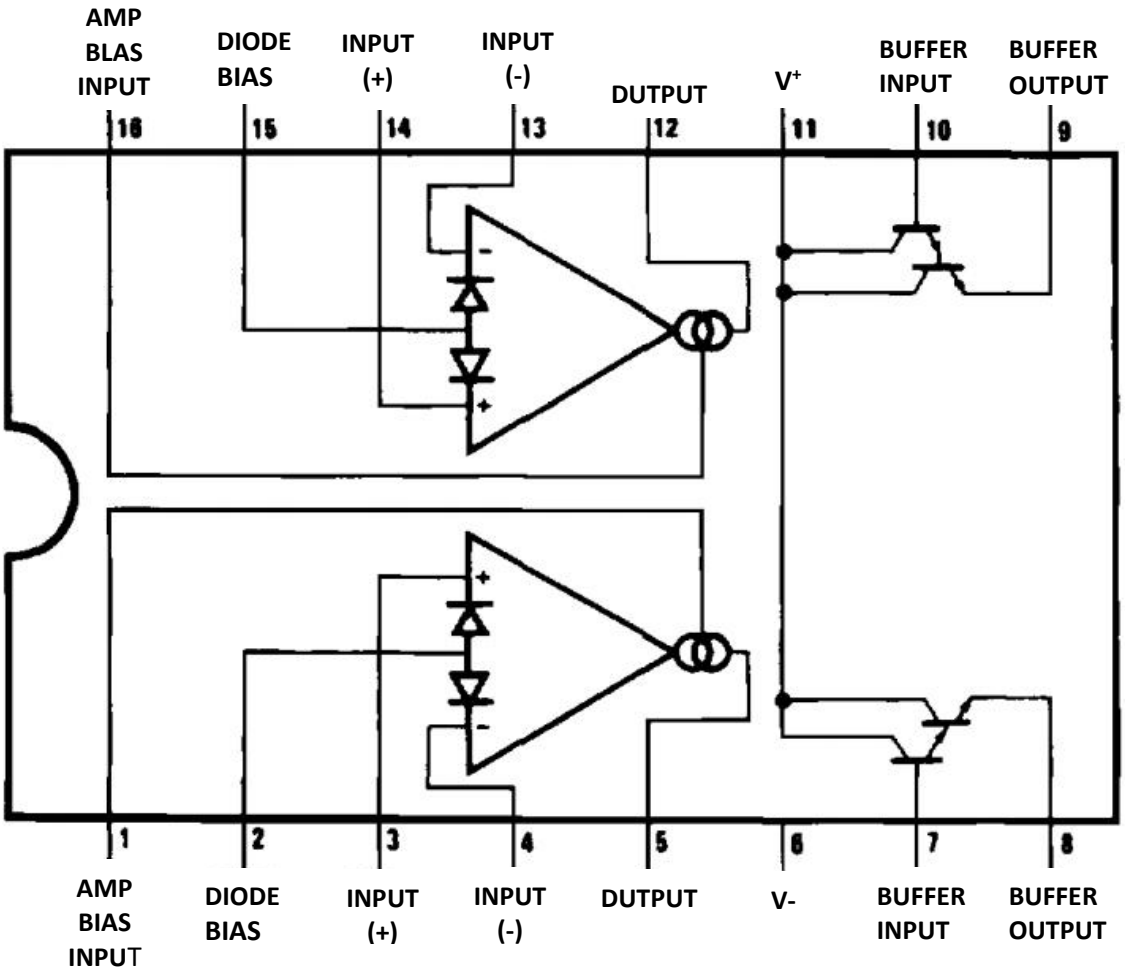
- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio

3. APPLICATIONS

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

4. CONNECTION DIAGRAM

Dual-In-Line and Small Outine Packages



5. ABSOLUTE MAXIMUM RATINGS

- Supply Voltage (Note 1)

  XD/XL13600.....36VDc or ±18V
- Power Dissipation (Note2) TA=25C.....570 mW
- Differential Input Voltage.....±5V
- Diode Bias Current (Ip).....2 mA
- Amplifier Bias Current (IABC).....2 mA
- Output Short Circuit Duration.....Continuous
- Buffer Output Current (Note 3).....20mA
- Operating Temperature Range..... -40°Cto+85°C
- DC Input Voltage.....+Vsto-Vs
- Storage Temperature Range.....-65°C to + 150°C
- Soldering Information

  Dual-In-Line Package

  Soldering (10 seconds).....260°C
- Small Outline Package

  Vapor Phase(60 seconds).....215°C

  Infrared (15 seconds).....220°C

6. ELECTRICAI CHARACTERISTICS(Note 4)

Parameter	Condltions	XL/XD13600			Unlts
		Min	Typ	Max	
Input Offset Voltage (V_{OS})	Over Specified Temperature Range		0.4	4	mV
					mV
	I_{ABC}=5 μA		0.3	4	mV
Vos Including Diodes	Diode Bias Current (I_D) = 500μA		0.5	5	mV
Input Offset Change	5 μA≤ I_{ABC}≤ 500μA		0.1	3	mV
Input Offset Current			0.1	0.6	μA
Input Bias Current			0.4	5	μA
	Over Specified Temperature Range		1	8	μA
Forward Transconductance (gm)					
		6700	9600	13000	μmho
	Over Specified Temperature Range	5400			μmho
gm Tracking			0.3		dB
Peak Output Current	R_L=0, I_{ABC}=5 μA		5		μA
	R_L=0, I_{ABC}=500μA	350	500	650	μA
	R_L=0, Over Specified Temp Range	300			μA
Peak Output Voltage					
Positive	RL= ∞, 5 μA≤ I_{ABC} ≤500μA	+12	+14.2		V
Negative	RL= ∞, 5 μA≤ I_{ABC} ≤500μA	-12	-14.4		V
Supply Current	I_{ABC} =500 μA, Both Channels		2.6		mA
V_{OS} Sensitivity					
Positive	△Vos/△V+		20	150	μV/V
Negative	△ Vos/△V-		20	150	μV/V
CMRR		80	110		dB
Common Mode Range		±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz		100		dB
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)		0.2	100	nA
Input Resistance		10	26		
Open Loop Bandwidth			2		
Slew Rate	Unity Gain Compensated		50		
Butfer Input Current	(Note 5), Except I_{ABC}= 0 μA		0.2		
Peak Buffer Output Voitage	(Note 5)	10			

Note 1: For selections to a supply voitage above ±22V, contact factory.

Note 2: For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.

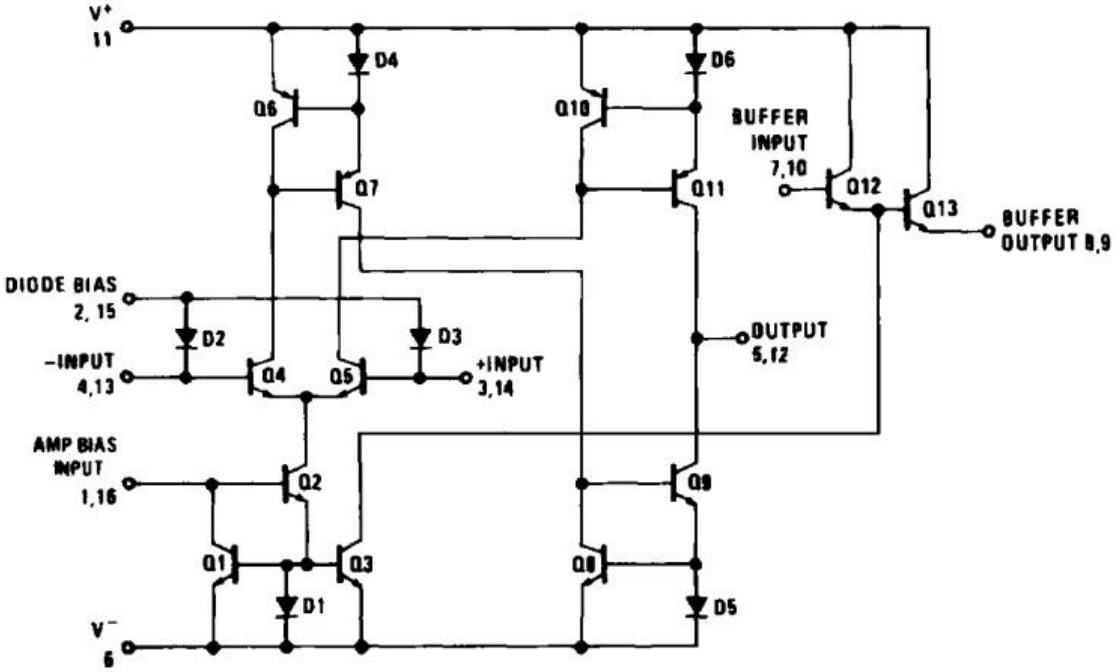
Note 3: Buffer output current should be limited so as to not exceed package dissipation.

Note 4: These specifications apply tor Vs= ±15V, T_A= 25°C, amplifier bias current (I_{ABC})= 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

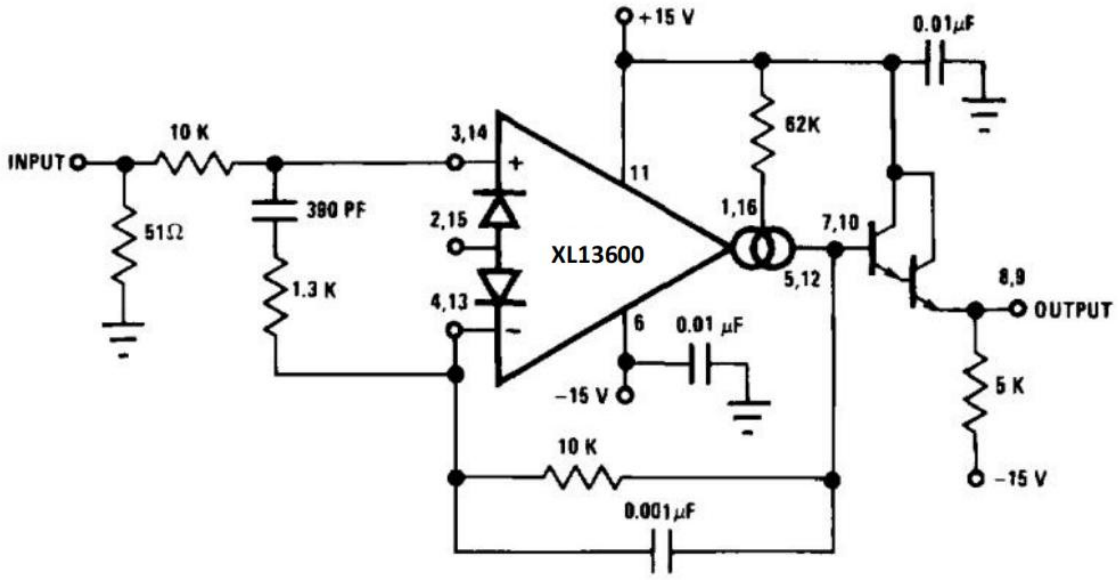
Note 5: These specifications apply for Vs=±15V,I_{ABC} = 500μA.R_{OUT} = 5 kΩ connected from the buffer output to -Vs and the input of the butfer is connected to the transconduciance amplitier output.

7. SCHEMATIC DIAGRAM

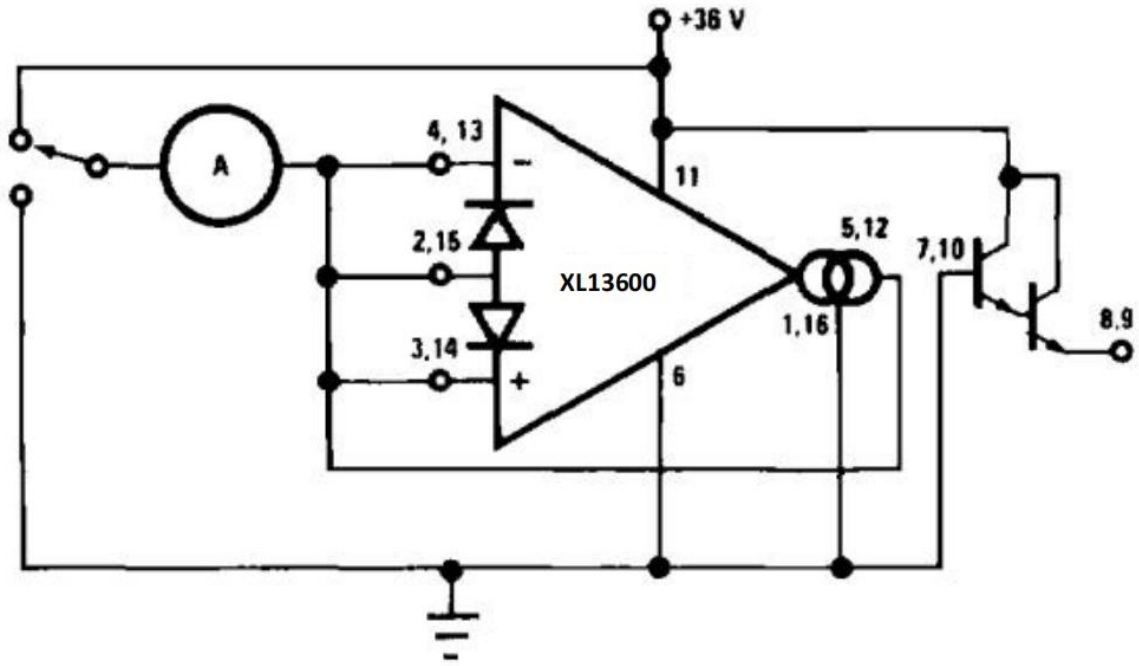
One Operational Transconductance Amplifier



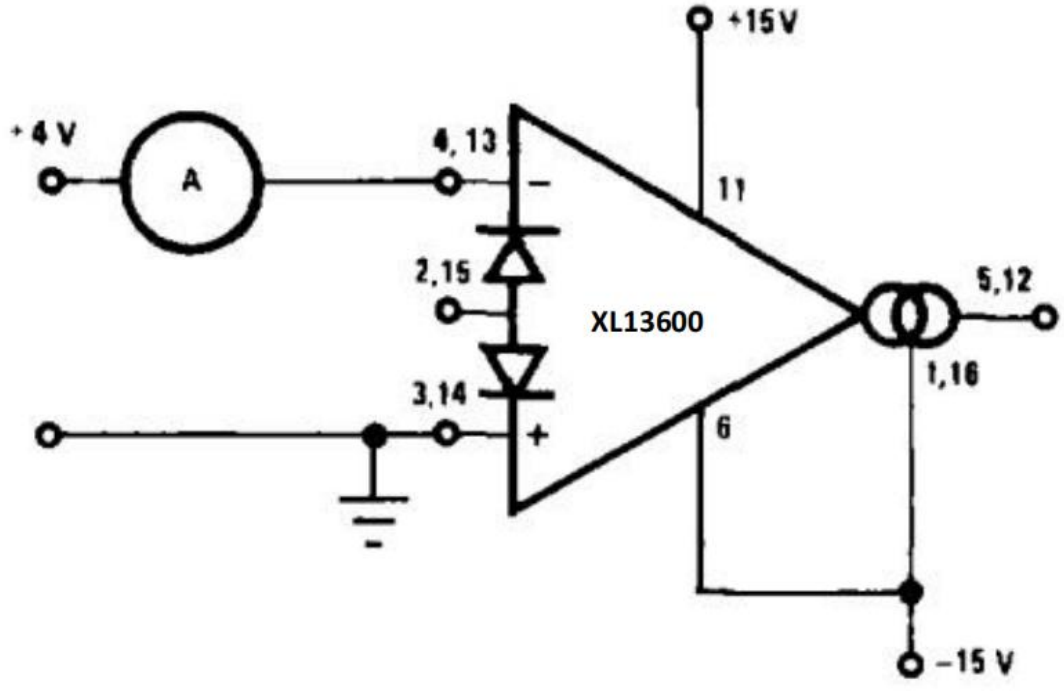
8. TYPICAL PERFORMANCE CHARACTERISTICS



Unity Gain Follower



Leakage Current Test Circuit



Differential Input Current Test Circuit

9. CIRCUIT DESCRIPTION

The differential transistor pair Q_4 and Q_5 form a transcon.ductance stage in that the ratio of their collector currents is defined by the differential input voltage according to thetransfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where V_{IN} is the differential input voltage, kT/q is approxi mately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \qquad (2)$$

where lABc is the amplifier bias current applied to the gainpin.
For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the In function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_5 - I_4 \qquad (4)$$

Collector currents I_4 and I_5 are not very useful by them selves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

10. LINEARIZING DIODES

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current Is. Since the sum of I4 and I5 is IABc and the difference is IoUT, currents I4 and I5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and tempera tures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_{ABC}}{I_D} \right) \quad \text{for } |I_S| < \frac{I_D}{2} \qquad (6)$$

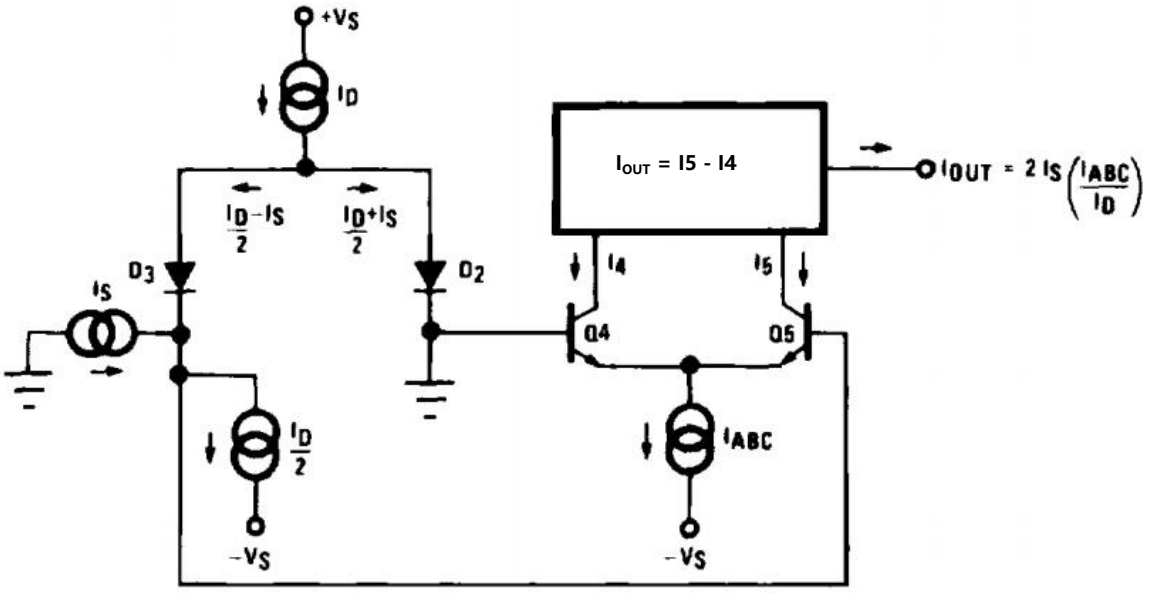


FIGURE 1. LInearizing Diodes

LINEARIZING DIODES (Continued)

Notice that in deriving Equation 6 no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

11. CONTROLLED IMPEDANCE BUFFERS

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC}, a buffer which has very low input bias current is desirable. An FETfoilower satisfies the low input current requirement, but is somewhat non-linear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC}, the buffer's input current is minimal. At higher levels of I_{ABC},transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate. When lABc is changed, the DC level of the Darlington output buffer will shift. In audio applica. tions where I_{ABC} is changed suddenly, this shift may produce an audible "pop". For these applications the XL/XD13600may produce superior results.

12. APPLICATIONS-VOITAGE CONTROLLED AMPLIFIERS

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs.Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting RL. Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, lp should be as large as possible. This minimizes the dynamic junction resistance of the diodes (re) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for Ip unless the specific application demands otherwise.

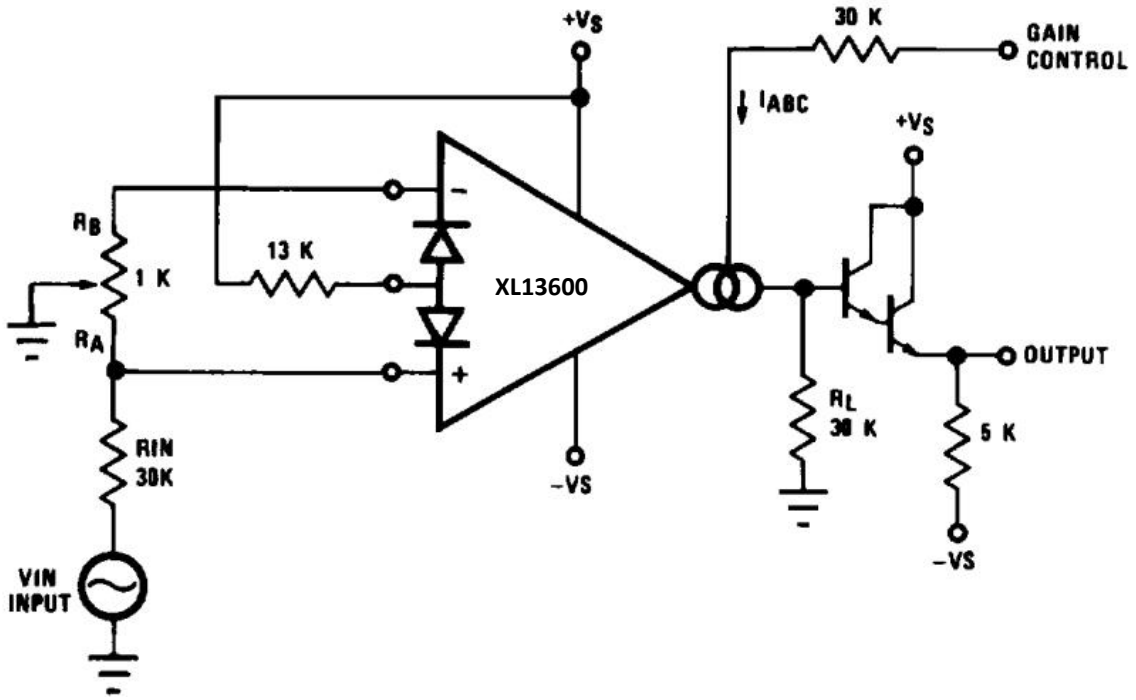


FIGURE 2. Voltage Controlled Amplifier

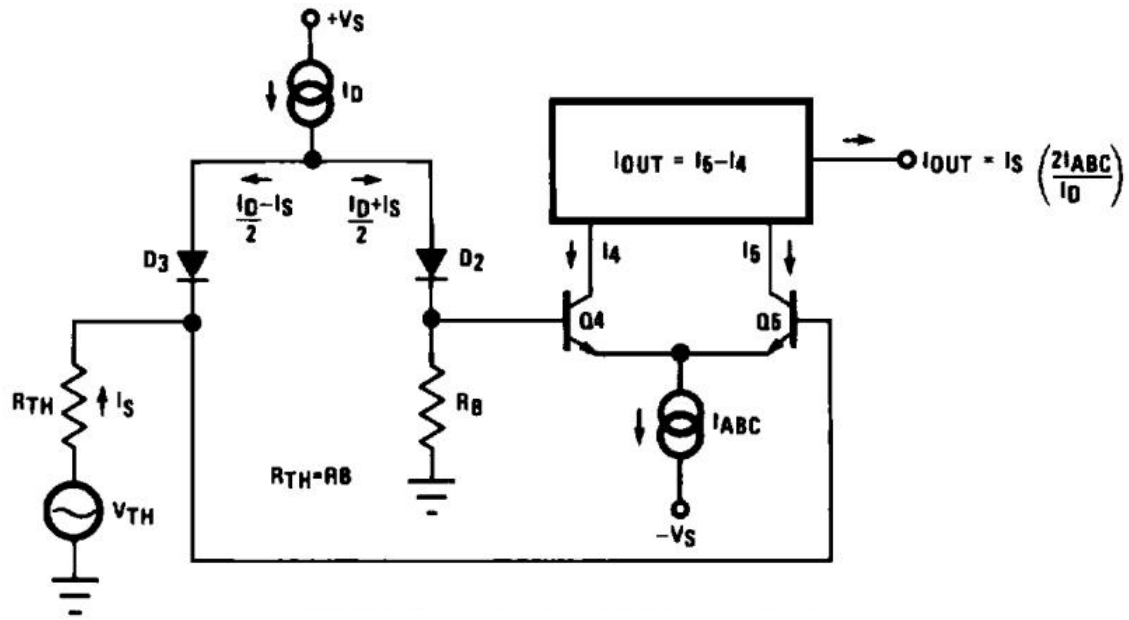


FIGURE 3. Equlvalent VCA Input Circuit

13. STEREO VOLUME CONTROL

The circuit of Figure 4 uses the excellent matching of the two XL/XD13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. Rp is provided to minimize the output offset voltage and may be replaced with two 510nresistors in AC-coupled applications. For the component values given, amplifier gain is derived for Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5,where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$

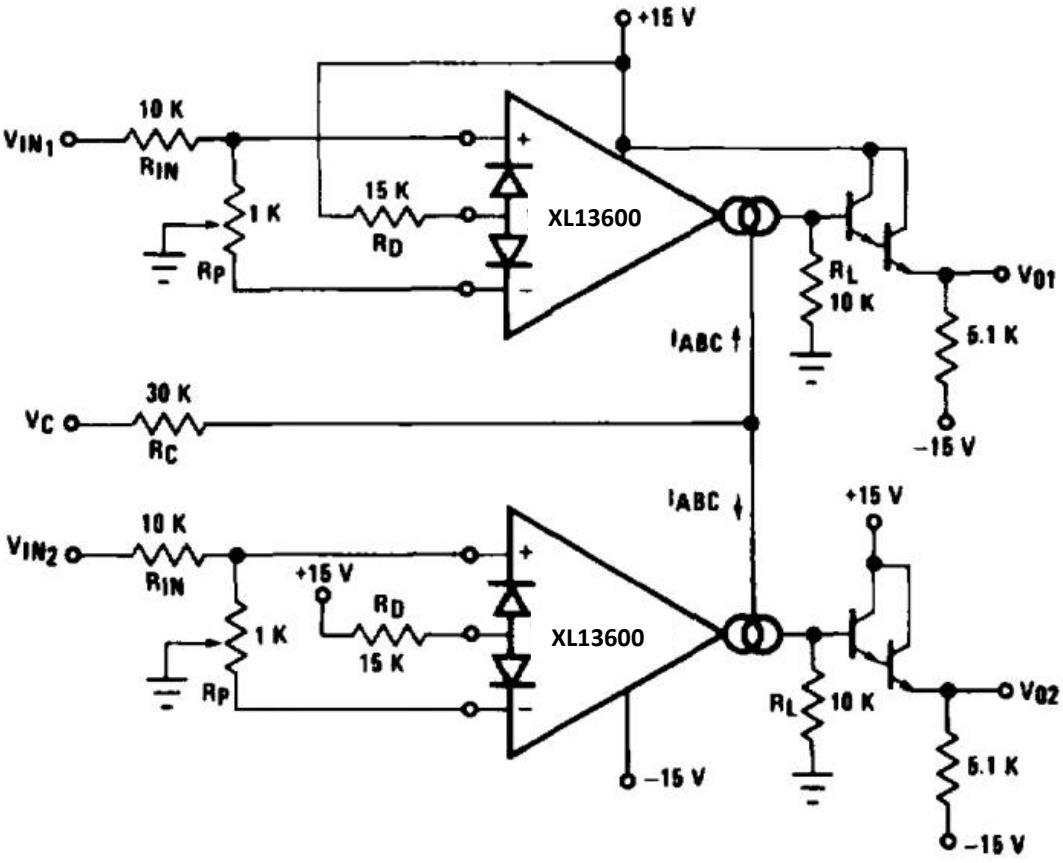


FIGURE 4. Stereo Volume Control

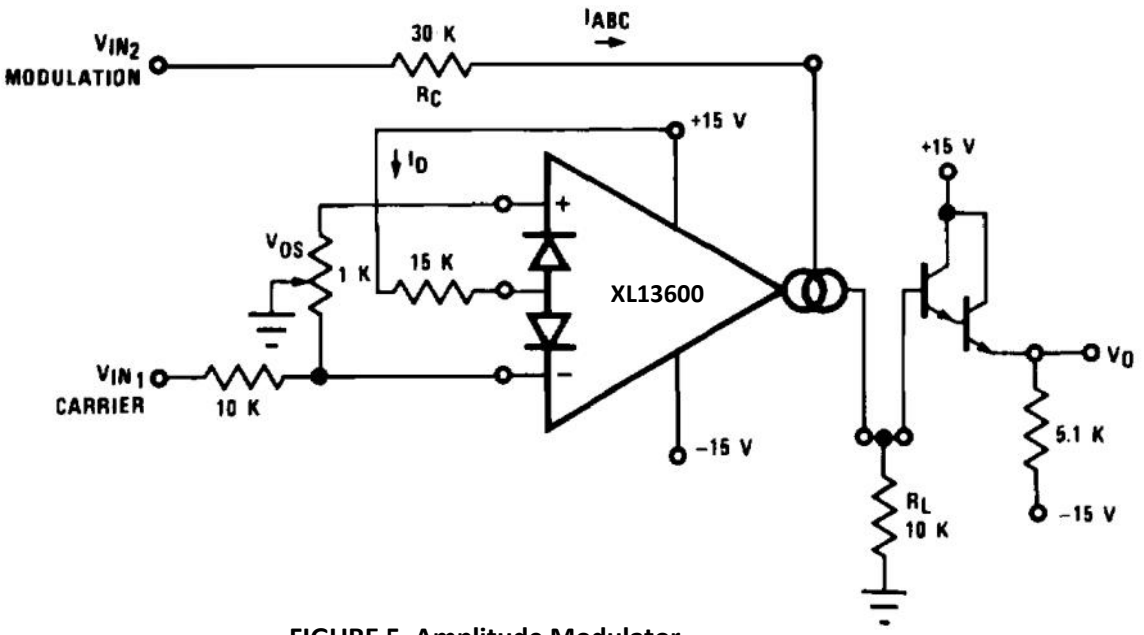


FIGURE 5. Amplitude Modulator

The constant term in the above equation may be cancelled by feeding Is x IpRc/2 (V^- + 1.4V) into Io. The circuit of Figure 6 adds RM to provide this current, resulting in a four. quadrant multiplier where Rc is trimmed such that Vo= 0V for V_{IN2} = 0V. R_M also serves as the load resistor for Io.

Noting that the gain of the XL/XD13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, Figure 7 shows an AGC Amplifier using this approach. As Vo reaches a high enough amplitude (3 V_{BE}) to turn on the Darlington transistors and the linearizing diodes, the increase in Ip reduces the amplifier gain so as to hold Vo at that level.

14. VOLTAGE CONTROLLED RESISTORS

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8.A signal voltage applied at R_X generates a V_{IN} to the XL/XD13600 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where g_m ≈19.2 I_{ABC} at 25°C. Note that the attenuation of Vo by R and Ra is necessary to maintain V_{IN} within the linear range of the XL/XD13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voitage range of the XL/XD13600.

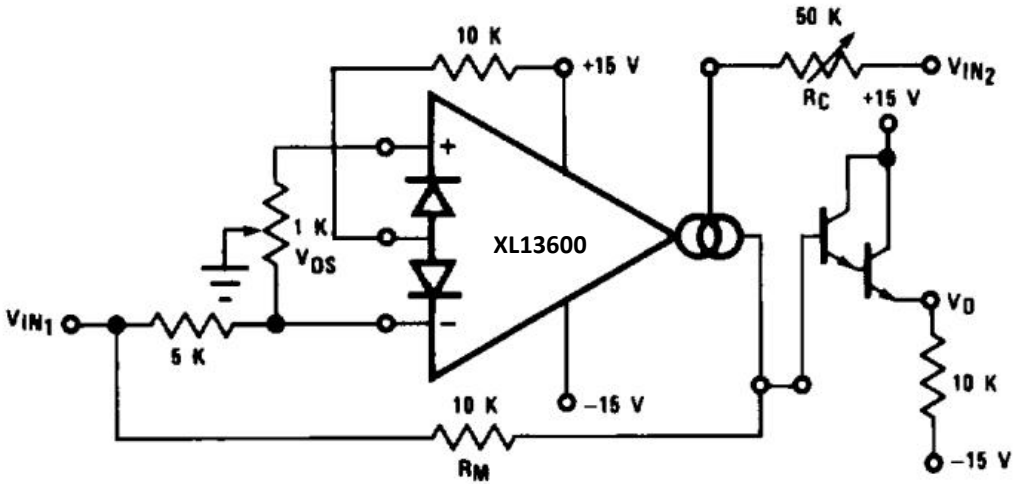


FIGURE 6. Four-Quadrant Multiplier

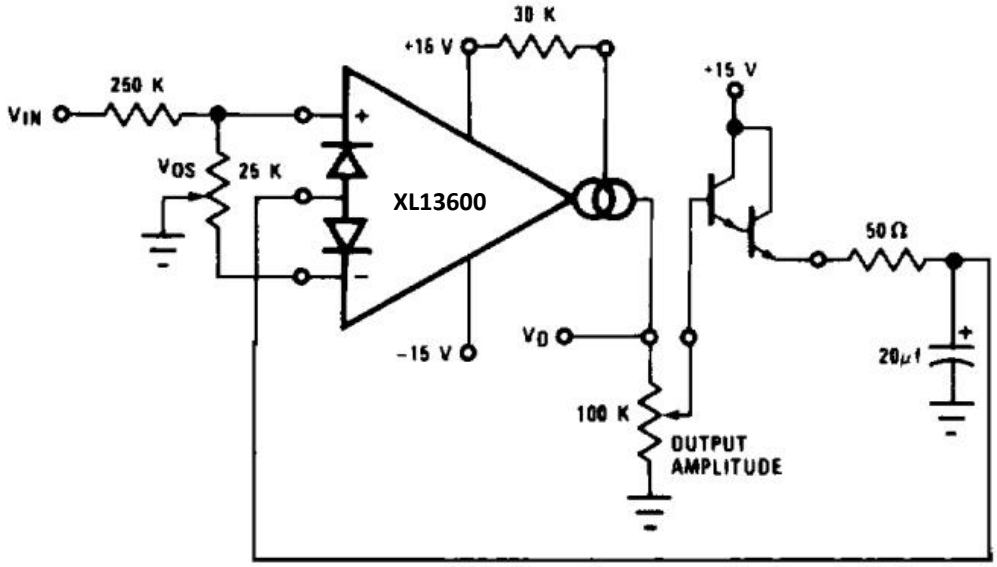


FIGURE 7. AGC Amplifier

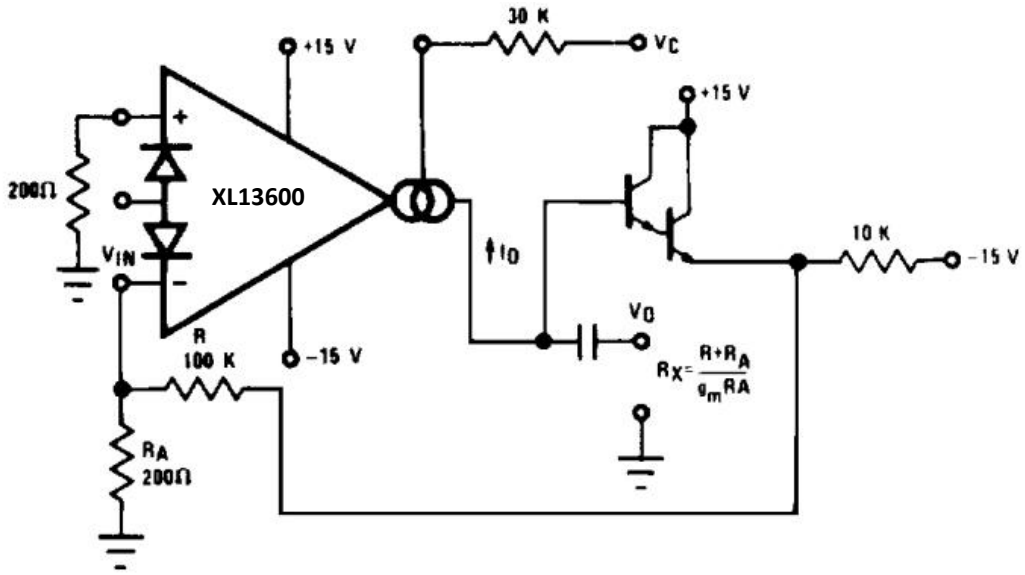


FIGURE 8. Voltage Controlled Resistor, Single-Ended

15. VOLTAGE CONTREOLLED FILTERS

OTA's are extremely useful for implementing voltage controlled filters, with the XL/XD13600 having the advantage that the required buffers are included on the I.C. The VC Lo Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cutoff, with the cut-off frequency being the point at which Xc/9m equals the closedloop gain of (R/RA) At frequencies above cut-off the circuit provides a single RC rotl-off (6 dB per octave) of the input signal ampltude with a -3 dB point defined by the given equation,where gm is again 19.2 × I_{ABC} at room temperature. Figure12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14.Due to the excellent gm tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

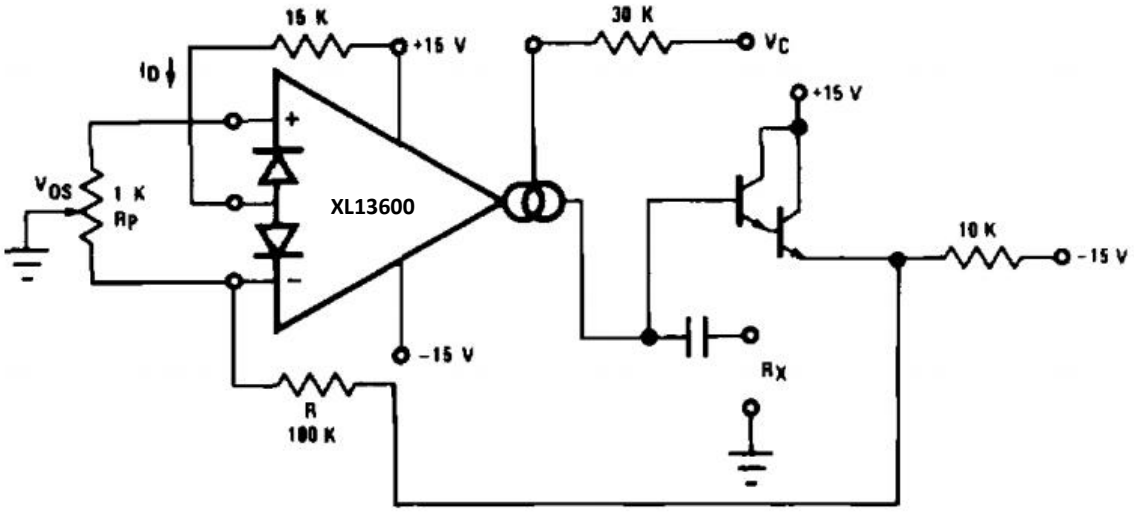


FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

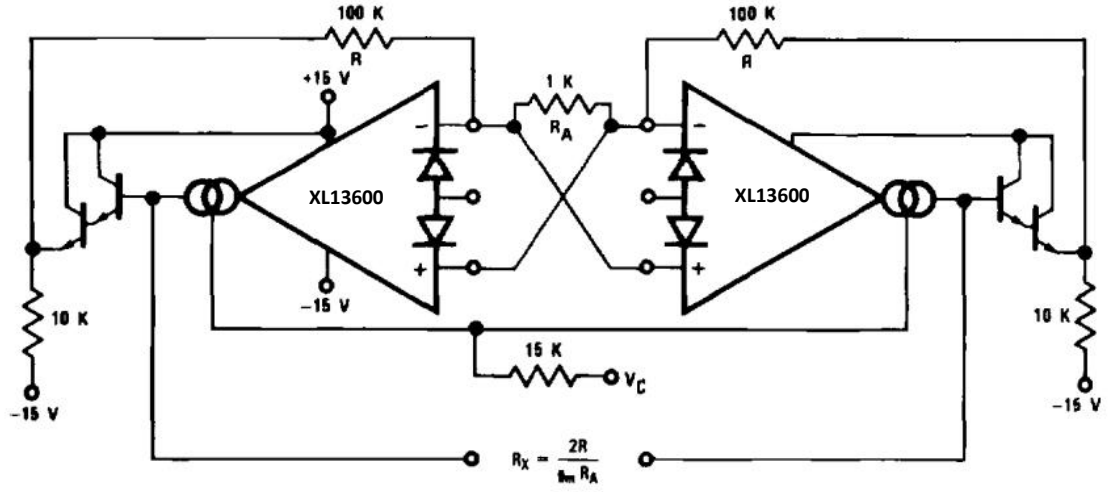


FIGURE 10. Floating Voltage Controlled Resistor

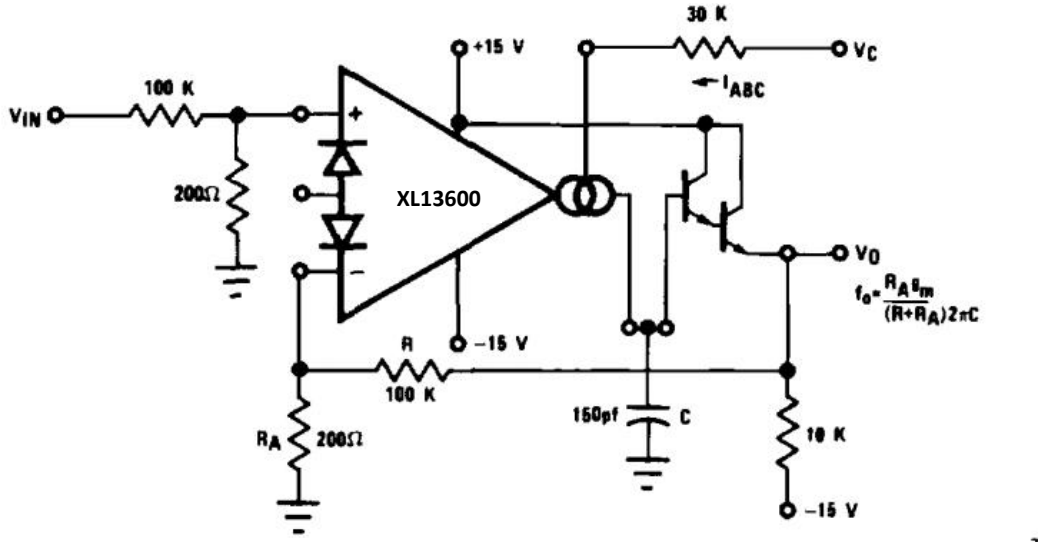


FIGURE 11. Voltage Controiled Low-Pass Fllter

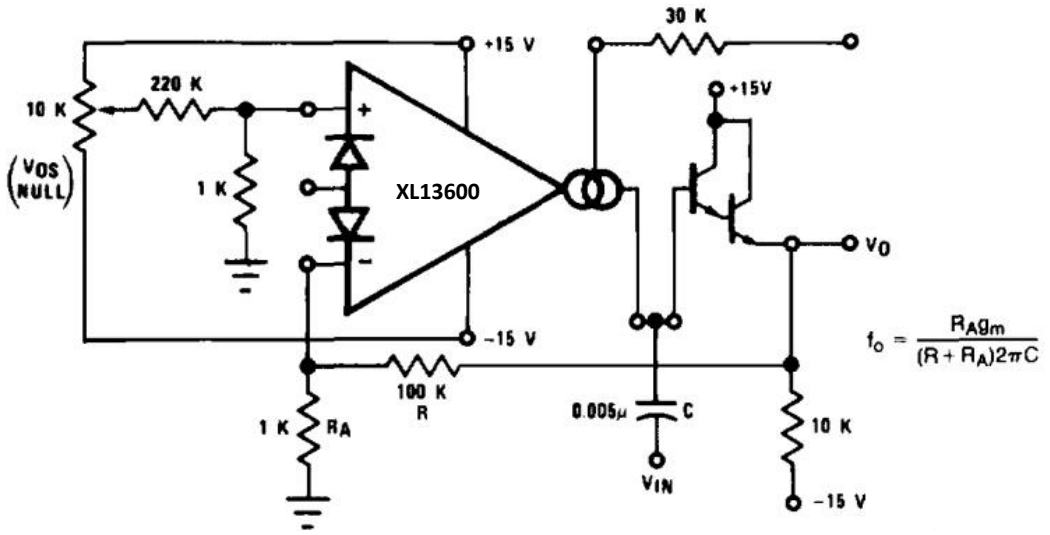


FIGURE 12. Voltage Controlled Hi-Pass Fliter

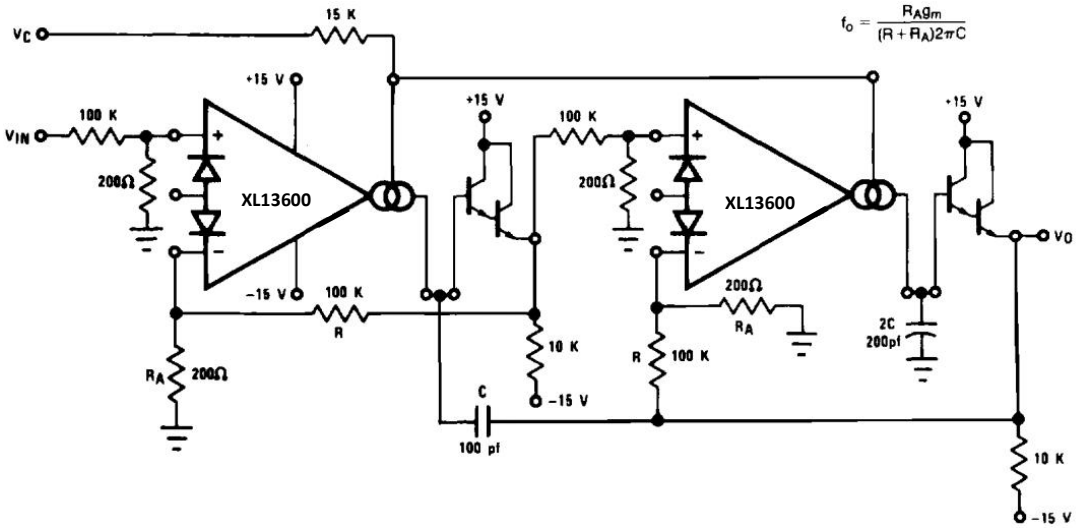


FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Fllter

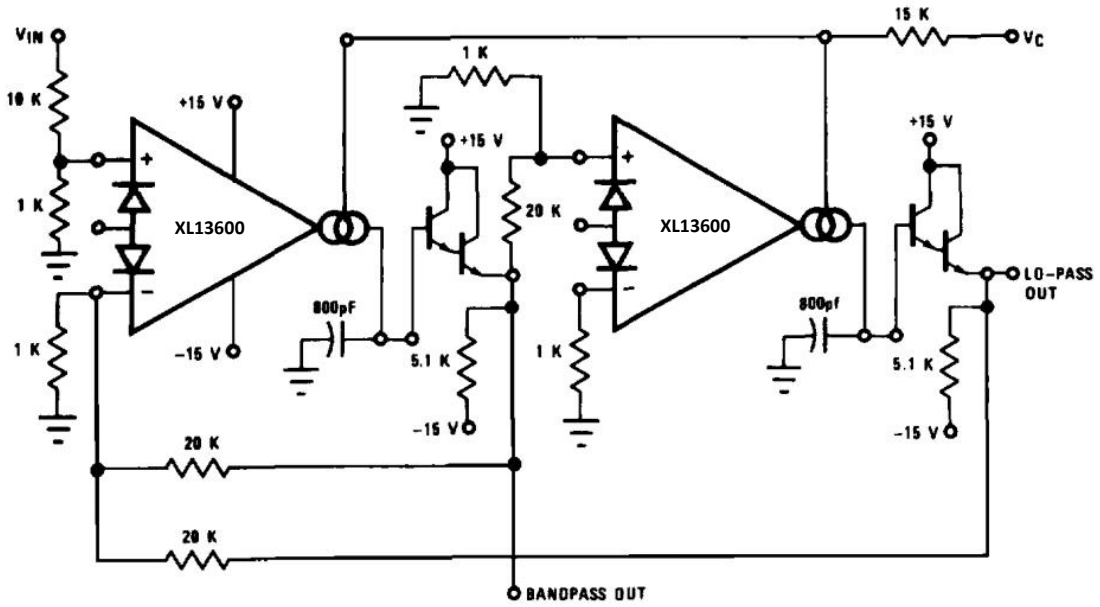


FIGURE 14. Voltage Controlled State Variable Filter

16. VOLTAGE CONTROLLED OSCILLATORS

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the XL/XD13600.With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as Ic is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differen-tial input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C.When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two XL/XD13600 packages, with three of the amplifiers

configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360°or 180°for the inverter and 60°per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

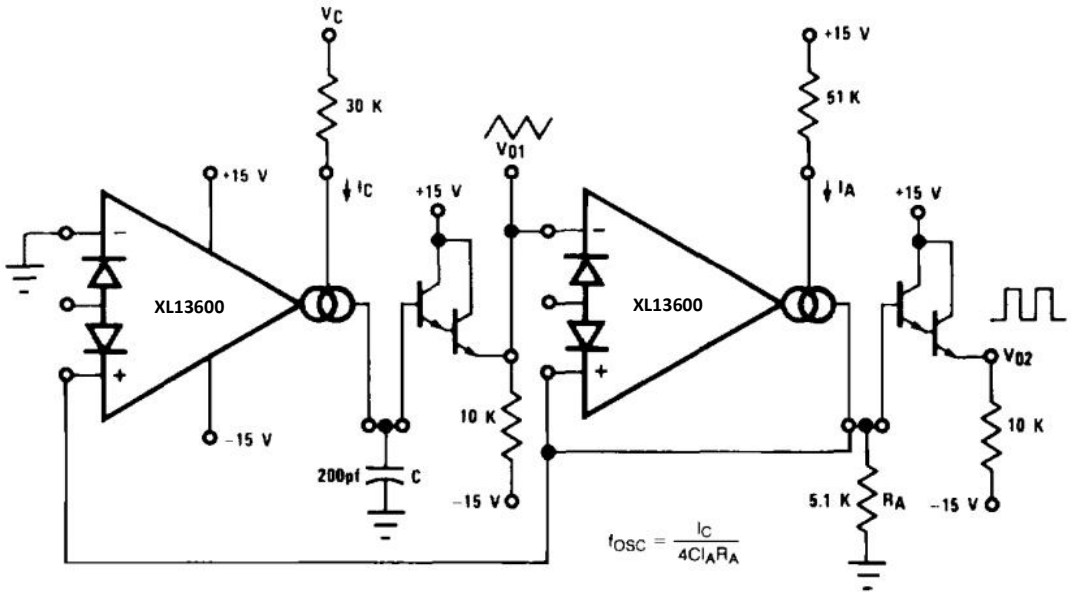


FIGURE 15. Triangular/Square-Wave VCO

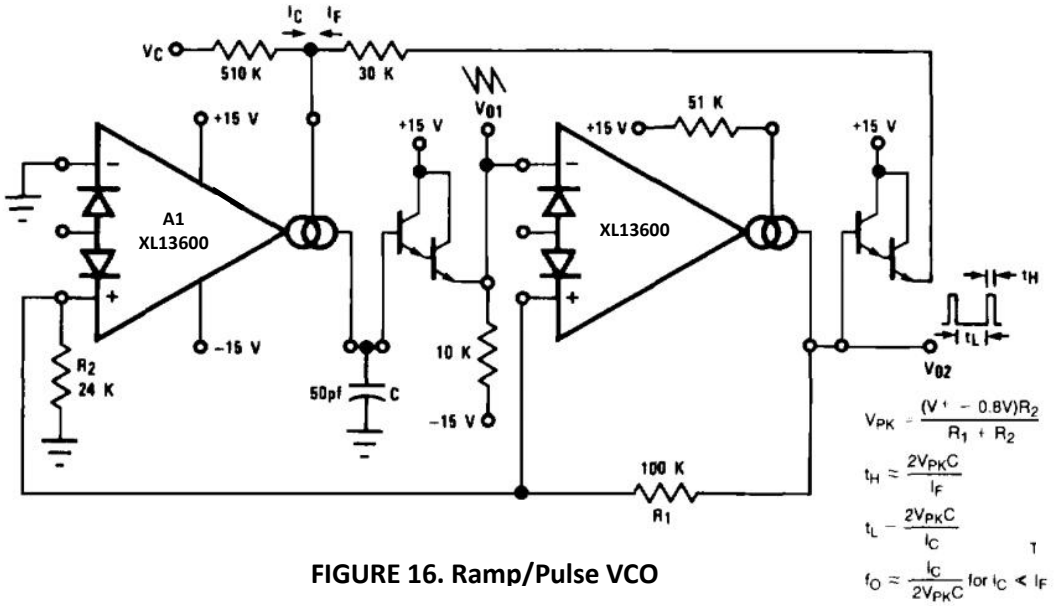


FIGURE 16. Ramp/Pulse VCO

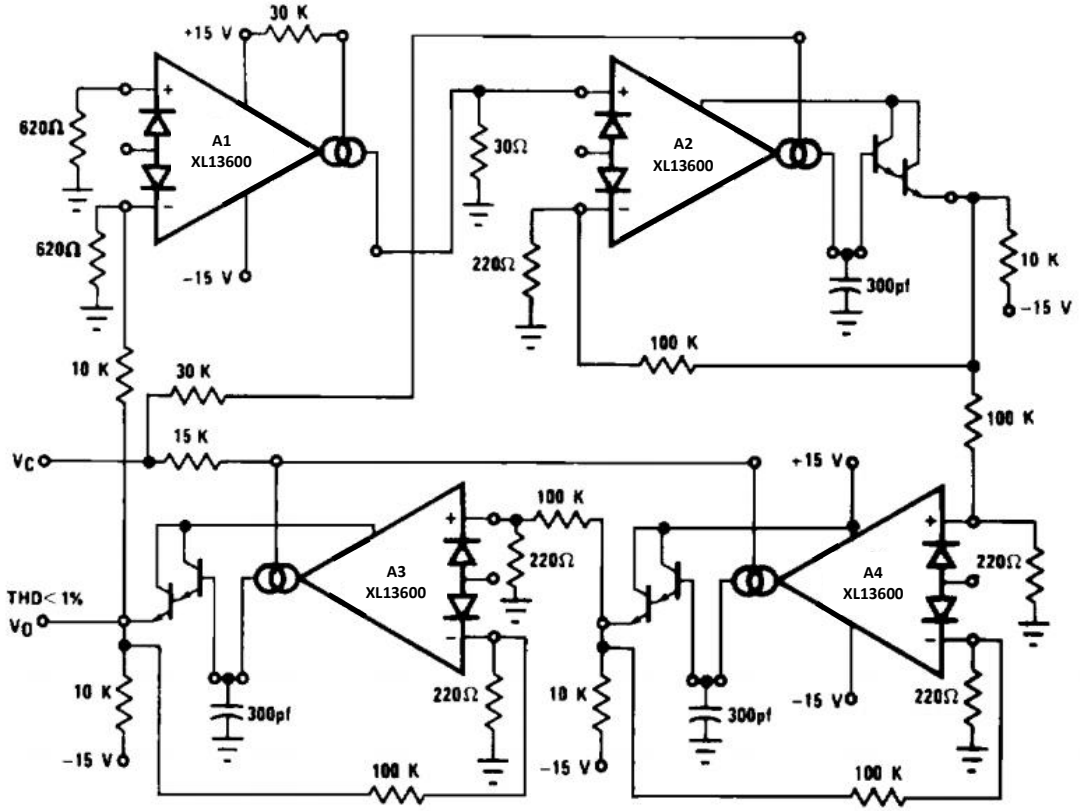


FIGURE 17. Sinusoidal VCo

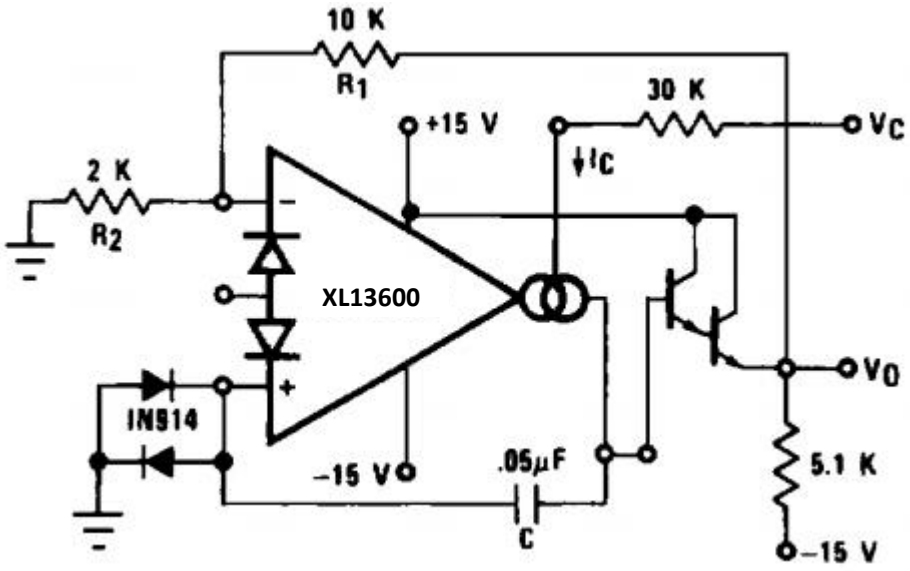


FIGURE 18. Single Amplifier VCo

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

17. ADDITIONAL APPLICATIONS

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through RB and pulls the non-inverting input high. The am-plifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input.The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting in-put so than an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O,can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of Figure 20 is very straight-forward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O.Cc and Rc serve to stabilize the unity-gain configuration of am-plifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the XL/XD13600 slew rate into 150 pF when the (V_{IN1}-VI_{N2}) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of Figure 21 uses the four-quad-rant multiplier of Figure 6 and the VCO of Figure 18 to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

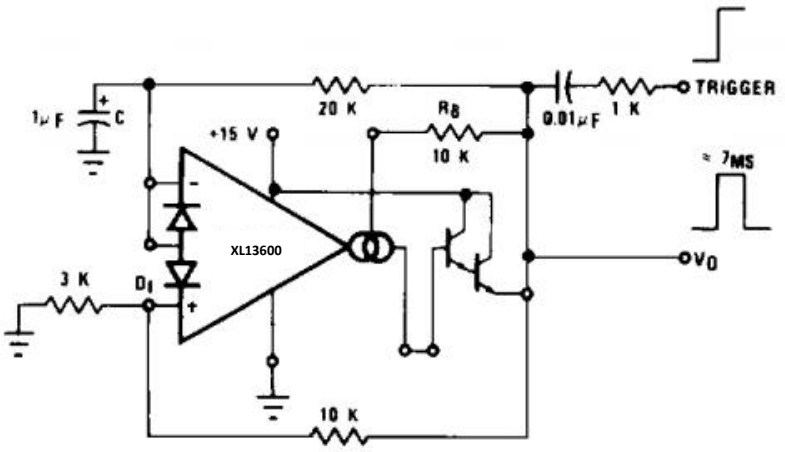


FIGURE 19. Zero Stand-By Power Timer

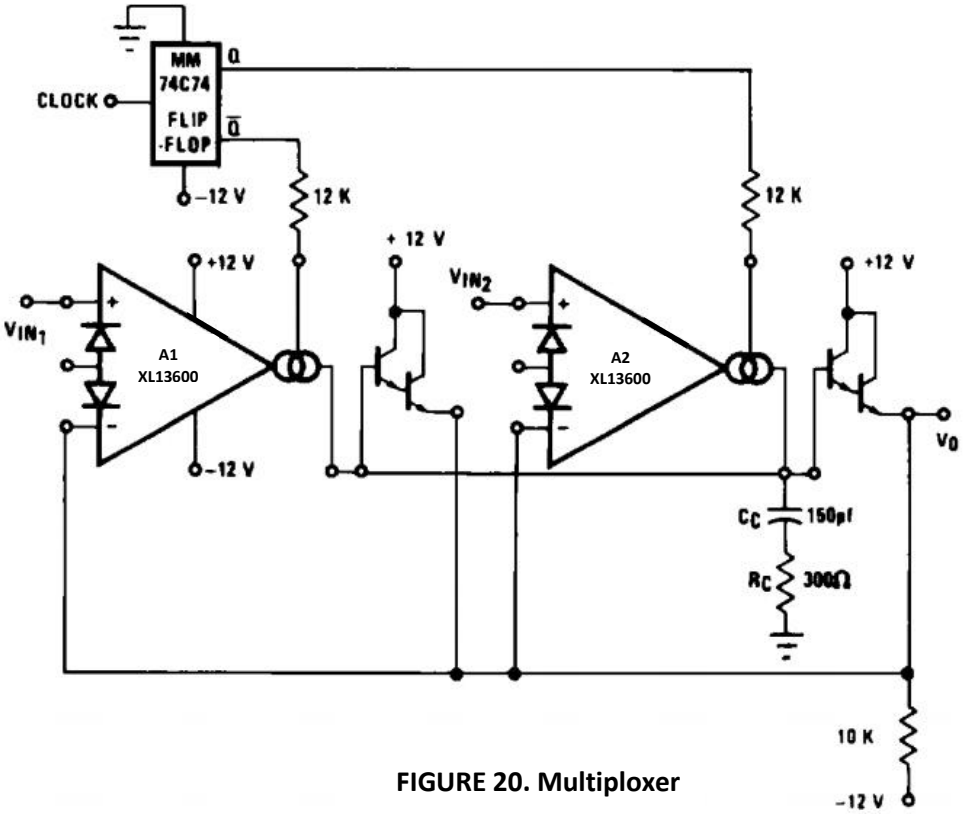


FIGURE 20. Multiploxer

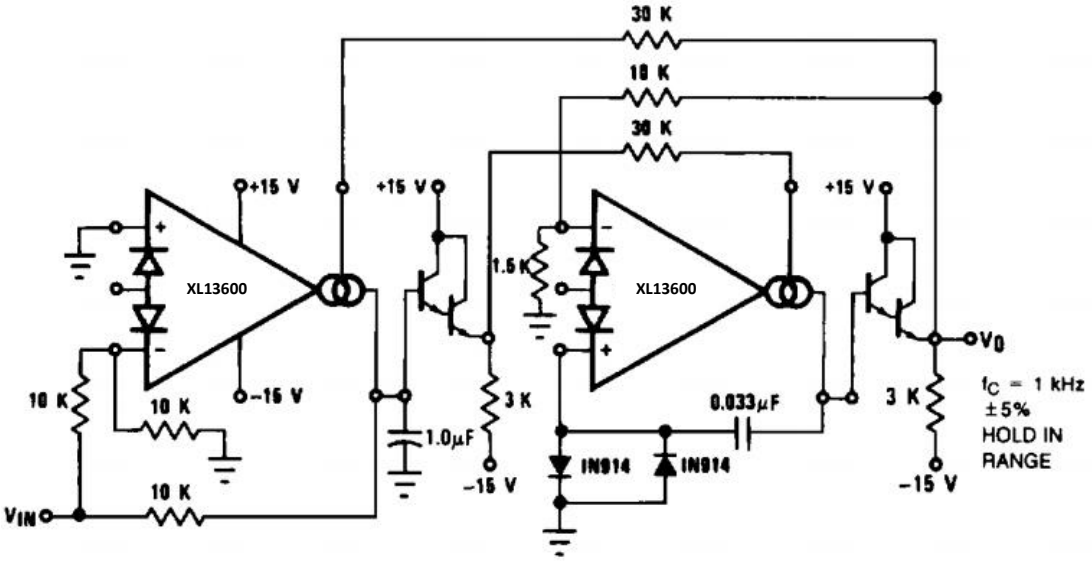


FIGURE 21. Phase Lock Loop

ADDITIONAL APPLICATIONS(Continued)

The Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying Ig will produce a Schmitt Trigger with variable hysteresis.

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input,an amount of charge equal to $(V_H\text{-}V_L)$ Ct is sourced into C_f and R_t. This once-per-cycle charge is then balanced by the current of V_O/R_t. The maximum f_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the XL/XD13600.D1 is added to provide a discharge path for C_1 when A_1 switches low.The Peak Detector of Figure 24 uses A2 to turn on A1

whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN}PK. One precautlon to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

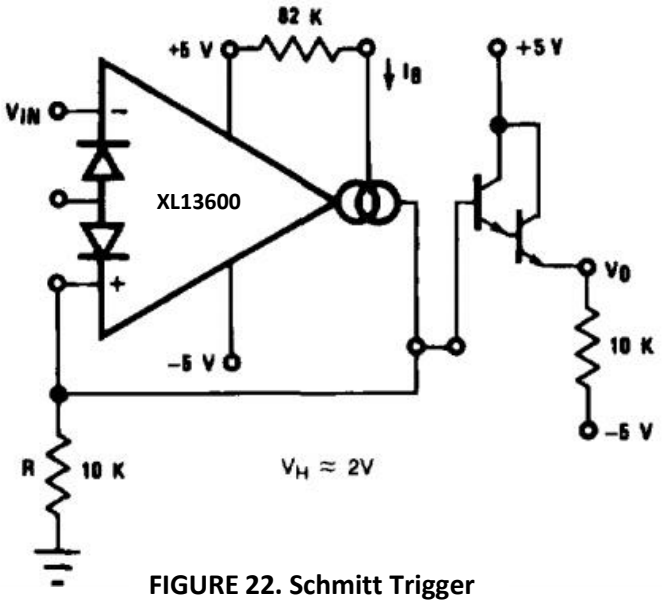


FIGURE 22. Schmitt Trigger

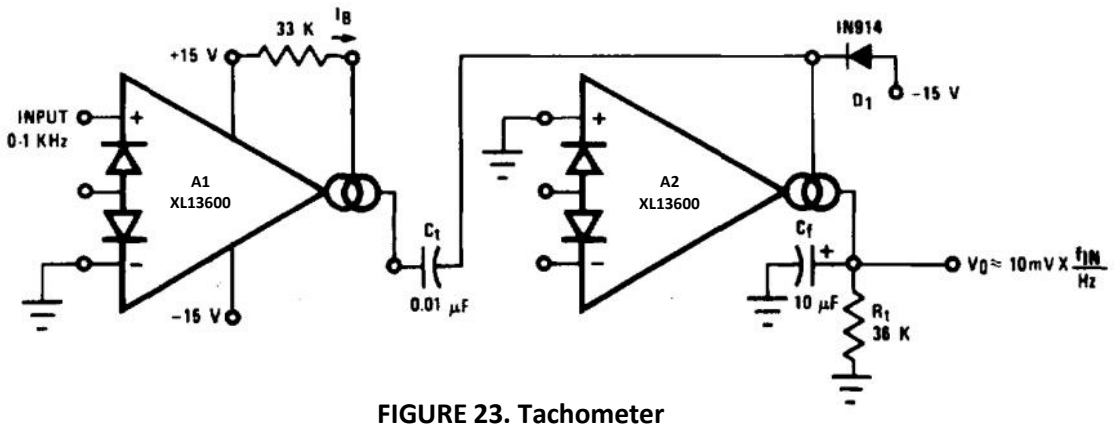


FIGURE 23. Tachometer

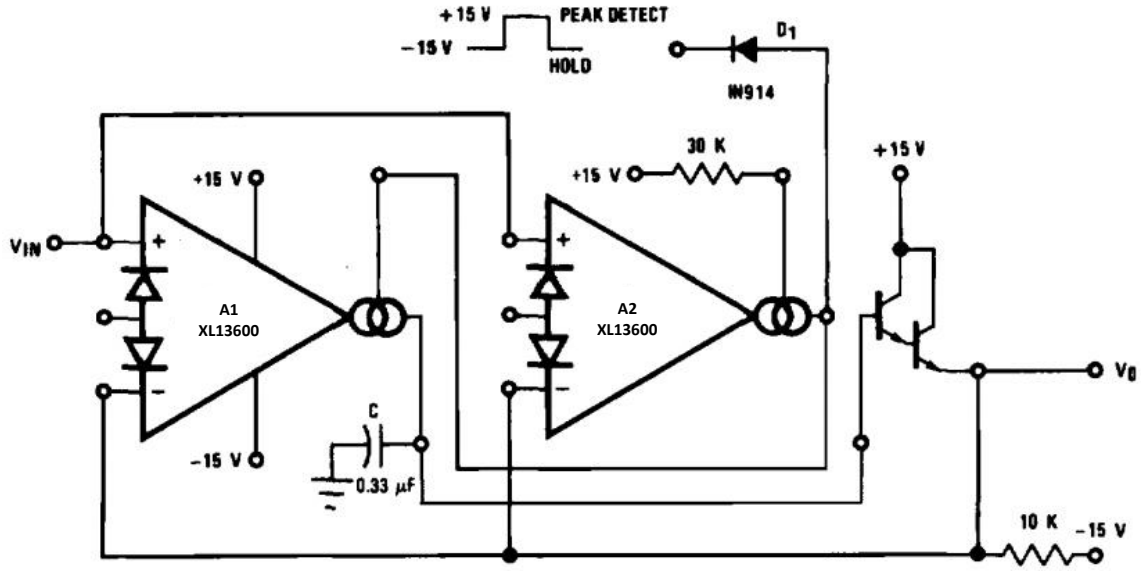


FIGURE 24. Peak Detector and Hold Circuit

The Sample-Hold circuit of Figure 25 also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously. The Ramp-and-Hold of Figure 26 sources lg into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true-RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also pro portional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and there fore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiome. ter is set such that V_O reads directly in RMS volts.

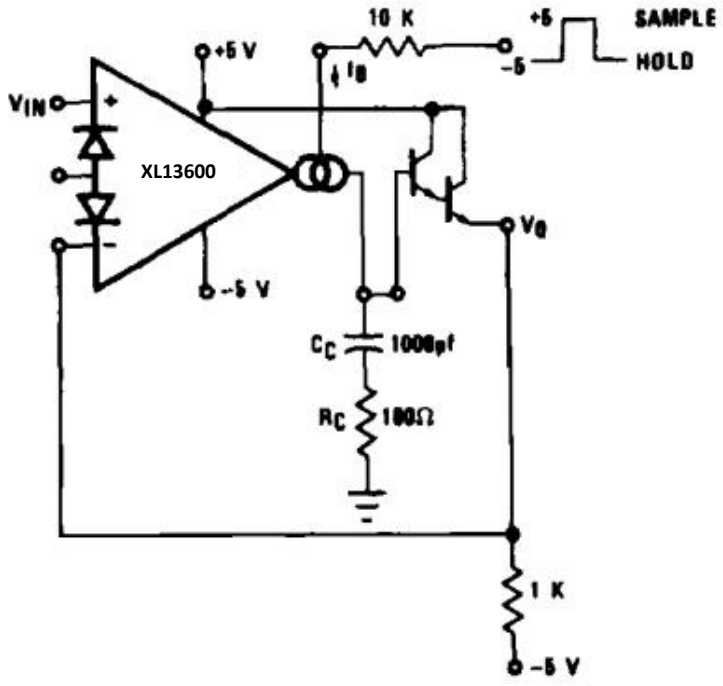


FIGURE 25. Sample-Hold Circuit

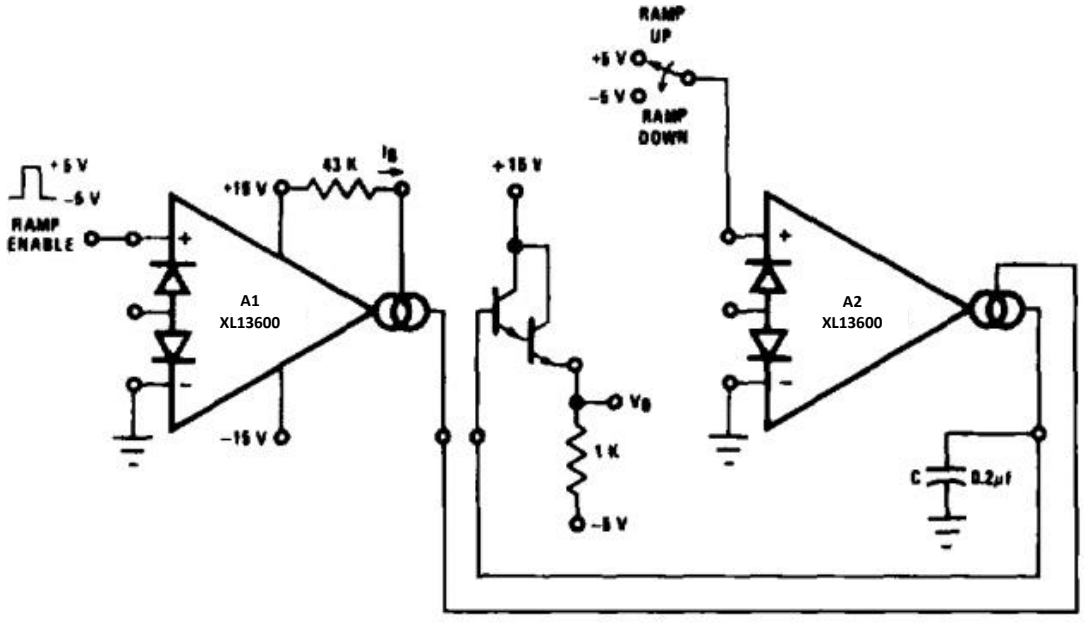


FIGURE 26. Ramp and Hold

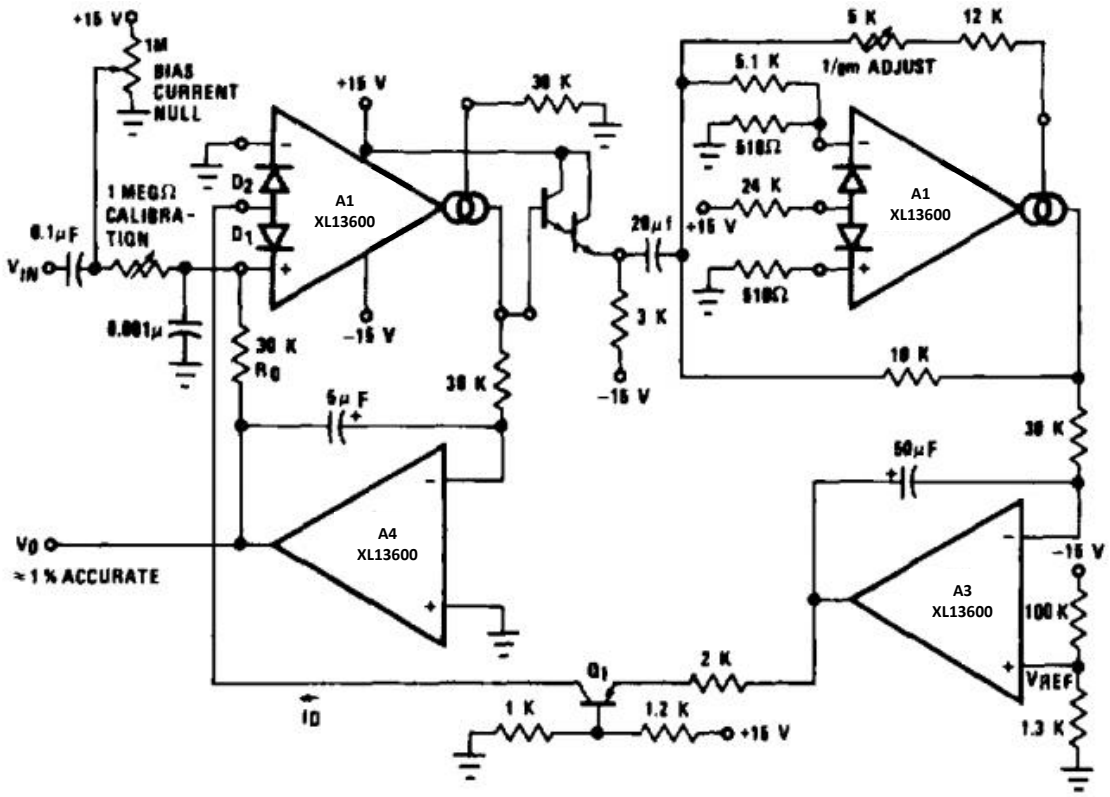


FIGURE 27. True RMS Converter

The circuit of Figure 28 is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V.zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of Figure 29 responds to the ratio of currents through buffer transistors Q3and Q4. Zero tempera ture dependence for V_{OUT} is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3and Q4.

The wide dynamic range of the XL/XD13600 allows easy con.trol of the output pulse width in the Pulse Width Modulator of Figure 30.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to Iɜ =-Vc/Rc.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be operating within its !inear range. From equation (5), the input voltage to A1 is:

$$V_{IN1} = \frac{-2kTI_3}{qI_2} = \frac{2kTV_C}{qI_2R_C}$$

ADDITIONAL APPLICATIONS(Continued)

The voltage on the base of Q1 is then：

$$V_{B1} \approx \frac{(R_1 + R_2)\, V_{IN1}}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_{B1} = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp\left[\frac{2(R_1 + R_2)\, V_C}{R_1 I_2 R_C}\right]$$

This logarithmic current can be used to bias the circuit of Figure 4 provide a temperature independent stereo attenuation characteristic.

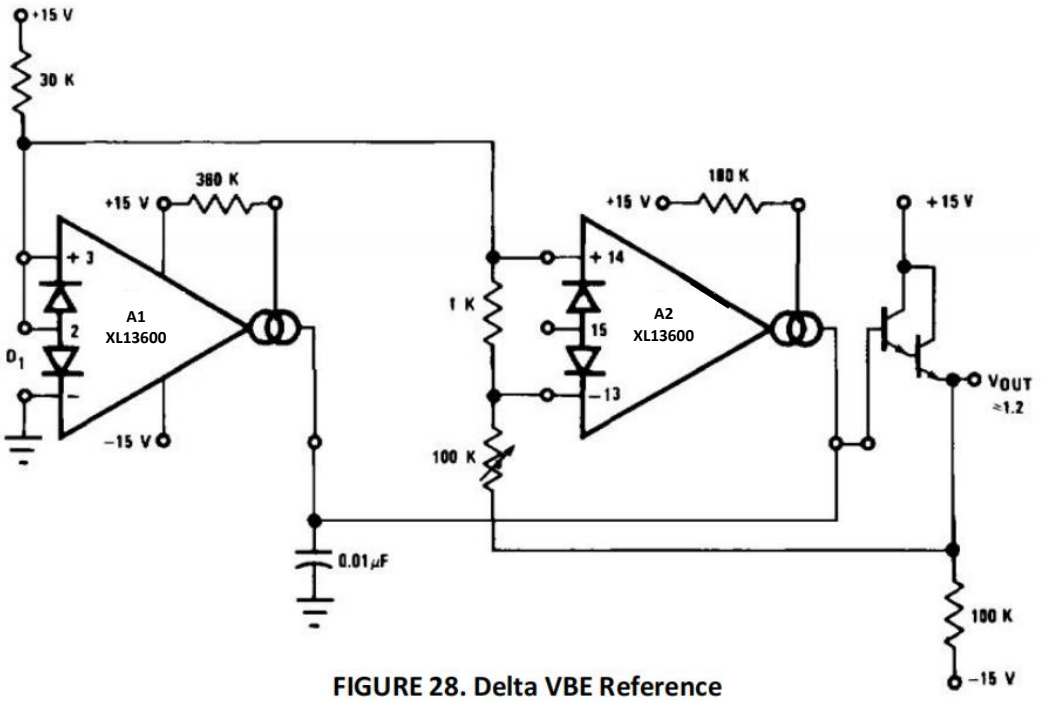


FIGURE 28. Delta VBE Reference

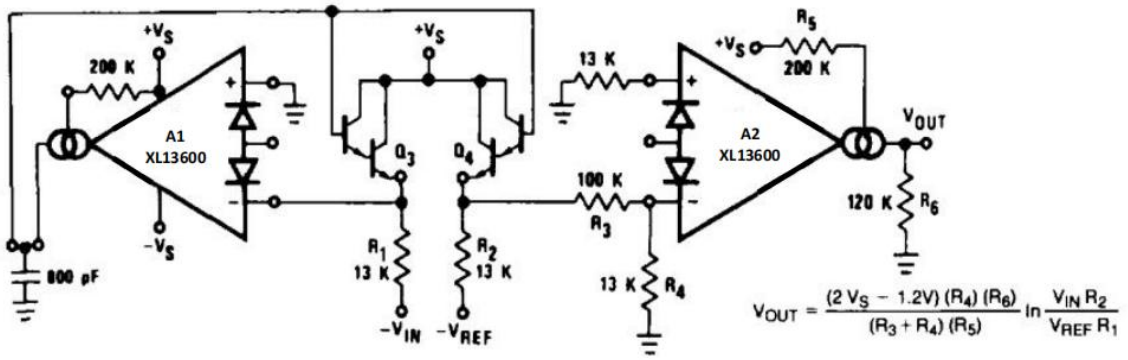


FIGURE 29. Log Amplifier

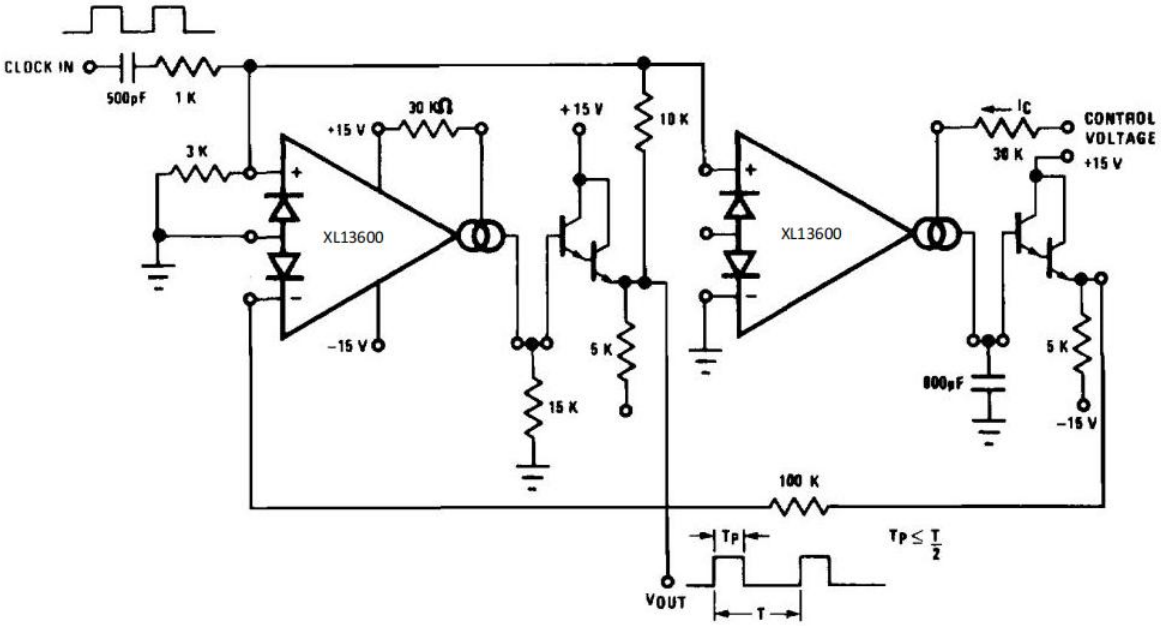


FIGURE 30. Pulse Width Modulator

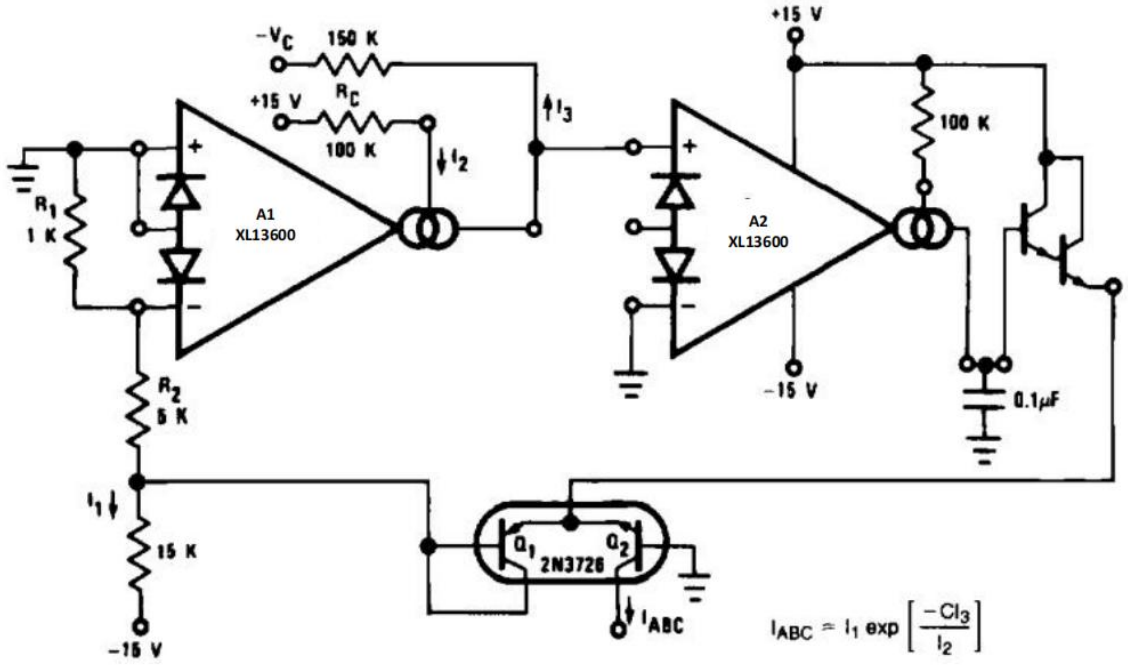


FIGURE 31. Logarlthmic Current Source

18. ORDERING INFORMATION

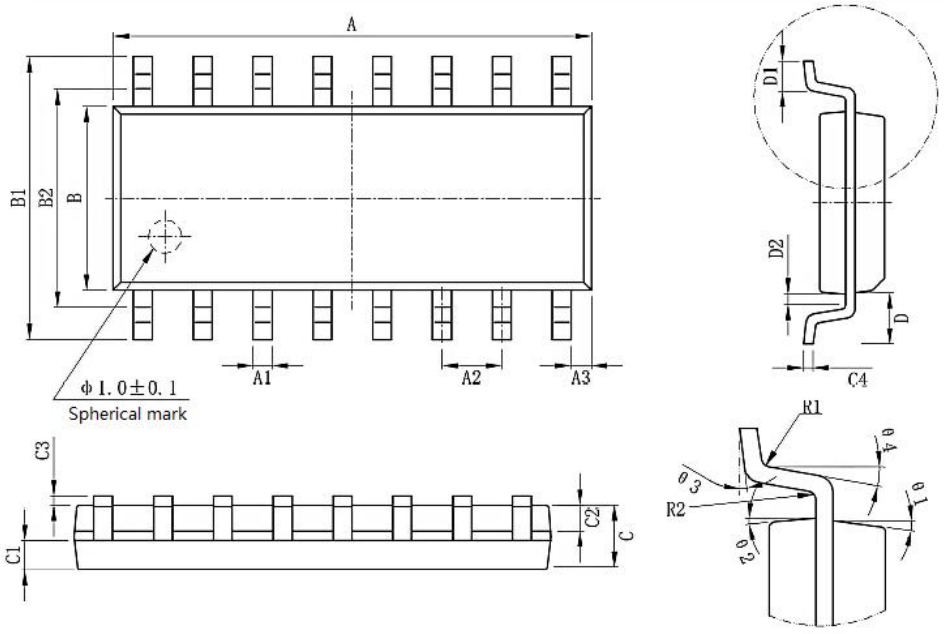
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL13600	XL13600	SOP16	10.00*3.95	-40 to +85	MSL3	T&R	2500
XD13600	XD13600	DIP16	19.05*6.35	-40 to +85	MSL3	Tube 25	1000

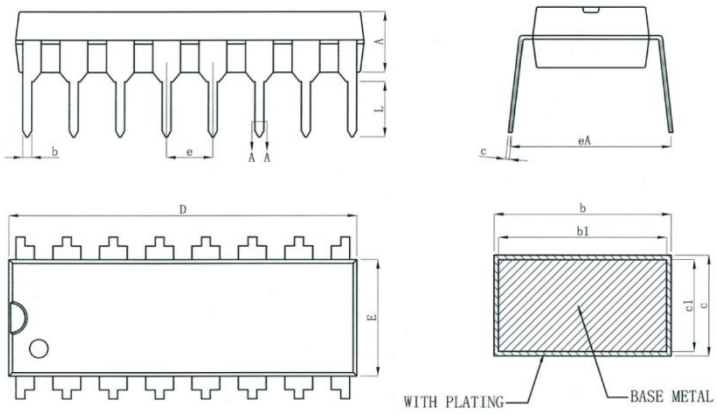
19. DIMENSIONAL DRAWINGS

SOP16

SYM / MARK	MIN (mm)	MAX (mm)	SYM / MARK	MIN (mm)	MAX (mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.40	1.60	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.05	0.25			



DIP16



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---