芯伯乐®
XINBOLE

Product Specification

XBLW SN74LS273

Octal D-type flip-flop with reset; positive edge-trigger

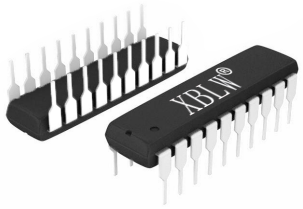
WEB | www.xinboleic.com

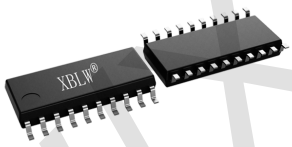
Description

The SN74LS273 is a octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset ($\overline{MR}$) inputs. The outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on $\overline{MR}$ forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features

- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Specified from -20°C to +85°C
- Packaging information: DIP-20/SOP-20/TSSOP-20/SOIC-20-208mil


DIP–20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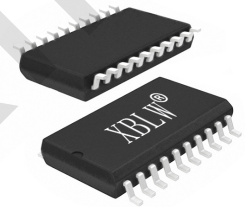
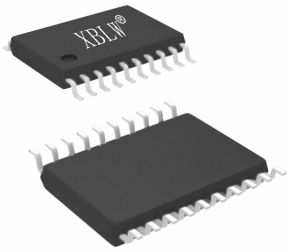

SOP–20


TSSOP-20

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS273N	DIP-20	74LS273N	Tube	720Pcs/Box
XBLW SN74LS273DTR	SOP-20	74LS273	Tape	2000Pcs/Reel
XBLW SN74LS273TDTR	TSSOP-20	74LS273	Tape	2000Pcs/Reel
XBLW SN74LS273NSDTR	SOIC-20-208mil	74LS273	Tape	2000Pcs/Reel

Block Diagram

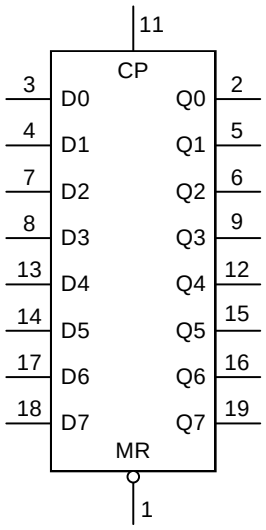


Figure 1. Logic symbol

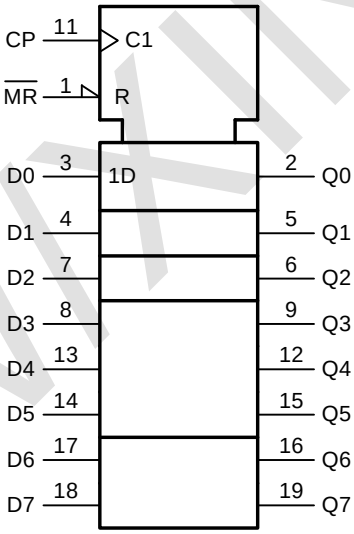


Figure 2. IEC logic symbol

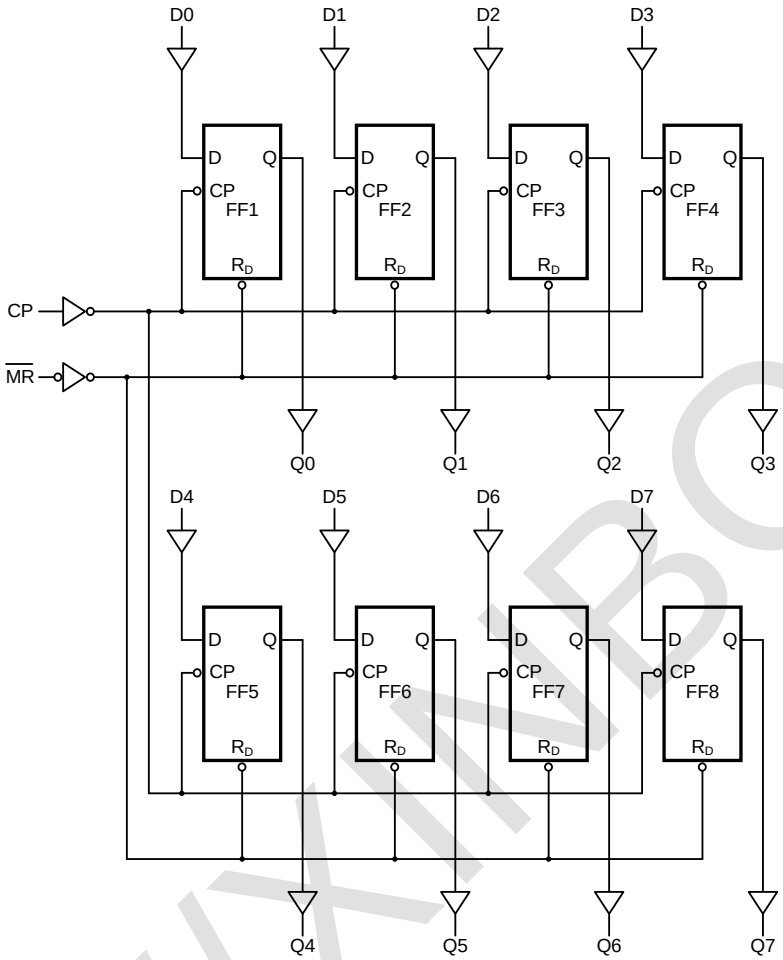


Figure 3. Logic diagram

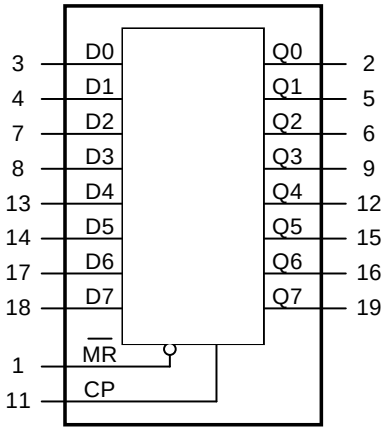
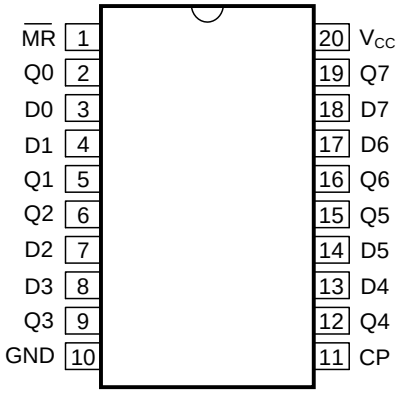


Figure 4. Functional diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	$\overline{MR}$	master reset input (active LOW)
2	Q0	flip-flop output
3	D0	data input
4	D1	data input
5	Q1	flip-flop output
6	Q2	flip-flop output
7	D2	data input
8	D3	data input
9	Q3	flip-flop output
10	GND	ground (0V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
12	Q4	flip-flop output
13	D4	data input
14	D5	data input
15	Q5	flip-flop output
16	Q6	flip-flop output
17	D6	data input
18	D7	data input
19	Q7	flip-flop output
20	V_{CC}	supply voltage

Function Table

Operating modes	Input			Output
	$\overline{MR}$	CP	Dn	Qn
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clocktransition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clocktransition;
↑=LOW-to-HIGH clock transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		℃

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-20	-	+85	℃

Electrical Characteristics

DC Characteristics 1

(T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(T_{amb}=-20°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA

AC Characteristics 1

(T_{amb}=25°C, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	13	26	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	44	150	ns
			V_{CC}=4.5V	-	16	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	26	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
		$\overline{MR}$ input LOW; see Figure 7	V_{CC}=2.0V	60	17	-	ns
			V_{CC}=4.5V	12	6	-	ns
			V_{CC}=6.0V	10	5	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7	V_{CC}=2.0V	50	-6	-	ns
			V_{CC}=4.5V	10	-2	-	ns
			V_{CC}=6.0V	9	-2	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8	V_{CC}=2.0V	60	11	-	ns
			V_{CC}=4.5V	12	4	-	ns
			V_{CC}=6.0V	10	3	-	ns
hold time	t_h	Dn to CP; see Figure 8	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	6	20.6	-	MHz
			V_{CC}=4.5V	30	103	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	66	-	MHz
			V_{CC}=6.0V	35	122	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I=GND to V_{CC}		-	20	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} isused to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

AC Characteristics 2

(T_{amb}=-20℃ to +85℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	-	185	ns
			V_{CC}=4.5V	-	-	37	ns
			V_{CC}=6.0V	-	-	31	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	-	185	ns
			V_{CC}=4.5V	-	-	37	ns
			V_{CC}=6.0V	-	-	31	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	15	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{MR}$ input LOW; see Figure 7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	73	-	-	ns
hold time	t_h	Dn to CP; see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

Measurement Points

Type	Input		Output
	V_I	V_M	V_M
SN74LS273	V_{CC}	0.5×V_{CC}	0.5×V_{CC}

Test Data

Type	Input		Load		S1 position
	V_I	t_r ,t_f	C_L	R_L	t_{PHL}, t_{PLH}
SN74LS273	V_{CC}	6ns	15pF, 50pF	1kΩ	open

Testing Circuit

AC Testing Circuit

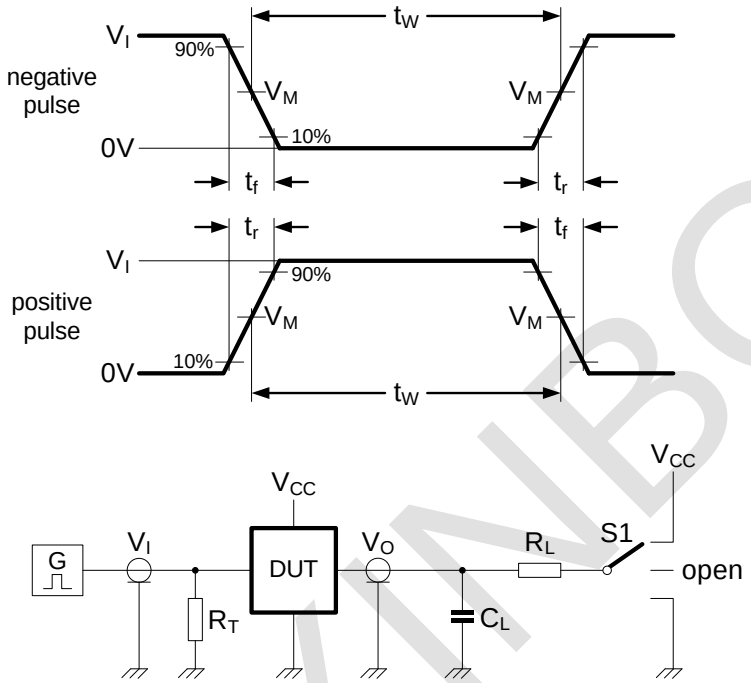


Figure 5. Test circuit for measuring switching times

Definitions for test circuit: R_L=Load resistance.
C_L=Load capacitance including jig and probe capacitance.
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.
S1=Test selection switch.

AC Testing Waveforms

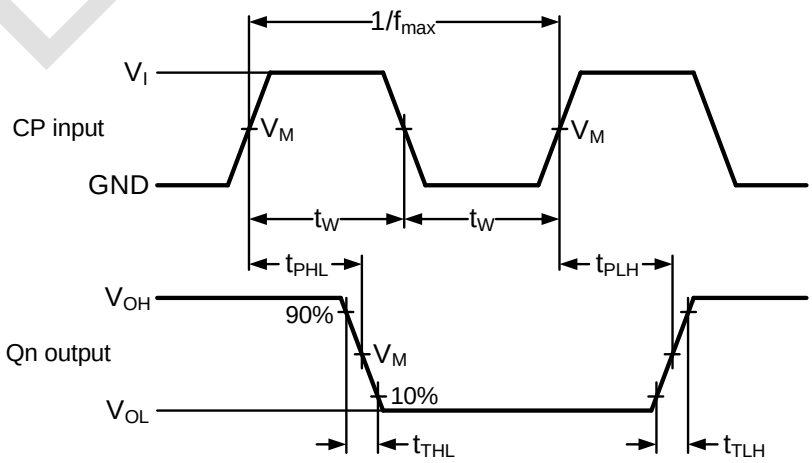


Figure 6. Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency

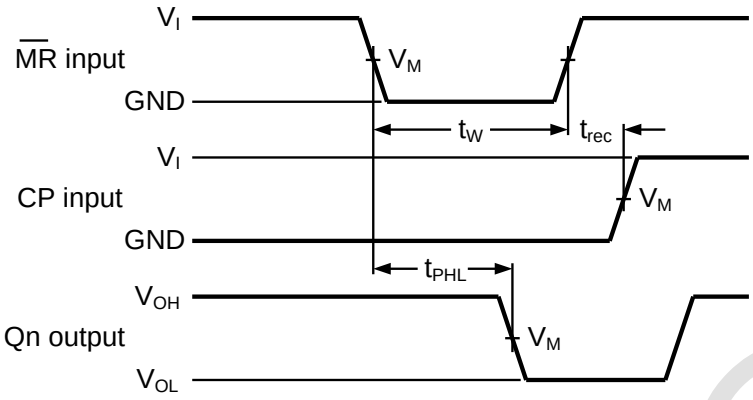


Figure 7. Propagation delay master reset ($\overline{MR}$) to output (Qn), pulse width master reset ($\overline{MR}$) andrecovery time master reset ($\overline{MR}$) to clock (CP)

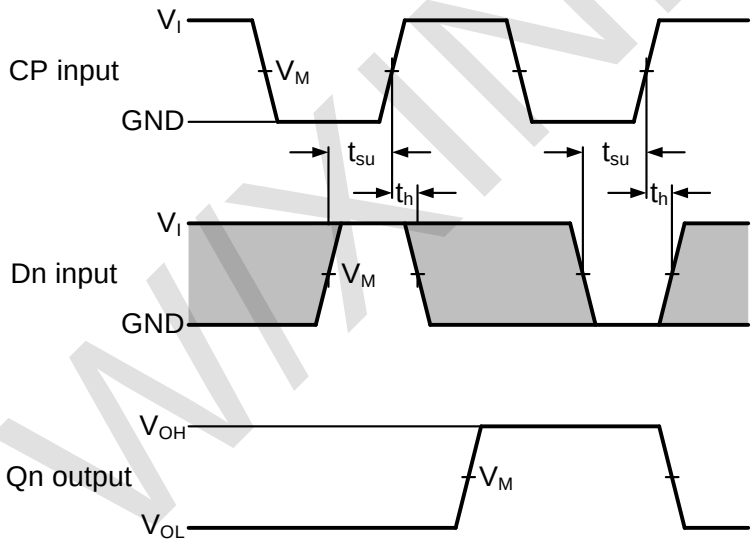
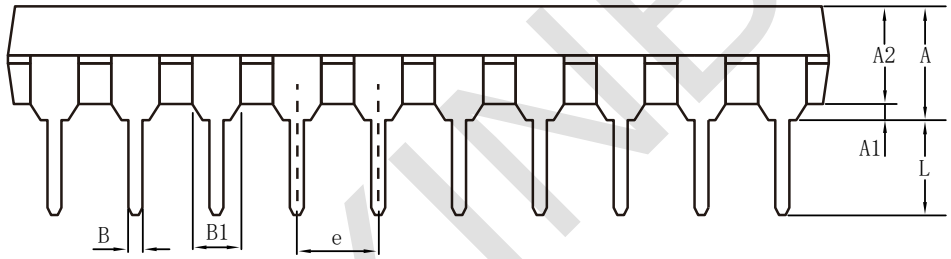


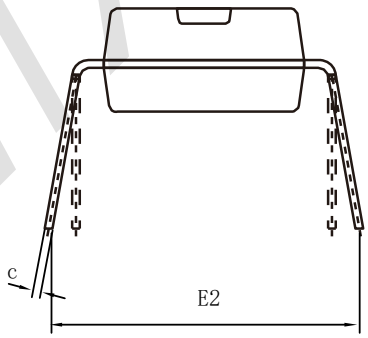
Figure 8. Data set-up and hold times data input (Dn)

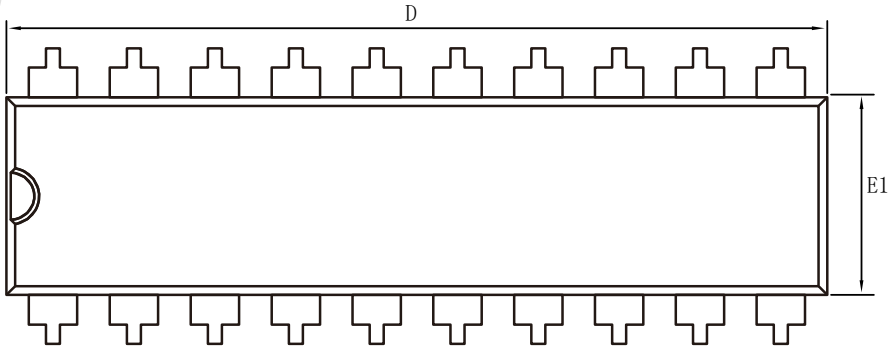
Package Information

· DIP-20

Size / Symbol	Dimensions In Millimeters Min(mm)	Max(mm)	Size / Symbol	Dimensions In Inches Min(in)	Max(in)
A	3.600	5.330	A	0.142	0.210
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.360	0.530	B	0.014	0.021
B1	1.52(BSC)		B1	0.060(BSC)	
c	0.204	0.360	c	0.008	0.014
D	25.70	26.54	D	1.010	1.040
E1	6.200	6.750	E1	0.244	0.260
E2	7.620	9.300	E2	0.300	0.366
e	2.54(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142

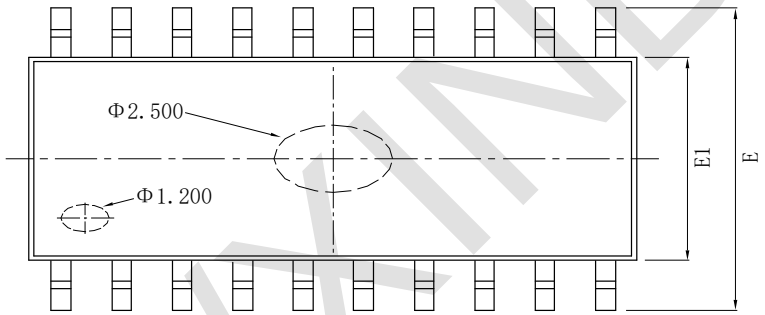


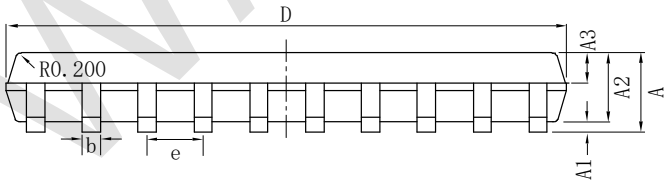


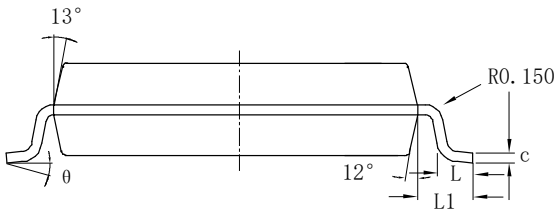


· SOIC-20-208mil

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		2.000	A		0.079
A1	0.050	0.250	A1	0.002	0.010
A2	1.650	1.850	A2	0.065	0.073
b	0.350	0.550	b	0.014	0.022
c	0.150	0.200	c	0.006	0.008
D	12.25	12.65	D	0.482	0.498
E	7.600	8.000	E	0.299	0.315
E1	5.100	5.500	E1	0.201	0.217
e	1.270		e	0.050	
L	0.550	0.950	L	0.022	0.037
L1	1.250		L1	0.049	
θ	0°	8°	θ	0°	8°

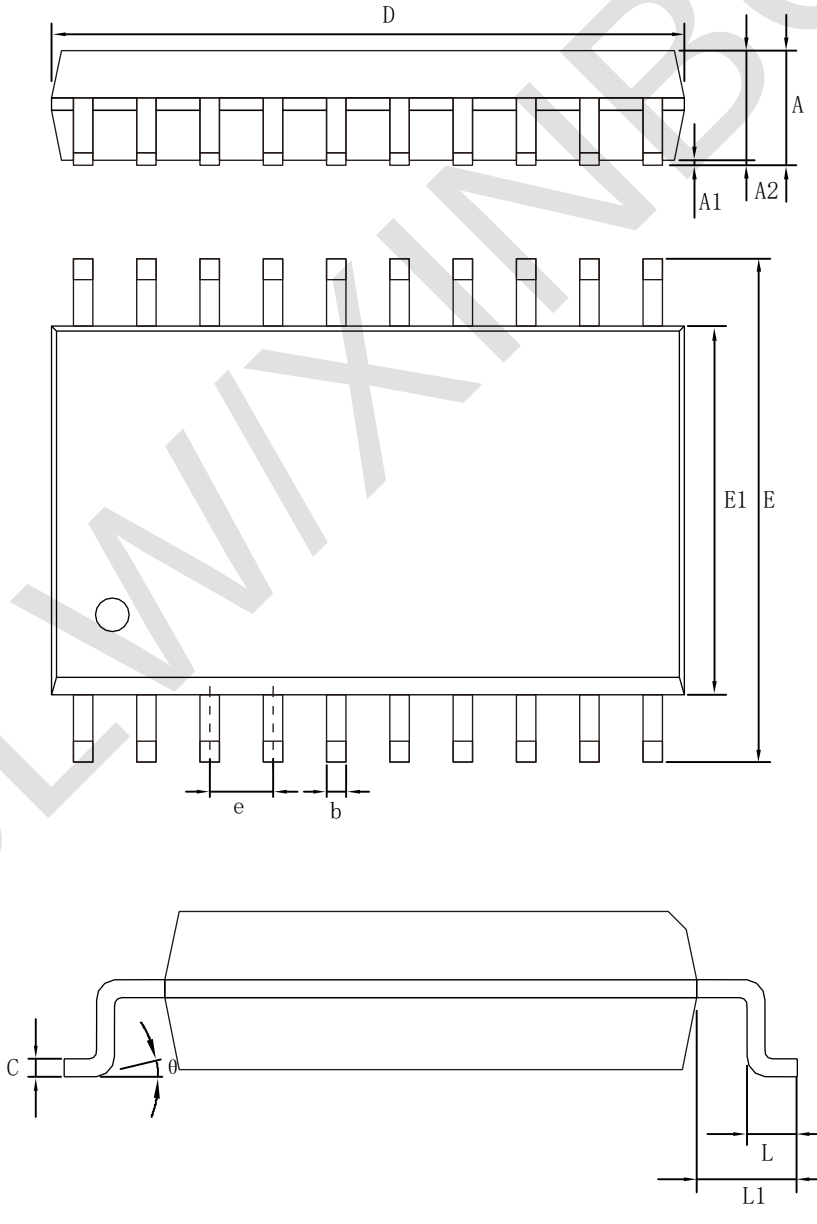






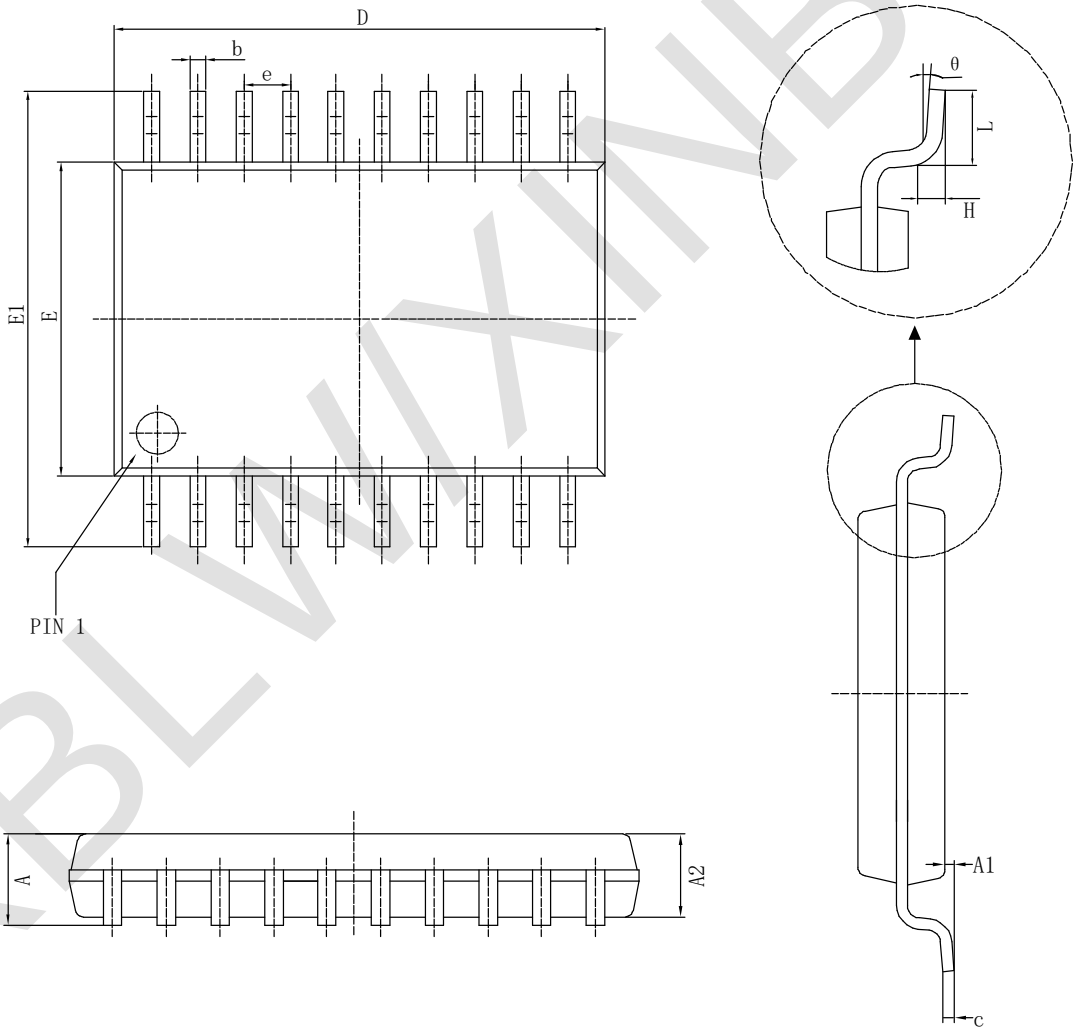
· SOP-20

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	2.470	2.650	A	0.097	0.104
A1	0.050	0.300	A1	0.002	0.012
A2	2.200	2.440	A2	0.087	0.096
b	0.350	0.500	b	0.014	0.020
c	0.150	0.300	c	0.006	0.012
D	12.54	12.94	D	0.494	0.509
E	10.00	10.60	E	0.394	0.417
E1	7.300	7.700	E1	0.287	0.303
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.050	L	0.016	0.041
L1	1.300	1.500	L1	0.051	0.059
θ	0°	8°	θ	0°	8°



· TSSOP-20

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
D	6.400	6.600	D	0.252	0.259
E	4.300	4.500	E	0.169	0.177
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.008
E1	6.250	6.550	E1	0.246	0.258
A		1.200	A		0.047
A2	0.800	1.000	A2	0.031	0.039
A1	0.050	0.150	A1	0.002	0.006
e	0.65(BSC)		e	0.026(BSC)	
L	0.500	0.700	L	0.020	0.028
H	0.25(TYP)		H	0.01(TYP)	
θ	1°	7°	θ	1°	7°



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