SC120N170T8L

Silicon Carbide Power MOSFET N-Channe Enhancement Mode

Features

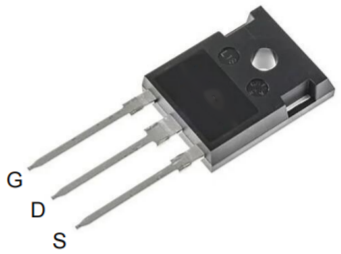
★ High Speed Switching with Low Capacitances
★ High Blocking Voltage with Low $R_{DS(on)}$
★ Easy to Parallel and Simple to Drive
★ Ultra-low Drain-gate capacitance
★ Halogen Free, RoHS Compliant

Product Summary

V_{DS}	$R_{DS(on)}$	I_D @25°
1700V	1.0Ω	5.0A

Benefits

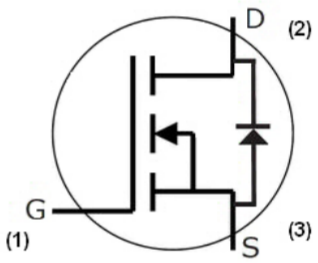
★ Higher System Efficiency
★ Increased System Switching Frequency
★ Reduced Cooling Requirements
★ Increased System Reliability



Applications

★ Auxiliary Power Supplies
★ Switch Mode Power Supplies
★ High-voltage Capacitive Loads

TO-247-3
Package



Maximum Ratings (T_C= 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1700	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	5.0	A	V_{GS} = 20 V, T_C = 25˚C	Fig. 19
		3.5		V_{GS} = 20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	15	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	69	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (TC= 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.8	4	V	V_{DS} = V_{GS}, I_D = 0.5 mA	Fig. 11
			2.4		V	V_{DS} = V_{GS}, I_D = 0.5 mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1.7 kV, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		0.80	1.4	Ω	V_{GS} = 20 V, I_D = 2 A	Fig. 4,5,6
			1.4			V_{GS} = 20 V, I_D = 2 A, T_J = 150 °C	
g_{fs}	Transconductance		1.04		S	V_{DS}= 20 V, I_{DS}= 2 A	Fig. 7
			1.09			V_{DS}= 20 V, I_{DS}= 2 A, T_J = 150 °C	
C_{iss}	Input Capacitance		215		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		19				
C_{rss}	Reverse Transfer Capacitance		2.2				
E_{oss}	C_{oss} Stored Energy		10.2		µJ		Fig 16
E_{ON}	Turn-On Switching Energy		89		µJ	V_{DS} = 1.2 kV, V_{GS} = -5/20 V I_D = 2 A, $R_{G(ext)}$ = 2.5 Ω, L= 1478 µH, T_J = 150 °C	Fig. 26
E_{OFF}	Turn Off Switching Energy		14				
$t_{d(on)}$	Turn-On Delay Time		5		ns	V_{DD} = 1.2 kV, V_{GS} = -5/20 V I_D = 2 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 600 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		19				
$t_{d(off)}$	Turn-Off Delay Time		14				
t_f	Fall Time		63				
$R_{G(int)}$	Internal Gate Resistance		24.8		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		4		nC	V_{DS} = 1.2 kV, V_{GS} = -5/20 V I_D = 2 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		12				
Q_g	Total Gate Charge		22				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.8		V	V_{GS} = - 5 V, I_{SD} = 1 A, T_J = 25 °C	Fig. 8, 9, 10
		3.3		V	V_{GS} = - 5 V, I_{SD} = 1 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		4	A	T_C= 25 °C	Note 1
t_{rr}	Reverse Recovery Time	30		ns	V_{GS} = - 5 V, I_{SD} = 2 A T_J = 150 °C V_R = 1.2 kV dif/dt = 1135 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	31		nC		
I_{rrm}	Peak Reverse Recovery Current	3		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.7	1.8	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

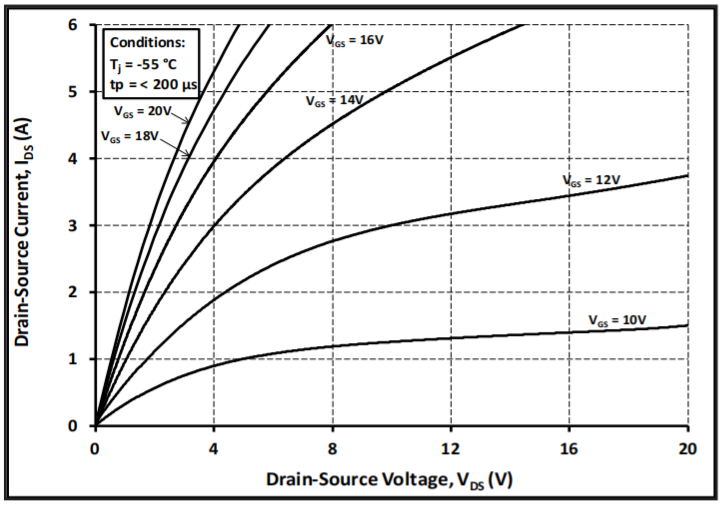


Figure 1. Output Characteristics T_J = -55 °C

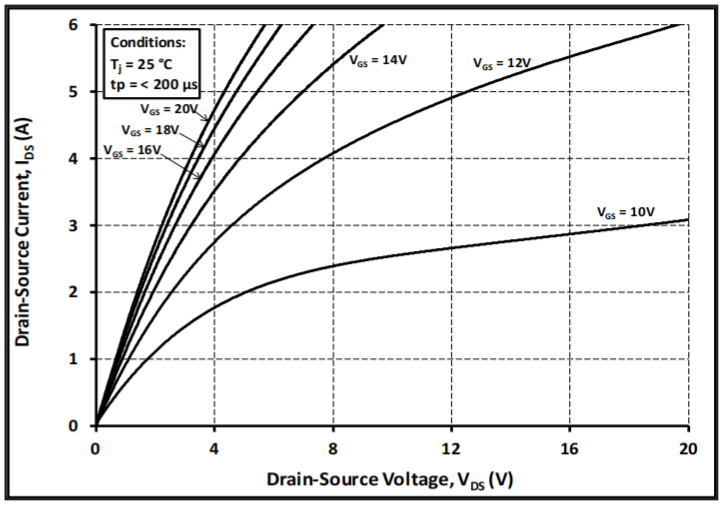


Figure 2. Output Characteristics T_J = 25 °C

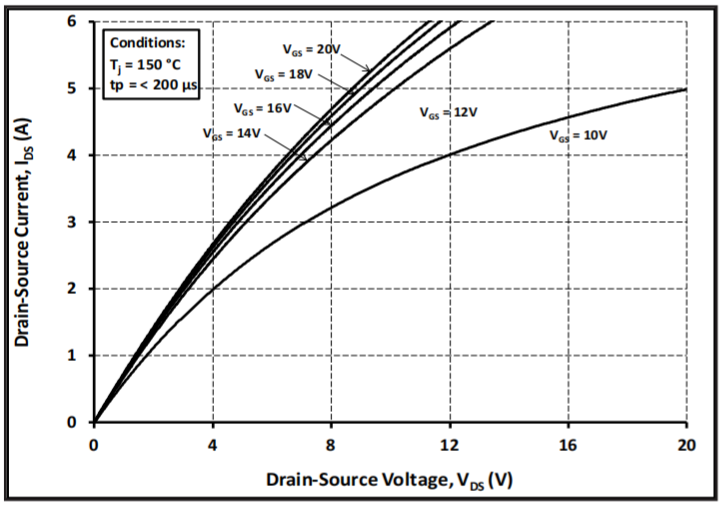


Figure 3. Output Characteristics T_J = 150 °C

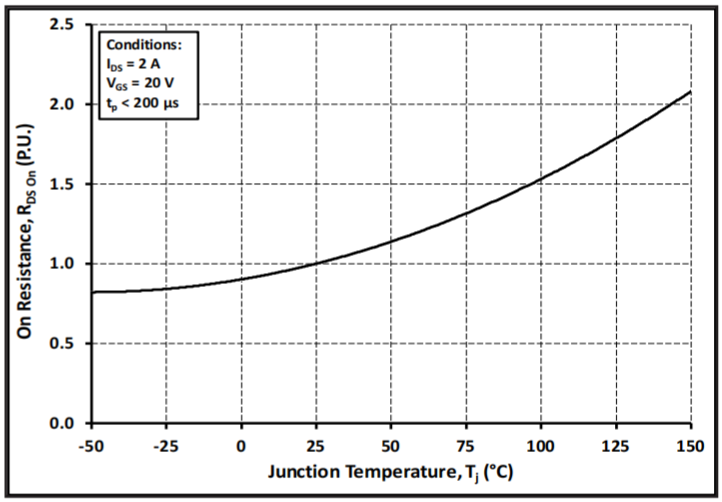


Figure 4. Normalized On-Resistance vs. Temperature

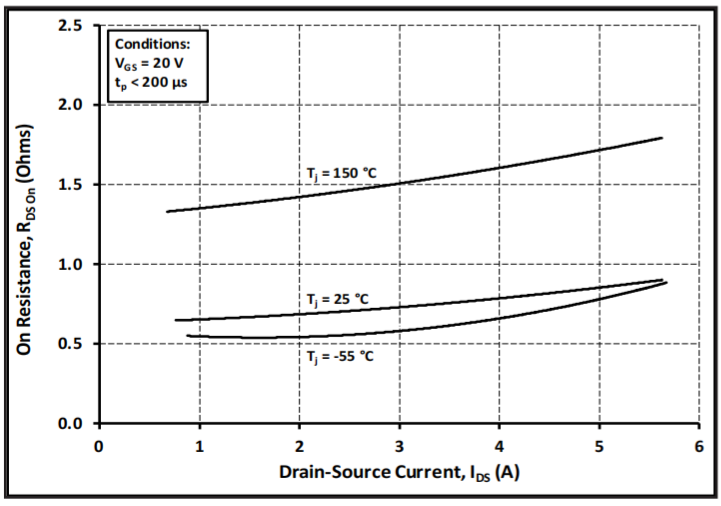


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

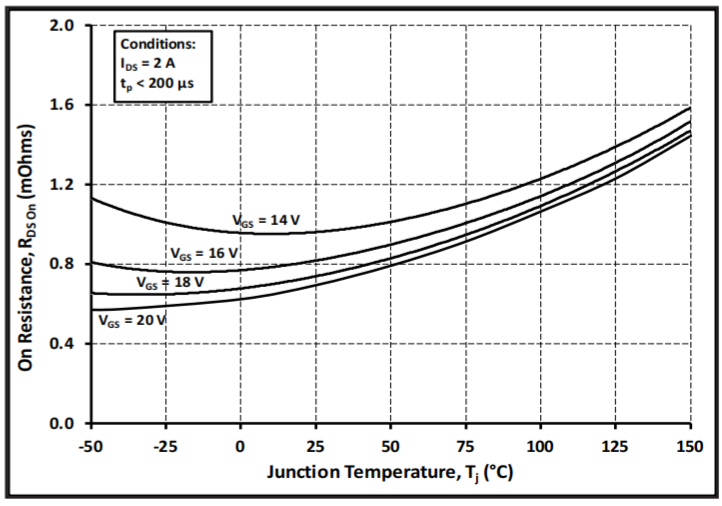


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

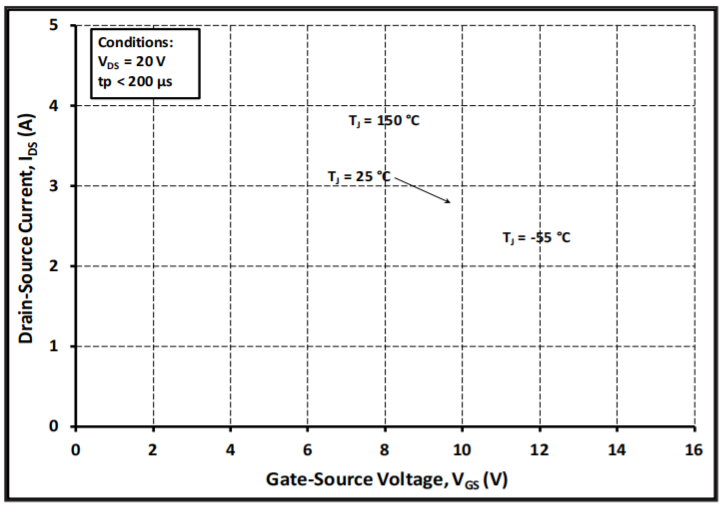


Figure 7. Transfer Characteristic for Various Junction Temperatures

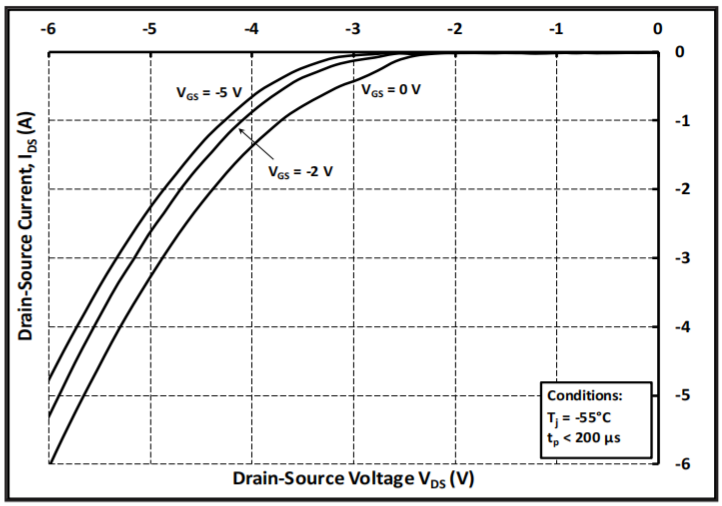


Figure 8. Body Diode Characteristic at -55 °C

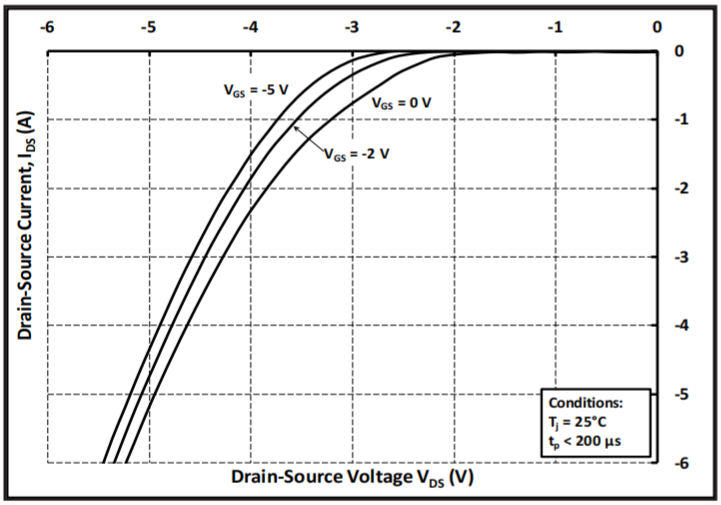


Figure 9. Body Diode Characteristic at 25 °C

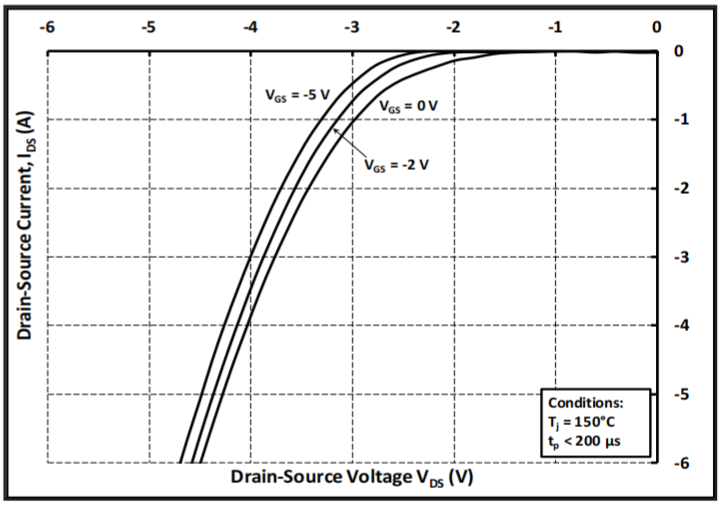


Figure 10. Body Diode Characteristic at 150 °C

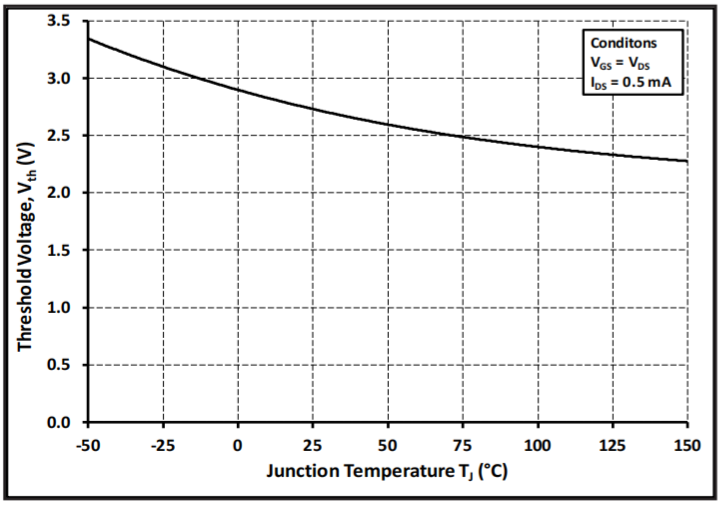


Figure 11. Threshold Voltage vs. Temperature

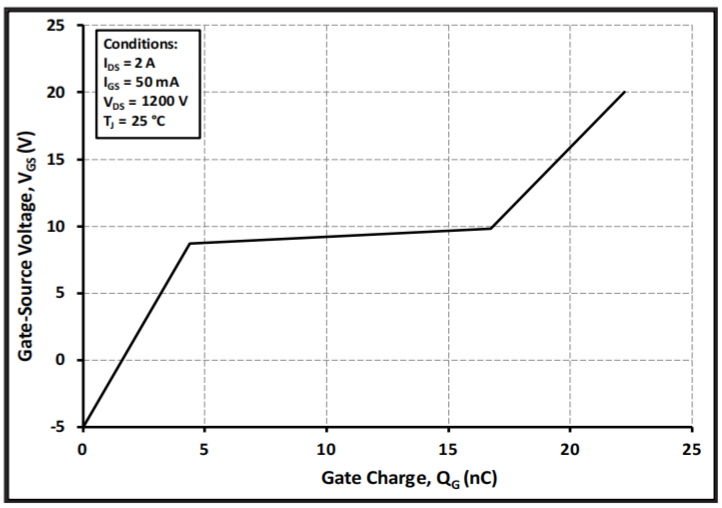


Figure 12. Gate Charge Characteristics

Typical Performance

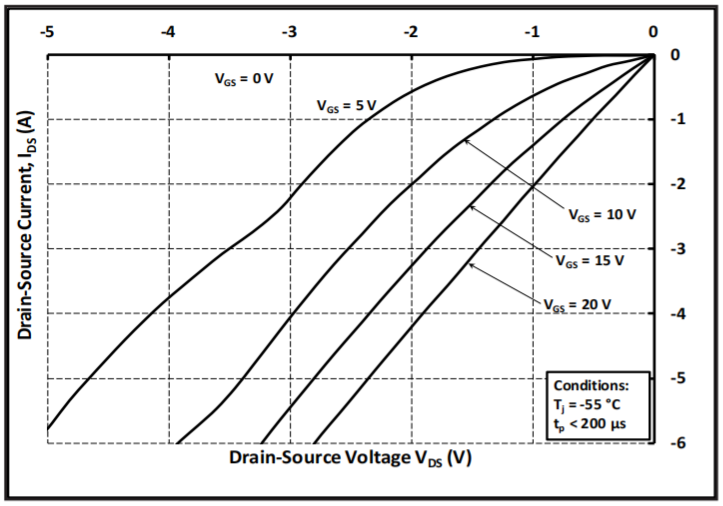


Figure 13. 3rd Quadrant Characteristic at -55 °C

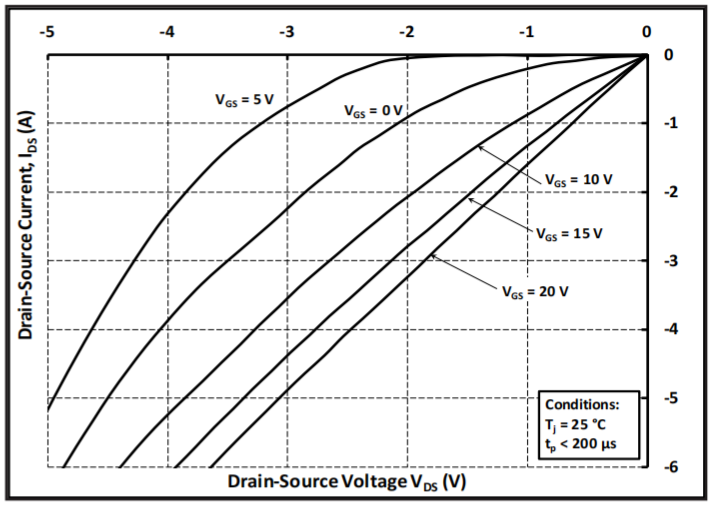


Figure 14. 3rd Quadrant Characteristic at 25 °C

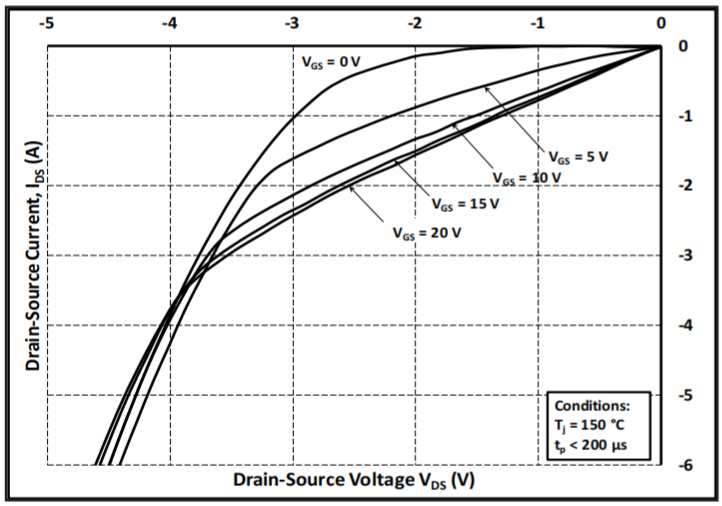


Figure 15. 3rd Quadrant Characteristic at 150 °C

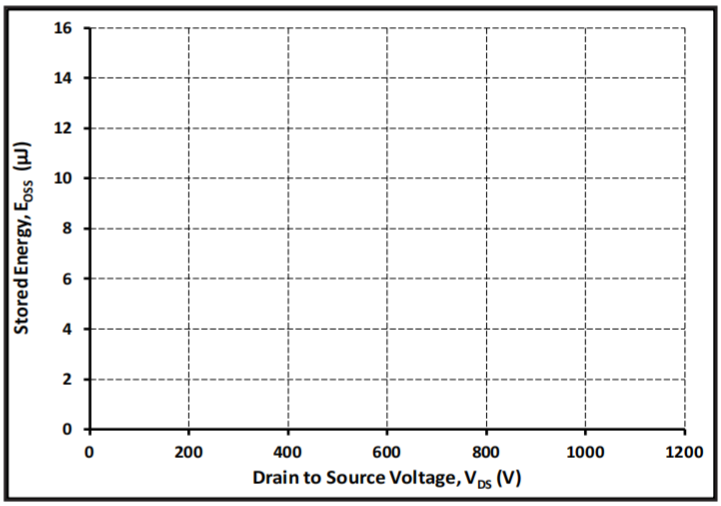


Figure 16. Output Capacitor Stored Energy

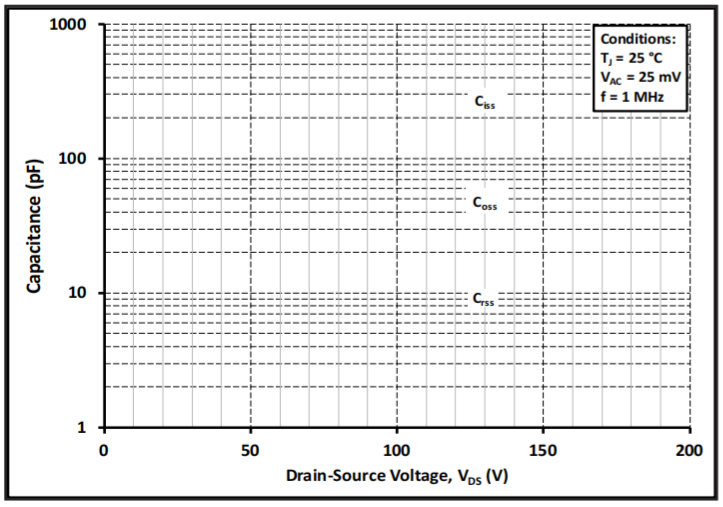


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

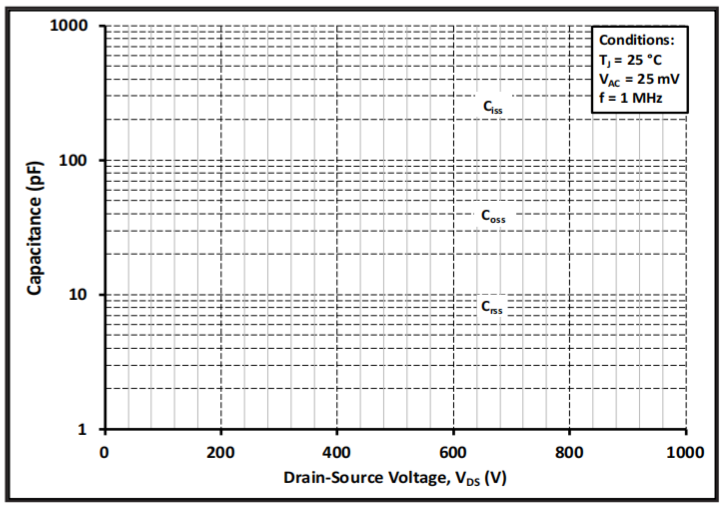


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

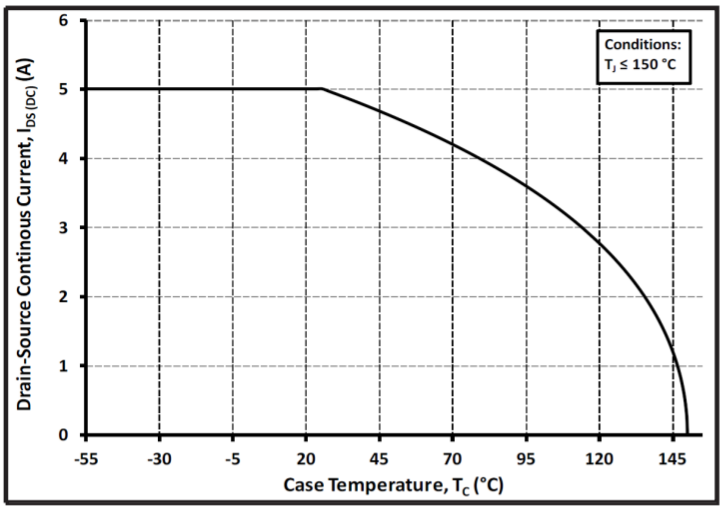


Figure 19. Continuous Drain Current Derating vs. Case Temperature

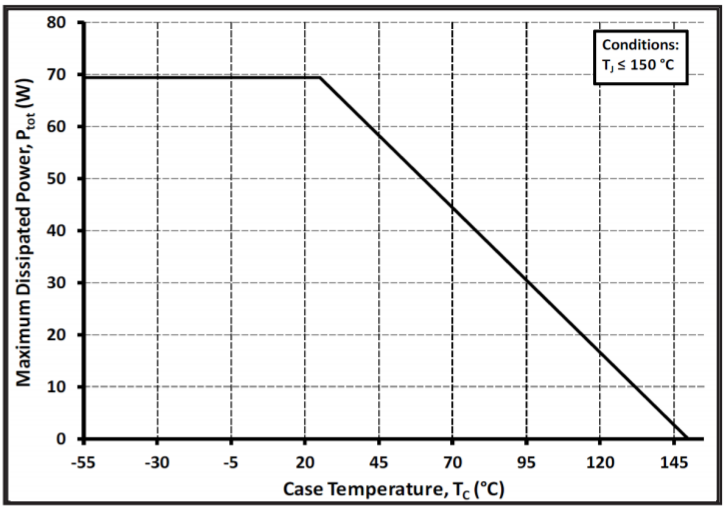


Figure 20. Maximum Power Dissipation Derating Vs Case Temperature

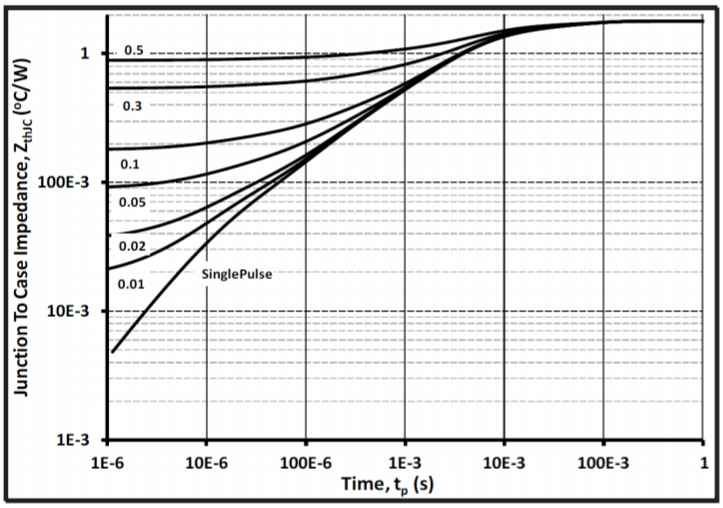


Figure 21. Transient Thermal Impedance (Junction - Case)

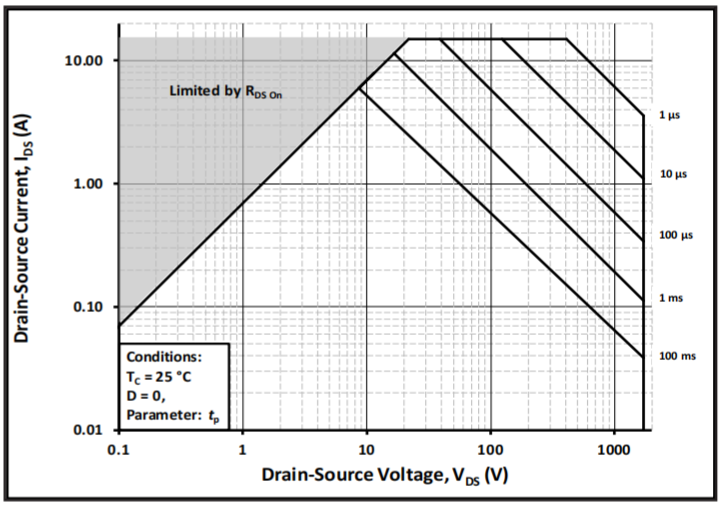


Figure 22. Safe Operating Area

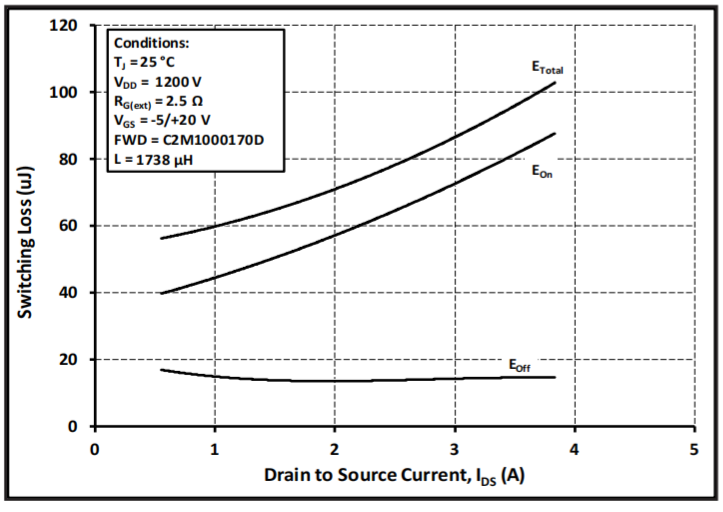


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 1200V)

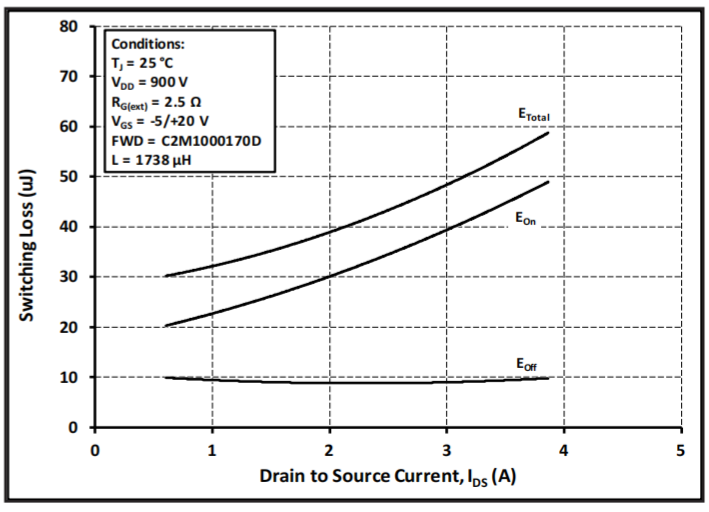


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 900 V)

Typical Performance

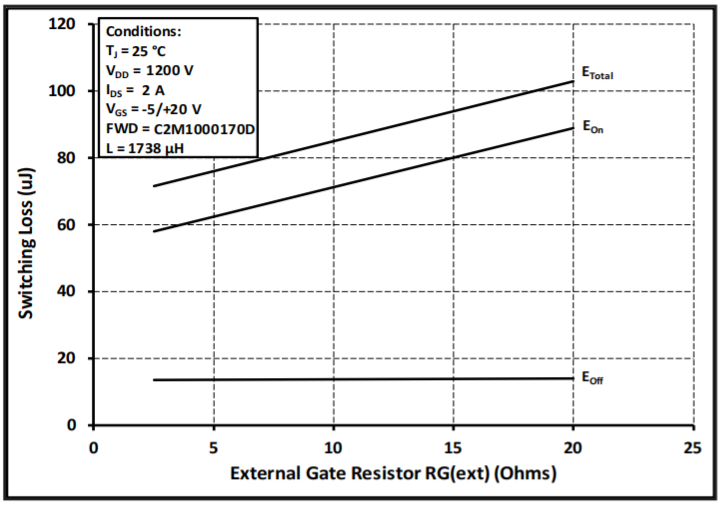


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

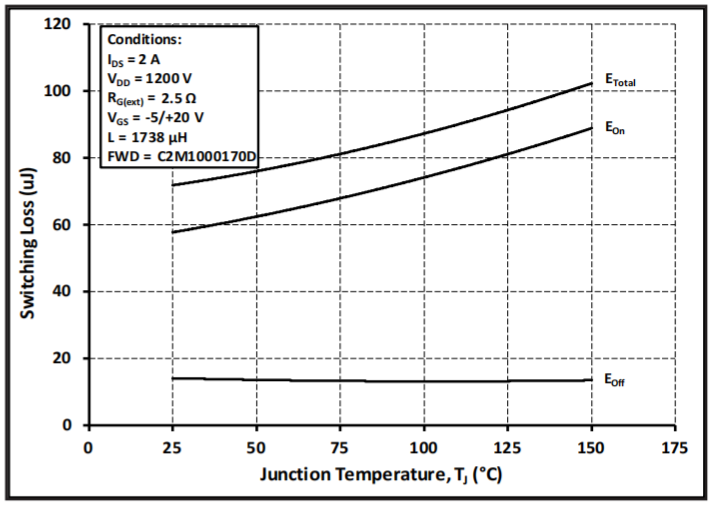


Figure 26. Clamped Inductive Switching Energy vs. Temperature

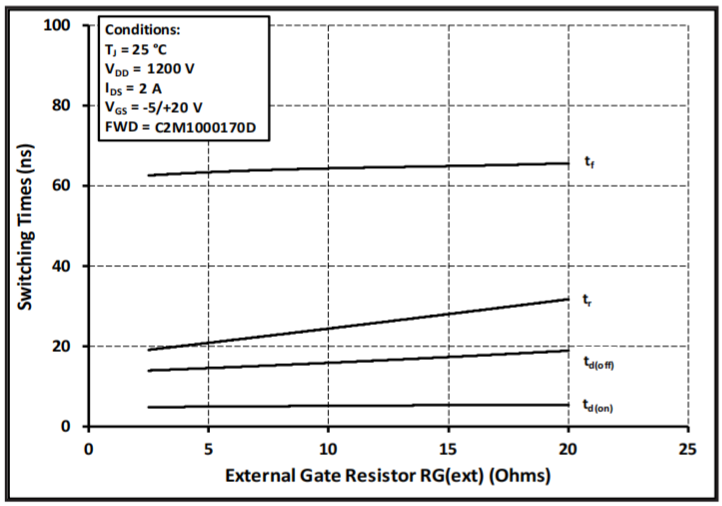


Figure 27. Switching Times vs. $R_{G(ext)}$

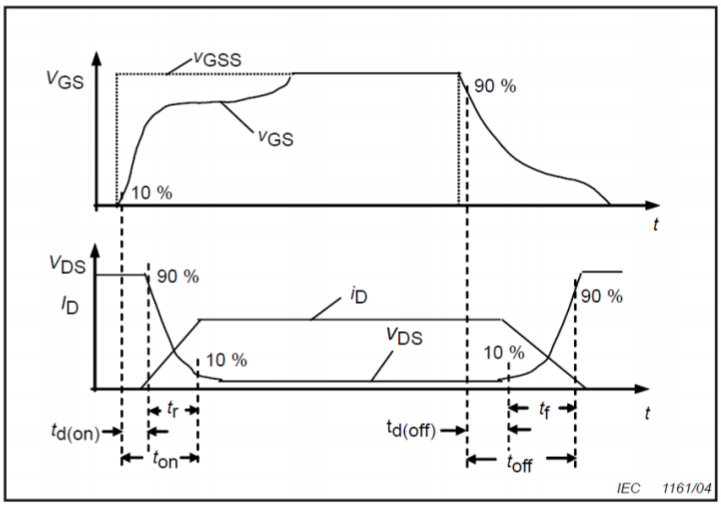


Figure 28. Switching Times Definition

Test Circuit Schematic

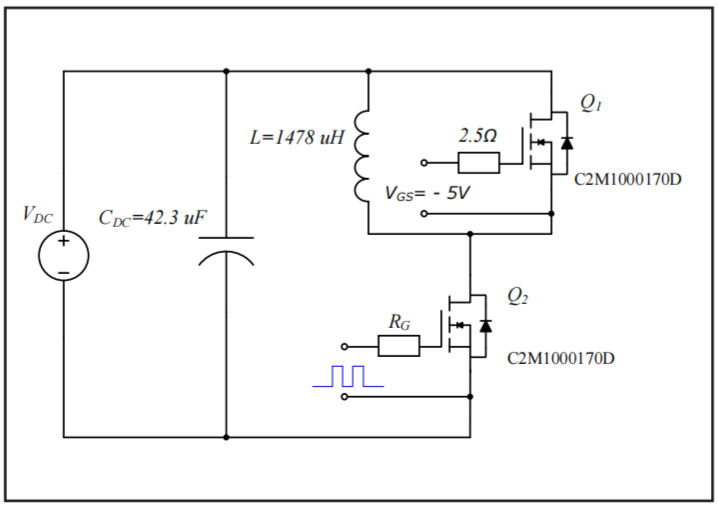


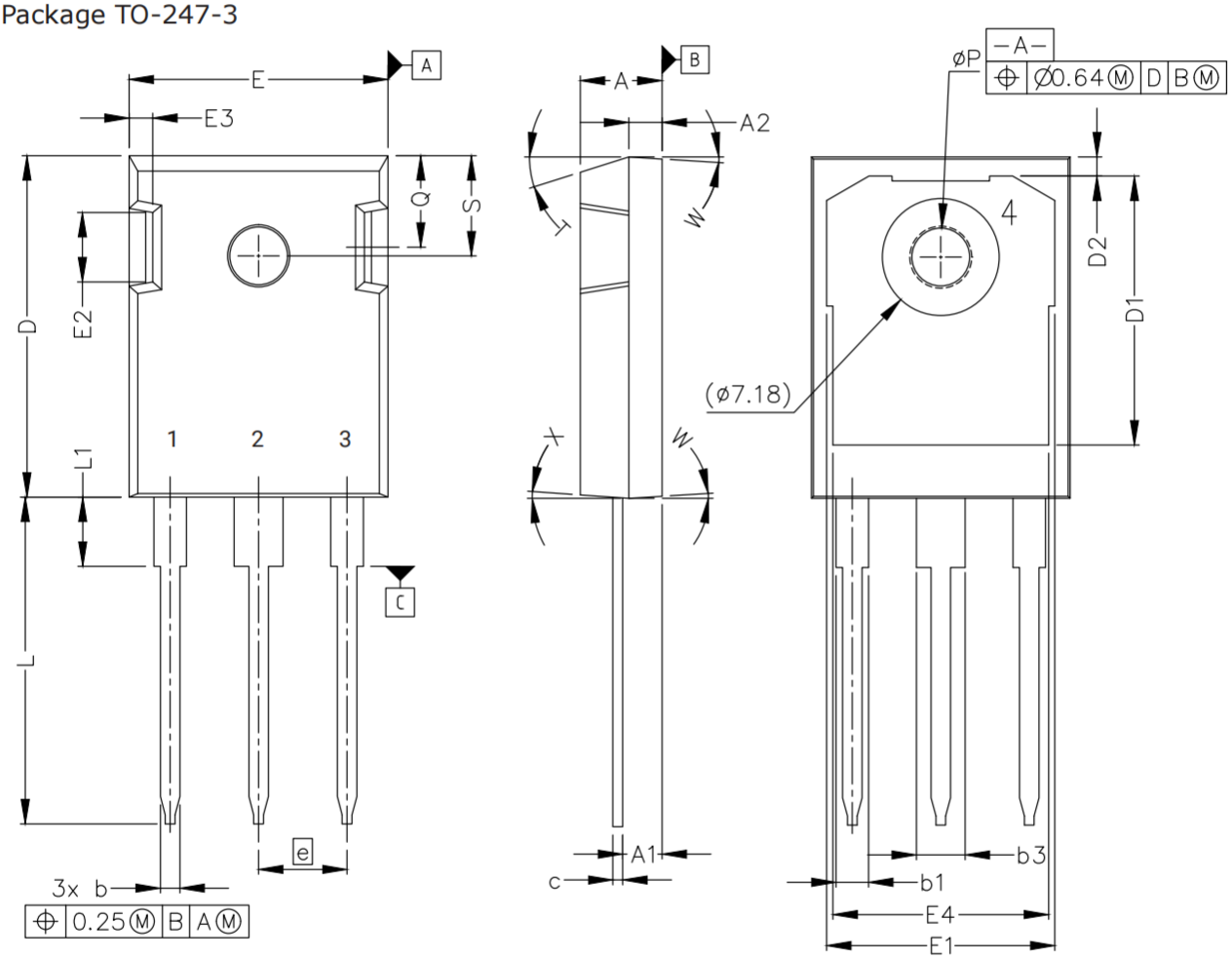
Figure 29. Clamped Inductive Switching Waveform Test Circuit

ESD Ratings

ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 4000V	3A (>4000V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Package Dimensions

Package TO-247-3



NOTE ;
1. ALL METAL SURFACES: TIN PLATED,EXCEPT AREA OF CUT
2. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THIS DRAWING WILL MEET ALL DIMENSIONS REQUIREMENT OF JEDEC outlines TO-247 AD.
5. DIMENSION DO NOT INCLUDE BURR OR MOLD FLASH.

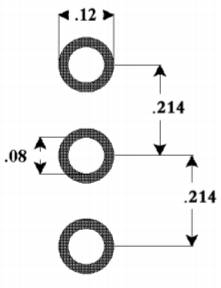
1 - GATE
2 - DRAIN (COLLECTOR)
3 - SOURCE (EMITTER)
4 - DRAIN (COLLECTOR)

Package Dimensions

Package TO-247-3

SYM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	.190	.205
A1	2.29	2.54	.090	.100
A2	1.91	2.16	.075	.085
b	1.07	1.33	.042	.052
b1	1.91	2.41	.075	.095
b3	2.87	3.38	.113	.133
c	0.55	0.68	.022	.027
D	20.80	21.10	.819	.831
D1	16.25	17.65	.640	.695
D2	0.95	1.25	.037	.049
E	15.75	16.13	.620	.635
E1	13.10	14.15	.516	.557
E2	3.68	5.10	.145	.201
E3	1.00	1.90	.039	.075
E4	12.38	13.43	.487	.529
e	5.44 BSC		.214 BSC	
N	3		3	
L	19.81	20.32	.780	.800
L1	4.10	4.40	.161	.173
ϕP	3.51	3.65	.138	.144
Q	5.49	6.00	.216	.236
S	6.04	6.30	.238	.248
T	17.5° REF.			
W	3.5° REF.			
X	4° REF.			

Recommended Solder Pad Layout



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