CSD95490Q5MC 同步降压 NexFET™ 智能功率级

1 特性

- 持续工作电流可达 75A
- 电流为 30A 时，系统效率大于 95%
- 工作频率高（高达 1.25MHz）
- 二极管仿真功能
- 温度补偿双向电流检测
- 模拟温度输出
- 故障监控
- 3.3V 和 5V 脉宽调制 (PWM) 信号兼容
- 三态 PWM 输入
- 集成自举开关
- 用于击穿保护的经优化死区时间
- 高密度 5mm × 6mm QFN 封装
- 超低电感封装
- 系统已优化的 PCB 封装
- 热增强型顶部散热
- 符合 RoHS 环保标准 – 无铅引脚镀层
- 无卤素

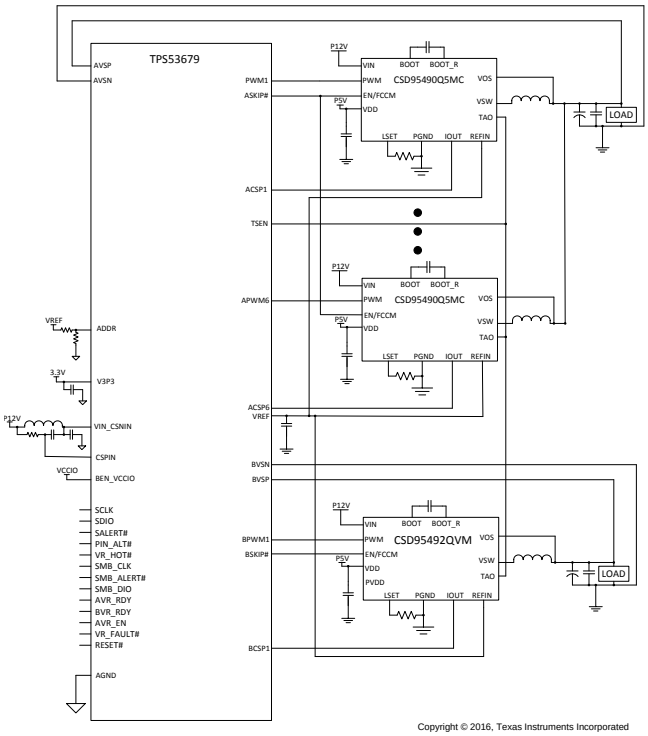
2 应用

- 多相位同步降压转换器
  - 高频 应用
  - 高电流、低占空比 应用
- 负载点 (POL) 直流/直流转换器
- 内存和图形卡
- 台式机和服务器 VR12.x / VR13 V-Core 同步降压转换器
- 用于网络通信的大电流 POL

3 说明

CSD95490Q5MC NexFET™功率器件是经过高度优化的设计，用于高功率、高密度场合的同步降压转换器。此产品集成了驱动器 IC 和功率 MOSFET 以实现功率级开关功能。该组合可在 5mm x 6mm 小型封装中实现高电流、高效率以及高速切换功能。它还集成了准确电流感测和温度感测功能，以简化系统设计并提高准确度。此外，PCB 封装已经过优化，可帮助减少设计时间并简化总体系统设计。

应用图表

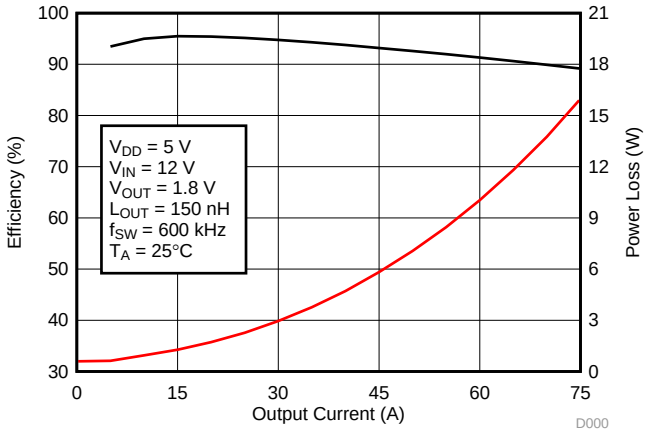


器件信息(1)

器件	包装介质	数量	封装	发货
CSD95490Q5MC	13 英寸卷带	2500	QFN 5.00mm × 6.00mm 封装	卷带封装
CSD95490Q5MCT	7 英寸卷带	250		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型功率级效率与功率损耗



目录

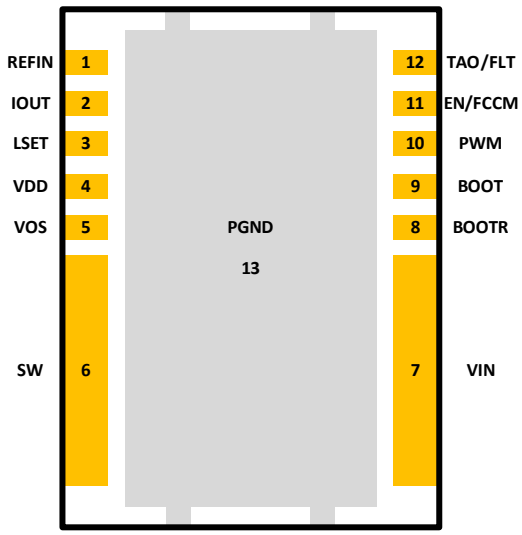
4 Revision History

Changes from Original (March 2017) to Revision A **Page**

- 更新了*机械制图* 部分 7

5 Pin Configuration and Functions

Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
REFIN	1	External reference voltage input for current sensing amplifier.
IOUT	2	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
LSET	3	A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.
VDD	4	Supply voltage for gate drivers and internal circuitry.
VOS	5	Output voltage sensing pin for the internal current sensing circuitry.
SW	6	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
VIN	7	Input voltage pin. Connect input capacitors close to this pin.
BOOTR	8	Return path for HS gate driver. It is connected to VSW internally.
BOOT	9	Bootstrap capacitor connection. Connect a minimum 0.1-µF, 16-V, X5R ceramic cap from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
PWM	10	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown hold-off time (t_{3HT}).
EN/FCCM	11	This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, Diode Emulation Mode (DEM) is enabled for sync FET. When the pin is high, device operates in Forced Continuous Conduction Mode (FCCM). When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.
TAO/FAULT	12	Temperature Amplifier Output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown, LSOC, or HSS detection circuit is tripped.
PGND	13	Power ground.

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise stated)(1)

		MIN	MAX	UNIT
	V_{IN} to P_{GND}	–0.3	20	V
	V_{IN} to V_{SW}	–0.3	20	V
	V_{IN} to V_{SW} (10 ns)		23	V
	V_{SW} to P_{GND}	–0.3	20	V
	V_{SW} to P_{GND} (10 ns)	–7	23	V
	V_{DD} to P_{GND}	–0.3	7	V
	EN/FCCM, TAO/FLT, LSET to P_{GND}(2)	–0.3	V_{DD} + 0.3	V
	IOUT, VOS, PWM to P_{GND}	–0.3	7	V
	REFIN	–0.3	3.6	V
	BOOT to BOOTR(2)	–0.3	V_{DD} + 0.3	V
	BOOT to P_{GND}	–0.3	30	V
T_J	Operating junction temperature	–55	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Should not exceed 7 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±500	

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise stated)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{DD}	Driver supply voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)		4.5	16	V
V_{OUT}	Output voltage			5.5	V
PWM	PWM to P_{GND}			V_{DD} + 0.3	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz(2)		75	A
I_{OUT-PK}	Peak output current(3)			105	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min), V_{OUT} = 2.5 V (max)		1250	kHz
	On-time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on-time		20		ns
	Operating junction temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10-µF (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 2. Peak output current is applied for t_p = 50 µs.

7 Application Schematic

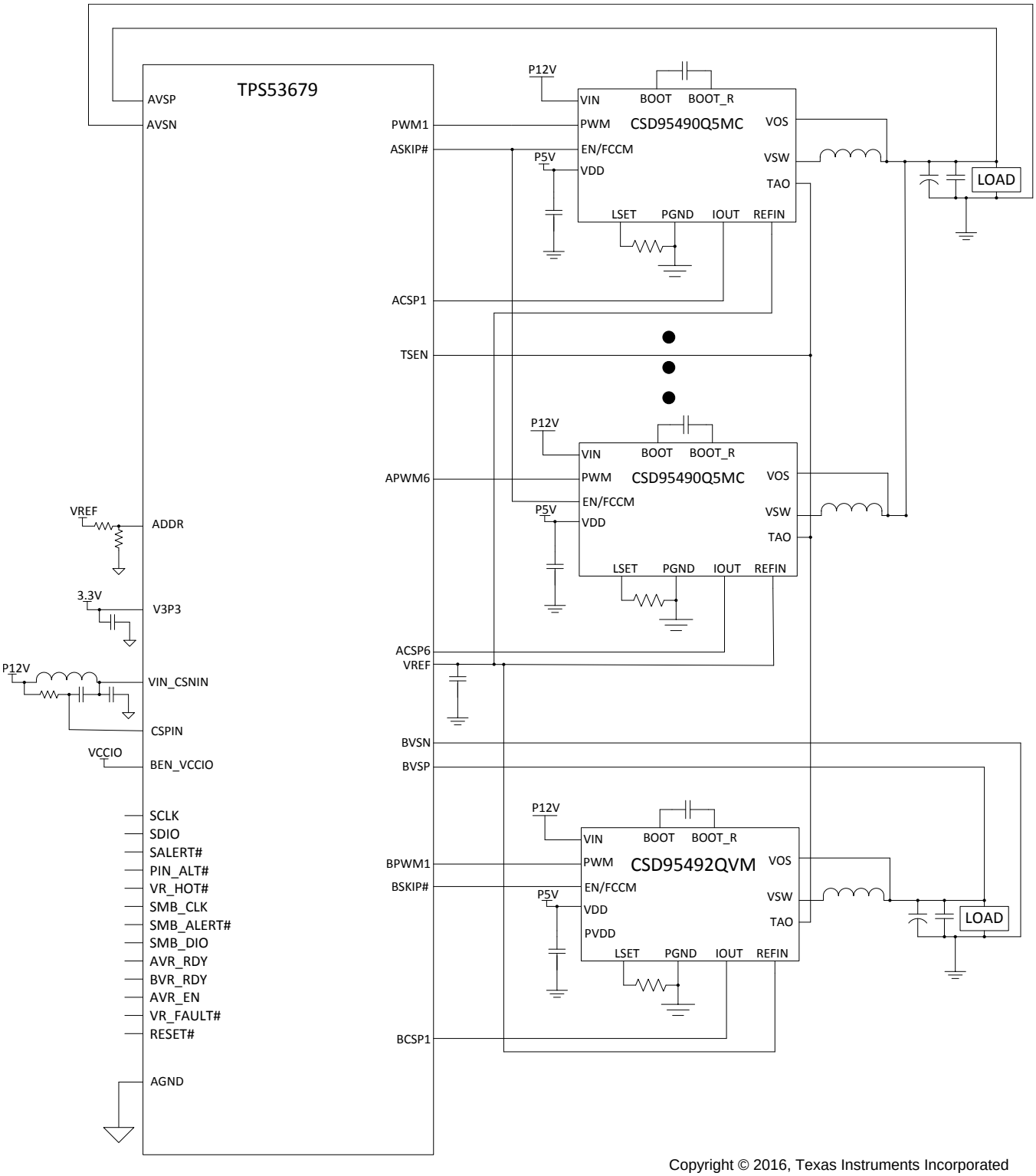


Figure 1. Application Schematic

Note: The schematic in Figure 1 is a conceptual drawing only. Actual designs may require additional components not shown.

8 器件和文档支持

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

8.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.5 Glossary

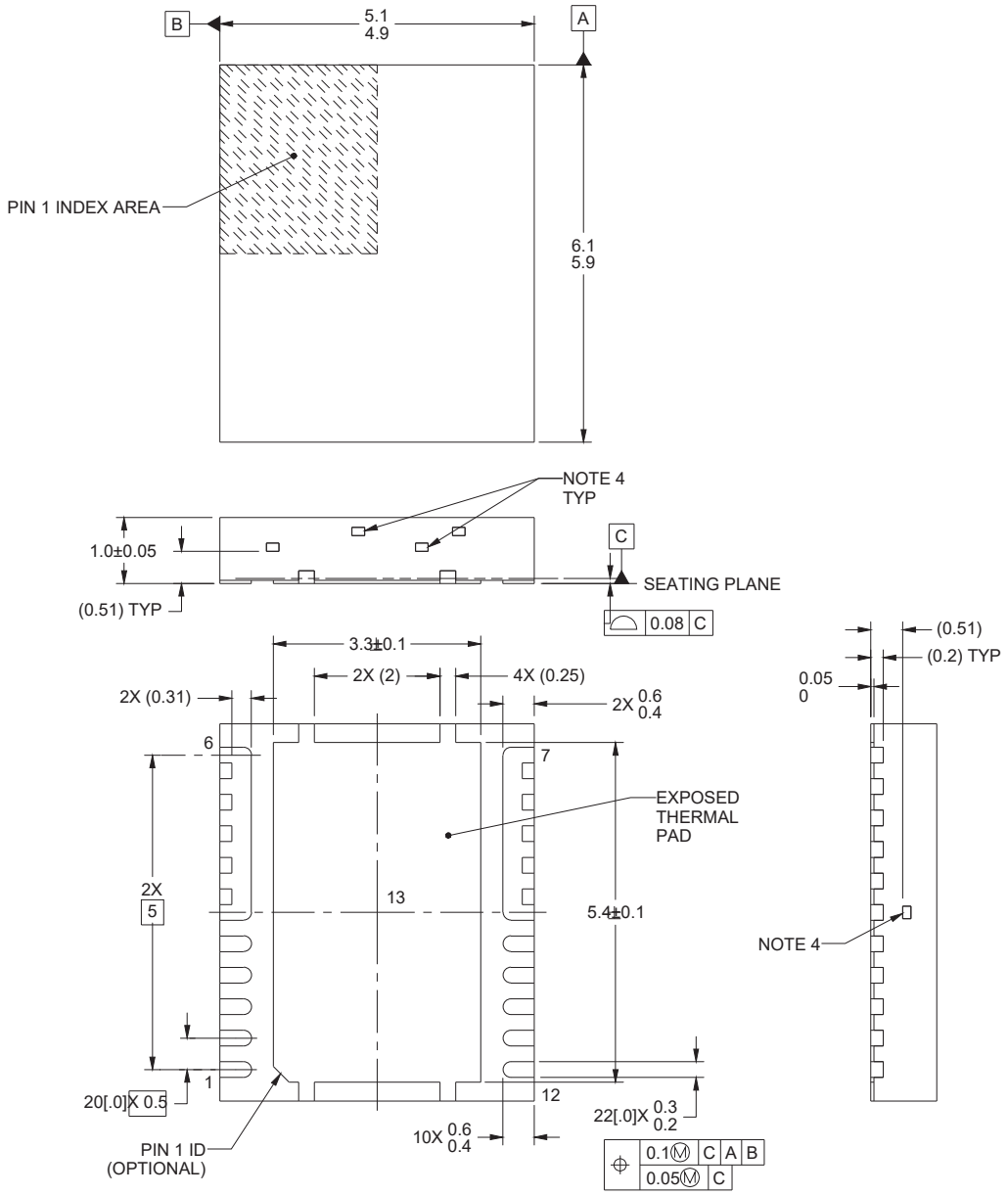
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

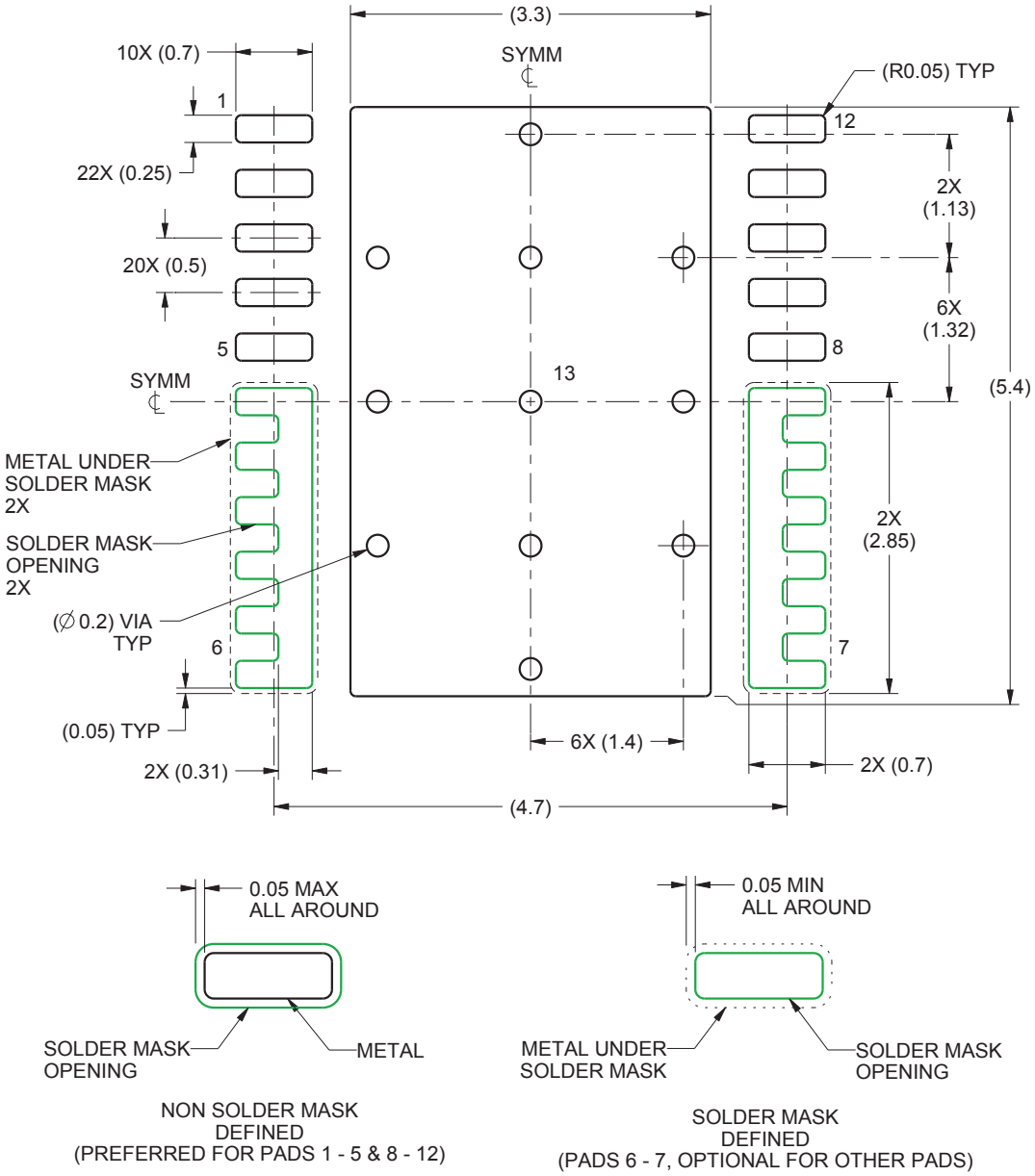
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

9.1 机械制图



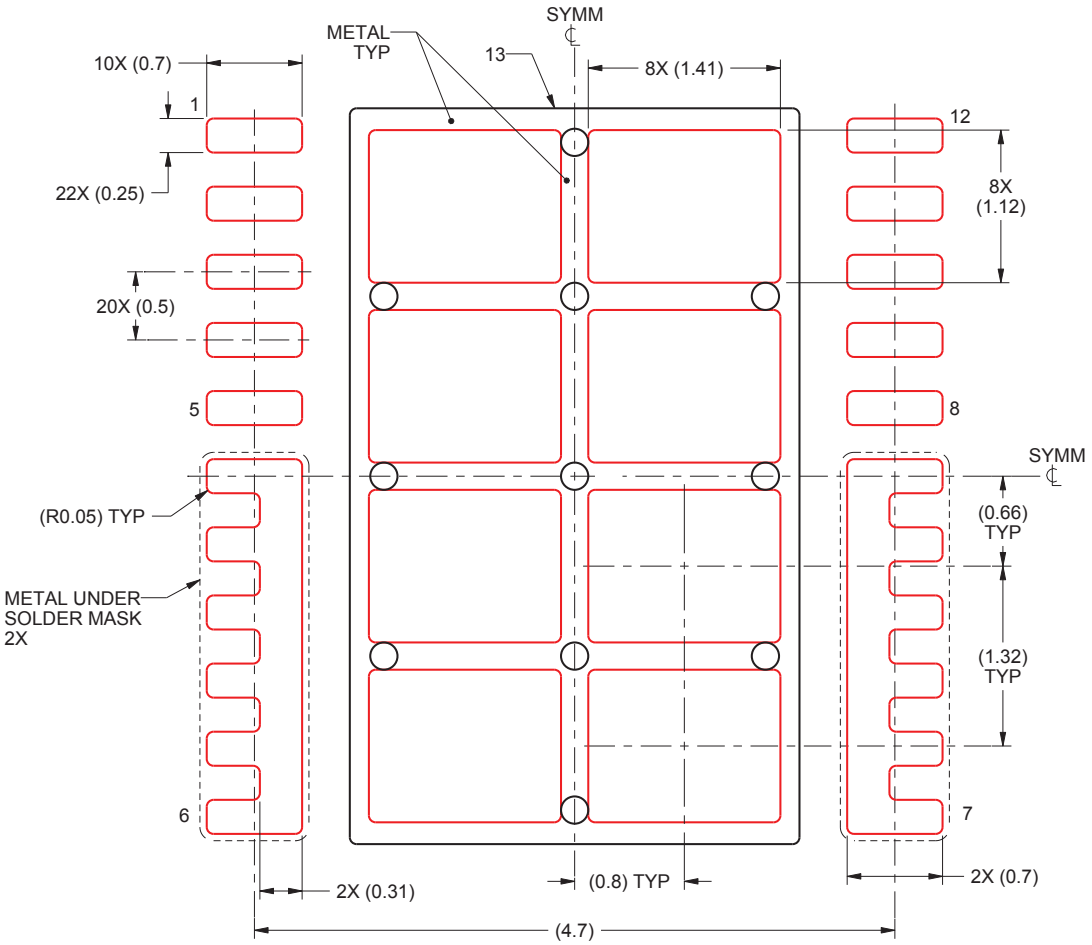
1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 封装散热盘必须在印刷电路板上焊接，包装散热和机械性能。
4. 外露的连接杆 特性 可能会有所不同。

9.2 推荐 PCB 焊盘图案



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 此封装设计用于焊接到电路板的散热焊盘上。有关更多信息，请参阅*《QFN/SON PCB 连接》*(SLUA271)。
4. 根据具体应用决定是否选用通孔，请参见器件数据表。如需实施任意通孔，请参见此视图上的通孔位置。建议对焊锡膏下方的通孔进行填充、堵塞或包覆。

9.3 建议模板开口



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95490Q5MC	NRND	Production	VSON-CLIP (DMC) | 12	2500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95490MC
CSD95490Q5MC.Z	NRND	Production	VSON-CLIP (DMC) | 12	2500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95490MC
CSD95490Q5MCT	NRND	Production	VSON-CLIP (DMC) | 12	250 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95490MC
CSD95490Q5MCT.Z	NRND	Production	VSON-CLIP (DMC) | 12	250 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95490MC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

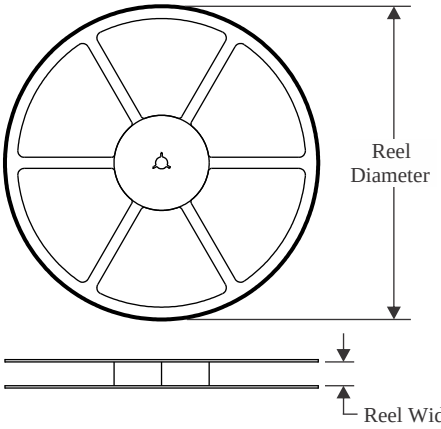
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

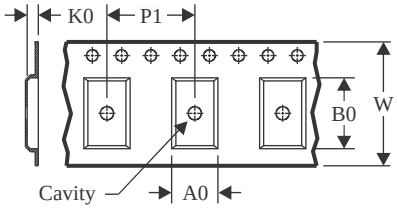
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

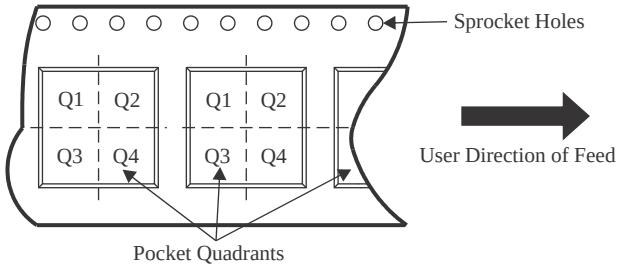


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

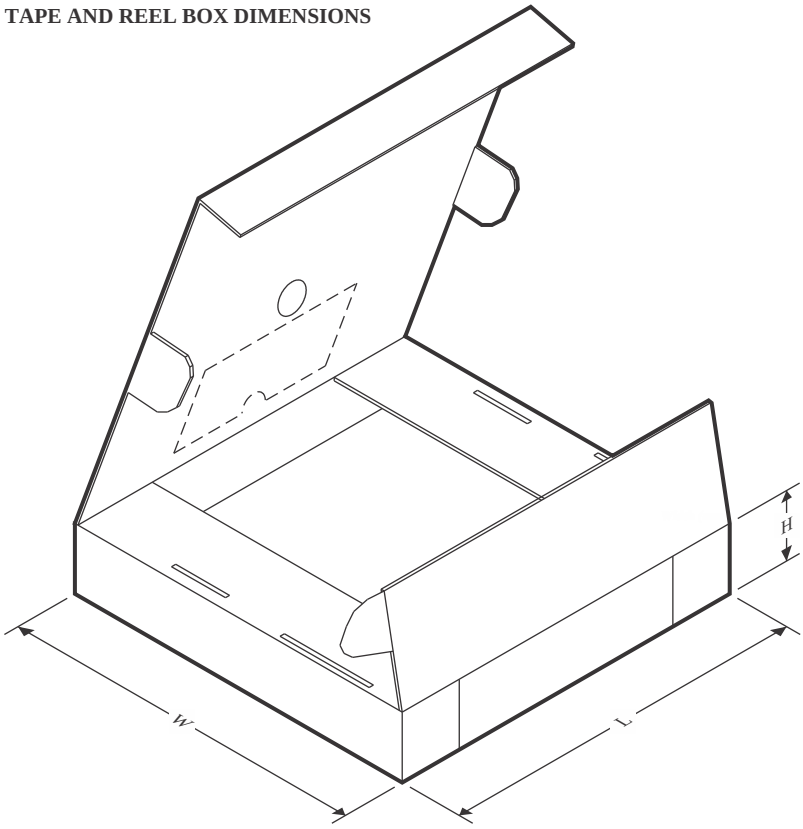
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95490Q5MC	VSON-CLIP	DMC	12	2500	330.0	12.4	5.3	6.3	1.2	8.0	12.0	Q1
CSD95490Q5MCT	VSON-CLIP	DMC	12	250	180.0	12.4	5.3	6.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95490Q5MC	VSON-CLIP	DMC	12	2500	367.0	367.0	38.0
CSD95490Q5MCT	VSON-CLIP	DMC	12	250	213.0	191.0	35.0

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265