Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

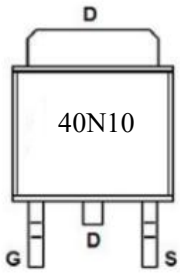
Bvdss	Rdson	ID
100V	20mΩ	40A

Application

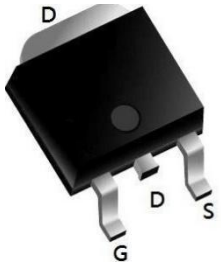
- PWM applications
- DC-DC Converters
- Synchronous-rectification applications

RoHS

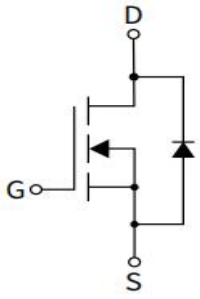
Package



Marking and pin assignment



TO252-3L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
40N10	S40N10	TO252-3L	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[5]	T_C = 25℃	I_D	40	A
	T_C = 100℃		16	A
Pulsed Drain Current[3]		I_{DM}	100	A
Avalanche Current[3,6]		I_{AS}	8	A
Single Pulsed Avalanche Energy[3,6]		EAS	16	mJ
Power Dissipation[2]	T_C = 25℃	P_D	27	W
Operating Junction Temperature Range		T_J	-55 ~ 150	℃
Storage Temperature Range		T_{STG}	-55 ~ 150	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance,Junction to Ambient[1,4]	$R_{\theta JA}$	62	℃/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.65	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS40N10	TO252-3L	1	2	3	Tape Reel

Electrical Characteristics (T_C=25℃,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	100	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1.2	1.8	2.6	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=15A	-	20	23	mΩ
		V_{GS}=4.5V, I_D=10A	-	-	33	
Forward Transconductance	gfs	V_{DS}=10V,I_D=20A	-	22	-	S
Gate Resistance	R_g	V_{DS}=V_{GS}=0V,f=1MHZ	-	1.62	-	Ω
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	822	-	pF
Output Capacitance	C_{oss}		-	310	-	
Reverse Transfer Capacitance	C_{rss}		-	23.5	-	
Total Gate Charge	Q_g	V_{DS}=50V, V_{GS}=10V, I_D=20A	-	22.7	-	nC
Gate-Source Charge	Q_{gs}		-	6.2	-	
Gate-Drain Charge	Q_{gd}		-	5.3	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=50V,I_D=20A, R_G=3Ω,V_{GS}=10V	-	15	-	ns
Rise Time	t_r		-	3.2	-	
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	
Fall Time	t_f		-	7.6	-	
Continuous Source Current	I_S	-	-	-	40	A

Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	0.88	1	V
Reverse Recovery Time	t_{rr}	I_F=20A,dI/dt=100A/μs	-	45	-	ns
Reverse Recovery Charge	Q_{rr}		-	59	-	nC

Notes:

1. The value of RθJC is measured in a still air environment with T_A =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
2. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case RθJC and case to ambient.
5. The maximum current rating is package limited.
6. The EAS data shows Max. rating. The test condition is V_{DS}=50V,V_{GS}=10V,L=0.5mH

Typical Performance Characteristics

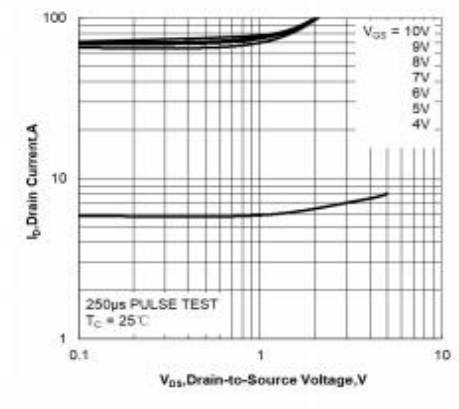


Figure 1. Output Characteristics

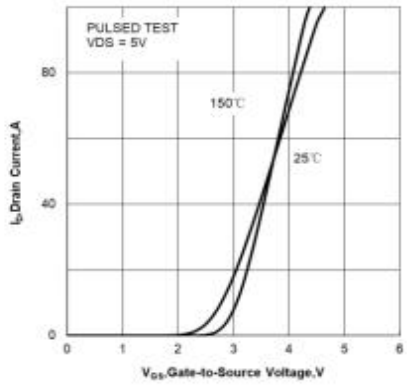


Figure 2. Transfer Characteristics

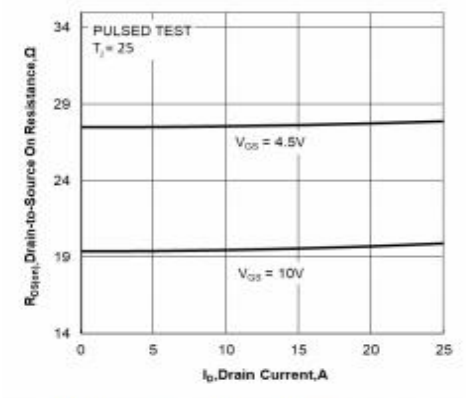


Figure 3. Drain-to-Source On Resistance vs Drain Current

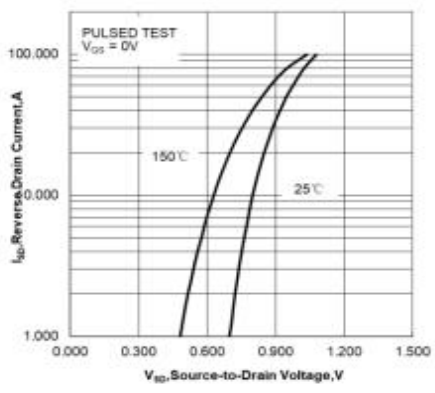


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

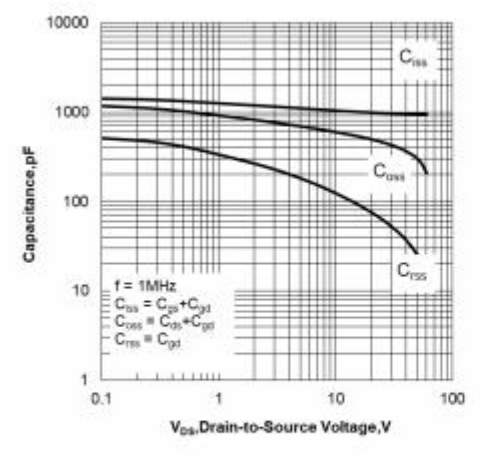


Figure 5. Capacitance Characteristics

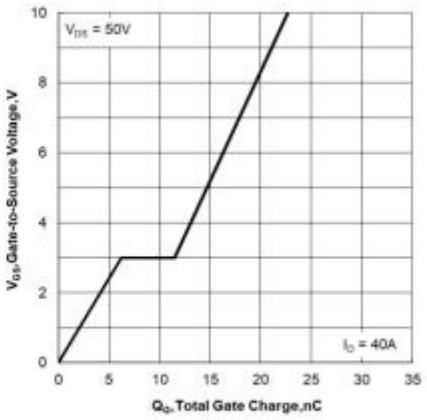


Figure 6. Gate Charge Characteristics

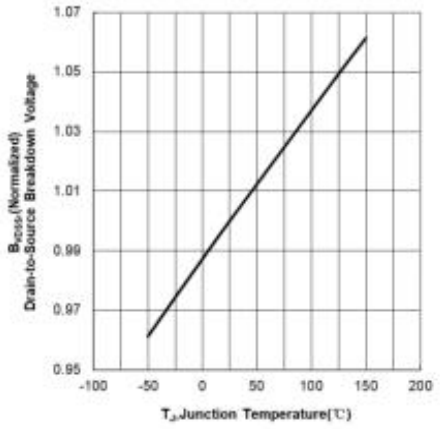


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

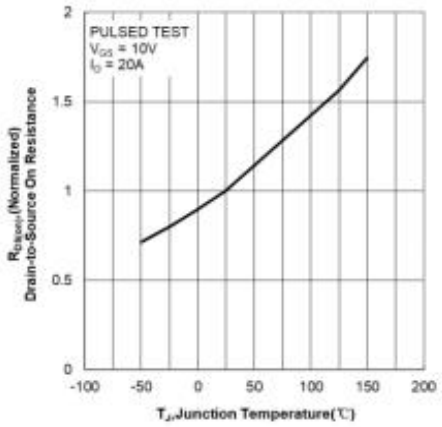


Figure 8. Normalized On Resistance vs Junction Temperature

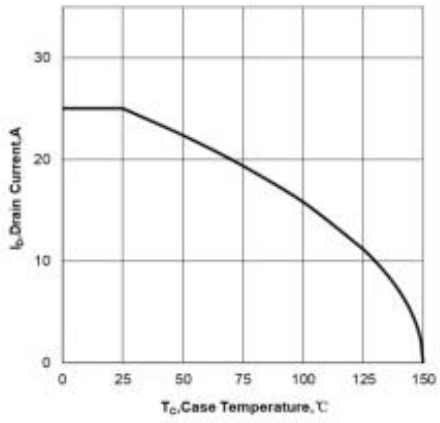


Figure 9. Maximum Continuous Drain Current vs Case Temperature

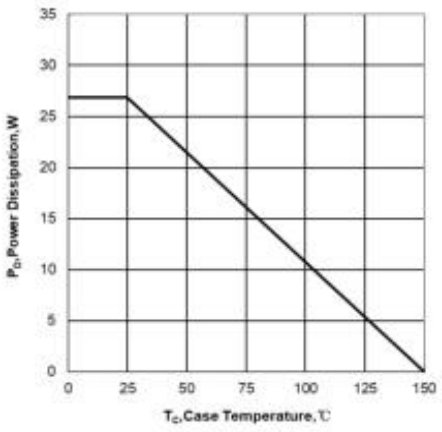


Figure 10. Maximum Power Dissipation vs Case Temperature

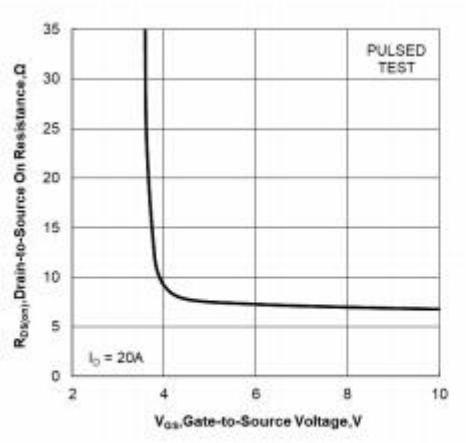


Figure11. Drain-to-Source On Resistance vs Gate

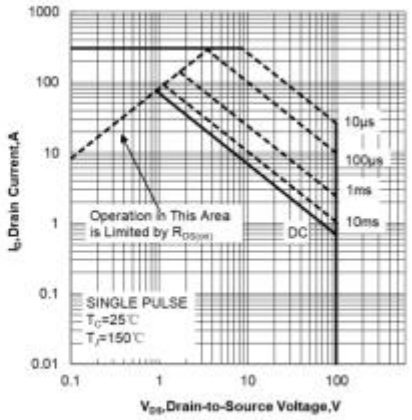


Figure 12. Maximum Safe Operating Area

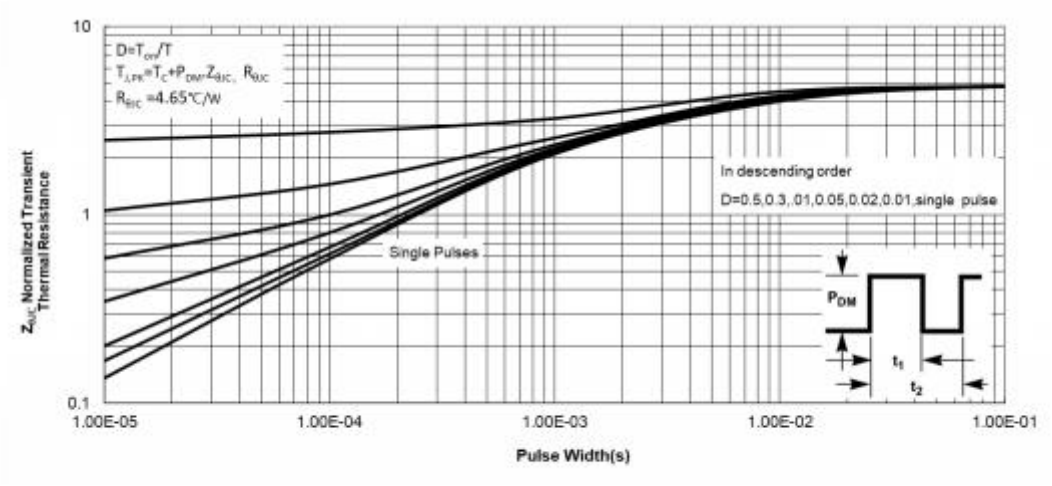
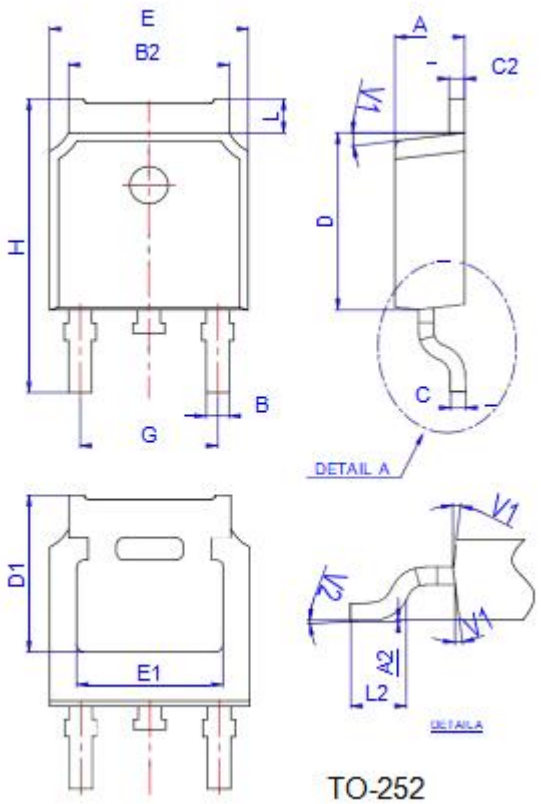


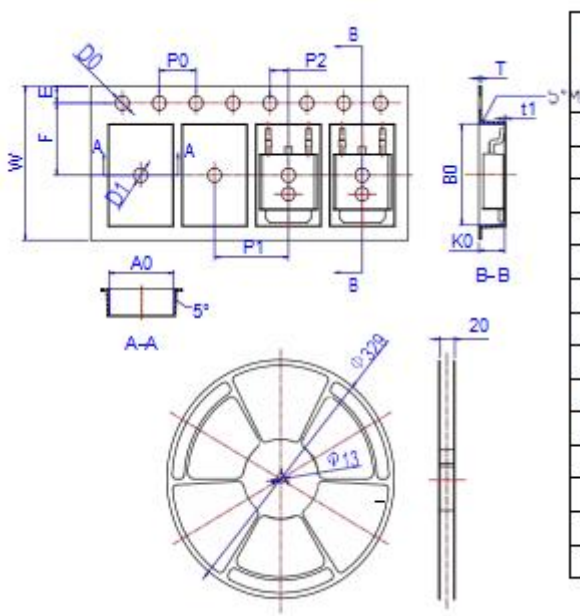
Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data TO252-3L



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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