74LVC1GX04

X-tal driver

Rev. 6 — 7 September 2023 | Product data sheet

1. General description

The 74LVC1GX04 is a crystal driver. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the Y output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power dissipation
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation at output Y
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1GX04GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74LVC1GX04GV	-40 °C to +125 °C	SC-74; TSOP6	plastic surface-mounted package; 6 leads	SOT457

nexperia

4. Marking

Table 2. Marking

Type number	Marking code[1]
74LVC1GX04GW	VX
74LVC1GX04GV	VX4

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

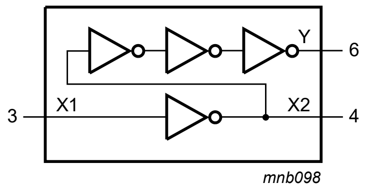
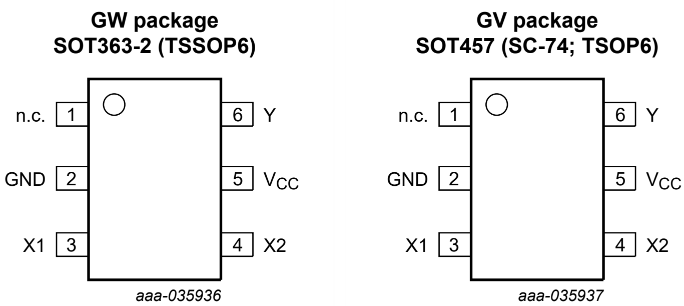


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
GND	2	ground (0 V)
X1	3	data input
X2	4	data output
V_{CC}	5	supply voltage
Y	6	data output

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output	
X1	**X2**	**Y**
H	L	H
L	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.
For SOT457 (SC-74; TSOP6) package: P_{tot} derates linearly with 4.1 mW/K above 89 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.65	-	5.5	V
V_I	input voltage			0	-	5.5	V
V_O	output voltage	Active mode	[2]	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V		0	-	5.5	V
T_{amb}	ambient temperature			-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V		-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V		-	-	10	ns/V

[1] For use of a regular crystal oscillator, the recommended minimum V_{CC} should be 2.0 V.
[2] Only for output Y.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 5.5 V		0.75V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 5.5 V		-	-	0.25V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V		-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V		-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V		-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V		-	-	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -100 μA; V_{CC} = 1.65 V to 5.5 V		V_{CC} - 0.1	-	-	V
		I_O = -4 mA; V_{CC} = 1.65 V		1.2	-	-	V
		I_O = -8 mA; V_{CC} = 2.3 V		1.9	-	-	V
		I_O = -12 mA; V_{CC} = 2.7 V		2.2	-	-	V
		I_O = -24 mA; V_{CC} = 3.0 V		2.3	-	-	V
		I_O = -32 mA; V_{CC} = 4.5 V		3.8	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND		-	±0.1	±1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	[2]	-	±0.1	±2	μA
I_{CC}	supply current	V_{CC} = 1.65 V to 5.5 V; I_O = 0 A; V_I = 5.5 V or GND;		-	0.1	4	μA
C_I	input capacitance			-	5.0	-	pF

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 5.5 V		0.8V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 5.5 V		-	-	0.2V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V		-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V		-	-	0.7	V
		I_O = 8 mA; V_{CC} = 2.3 V		-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.8	V
		I_O = 32 mA; V_{CC} = 4.5 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -100 μA; V_{CC} = 1.65 V to 5.5 V		V_{CC} - 0.1	-	-	V
		I_O = -4 mA; V_{CC} = 1.65 V		0.95	-	-	V
		I_O = -8 mA; V_{CC} = 2.3 V		1.7	-	-	V
		I_O = -12 mA; V_{CC} = 2.7 V		1.9	-	-	V
		I_O = -24 mA; V_{CC} = 3.0 V		2.0	-	-	V
		I_O = -32 mA; V_{CC} = 4.5 V		3.4	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND;		-	-	±1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	[2]	-	-	±2	μA
I_{CC}	supply current	V_{CC} = 1.65 V to 5.5 V; I_O = 0 A; V_I = 5.5 V or GND		-	-	4	μA

[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.
[2] V_O only for output Y.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 4.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	X1 to X2; see Fig. 2 [2]						
		V_{CC} = 1.65 V to 1.95 V	0.5	2.1	5.0	0.5	6.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.3	1.7	4.0	0.3	5.0	ns
		V_{CC} = 2.7 V	0.3	2.5	4.5	0.3	5.6	ns
		V_{CC} = 3.0 V to 3.6 V	0.3	2.1	3.7	0.3	4.5	ns
		V_{CC} = 4.5 V to 5.5 V	0.3	1.6	3.0	0.3	3.8	ns
		X1 to Y; see Fig. 3						
		V_{CC} = 1.65 V to 1.95 V	1.0	4.4	10.0	1.0	12.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.9	6.0	0.5	7.5	ns
		V_{CC} = 2.7 V	0.5	3.0	6.0	0.5	7.5	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.8	5.5	0.5	6.9	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	2.3	4.5	0.5	5.6	ns
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}; output enabled [3]	-	35	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

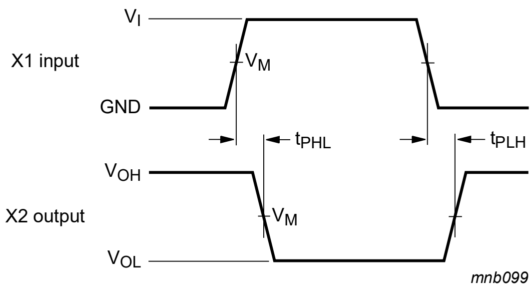
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

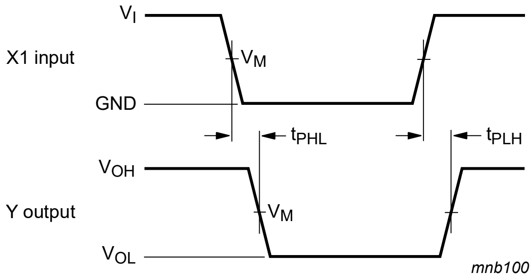
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 2. Input X1 to output X2 propagation delay times



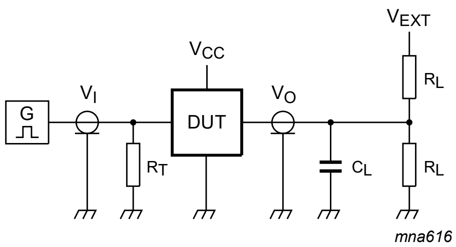
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Input X1 to output Y propagation delay times

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 10.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

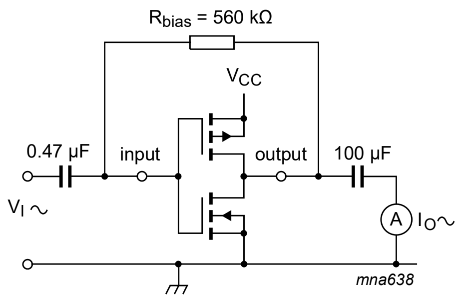
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 4. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

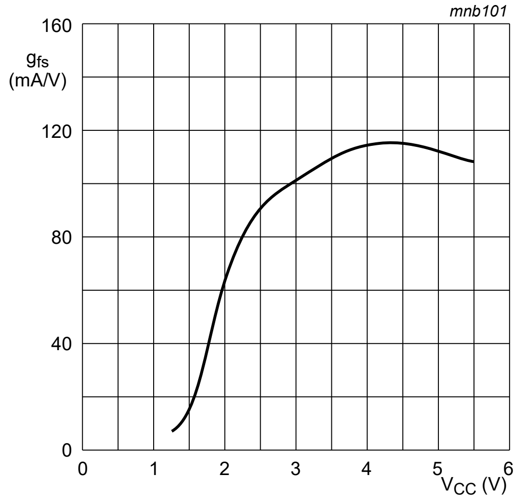


$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz.

V_O is constant.

Fig. 5. Test set-up for measuring forward transconductance



T_{amb} = 25 °C

Fig. 6. Typical forward transconductance as a function of supply voltage

12. Application information

Crystal controlled oscillator circuits are widely used in clock pulse generators because of their excellent frequency stability and wide operating frequency range. The 74LVC1GX04 provides the additional advantages of low power dissipation, stable operation over a wide range of frequency and temperature, and a very small footprint. This application information describes crystal characteristics, design and testing of crystal oscillator circuits based on the 74LVC1GX04.

12.1. Crystal characteristics

Fig. 7 is the equivalent circuit of a quartz crystal.

The reactive and resistive component of the impedance of the crystal alone and the crystal with a series and a parallel capacitance is shown in Fig. 8

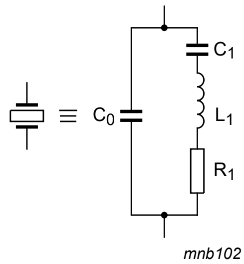
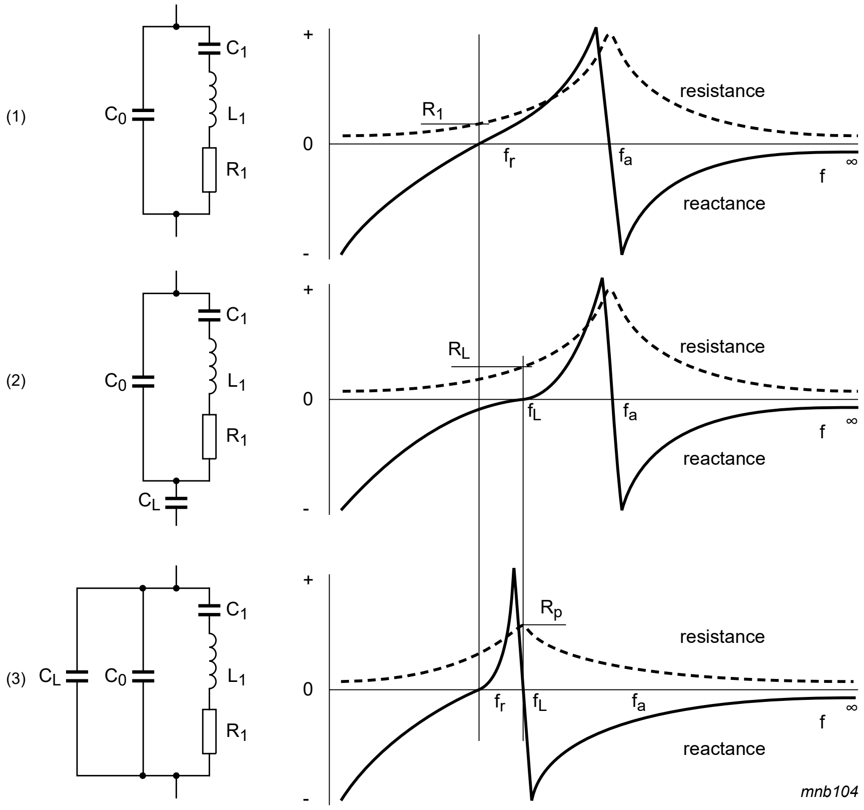


Fig. 7. Equivalent circuit of a crystal



(1) resonance
(2) anti-resonance
(3) load resonance

Fig. 8. Reactance and resistance characteristics of a crystal

12.1.1. Design

Fig. 9 shows the recommended way to connect a crystal to the 74LVC1GX04. This circuit is basically a Pierce oscillator circuit in which the crystal is operating at its fundamental frequency. The parallel load capacitance of C_1 and C_2 tune the circuit. C_1 and C_2 are in series with the crystal and they should be equal (approximately). R_1 is the drive-limiting resistor. It is set to approximately the same value as the reactance of C_1 at the crystal frequency ($R_1 = X_{C1}$). This setting results in an input to the crystal of 50 % of the rail-to-rail output of X2. It keeps the drive level into the crystal within drive specifications and the designer should verify it. Overdriving the crystal can cause damage.

The feedback resistor (R_f = 1 MΩ) provides negative feedback. It sets a bias point of the inverter near mid-supply, operating the 74LVC1GU04 portion in the high gain linear region.

To calculate the values of C_1 and C_2, the designer can use the formula:

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_s$$

C_L is the load capacitance as specified by the crystal manufacturer. C_s is the stray capacitance of the circuit (for the 74LVC1GX04 it is equal to an input capacitance of 5 pF).

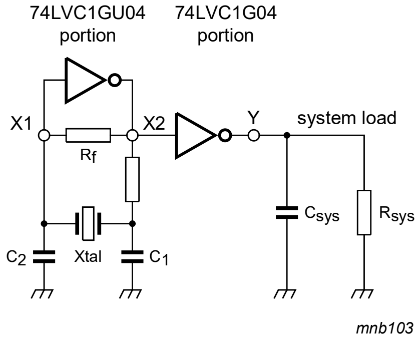


Fig. 9. Crystal oscillator configuration for the 74LVC1GX04

12.1.2. Testing

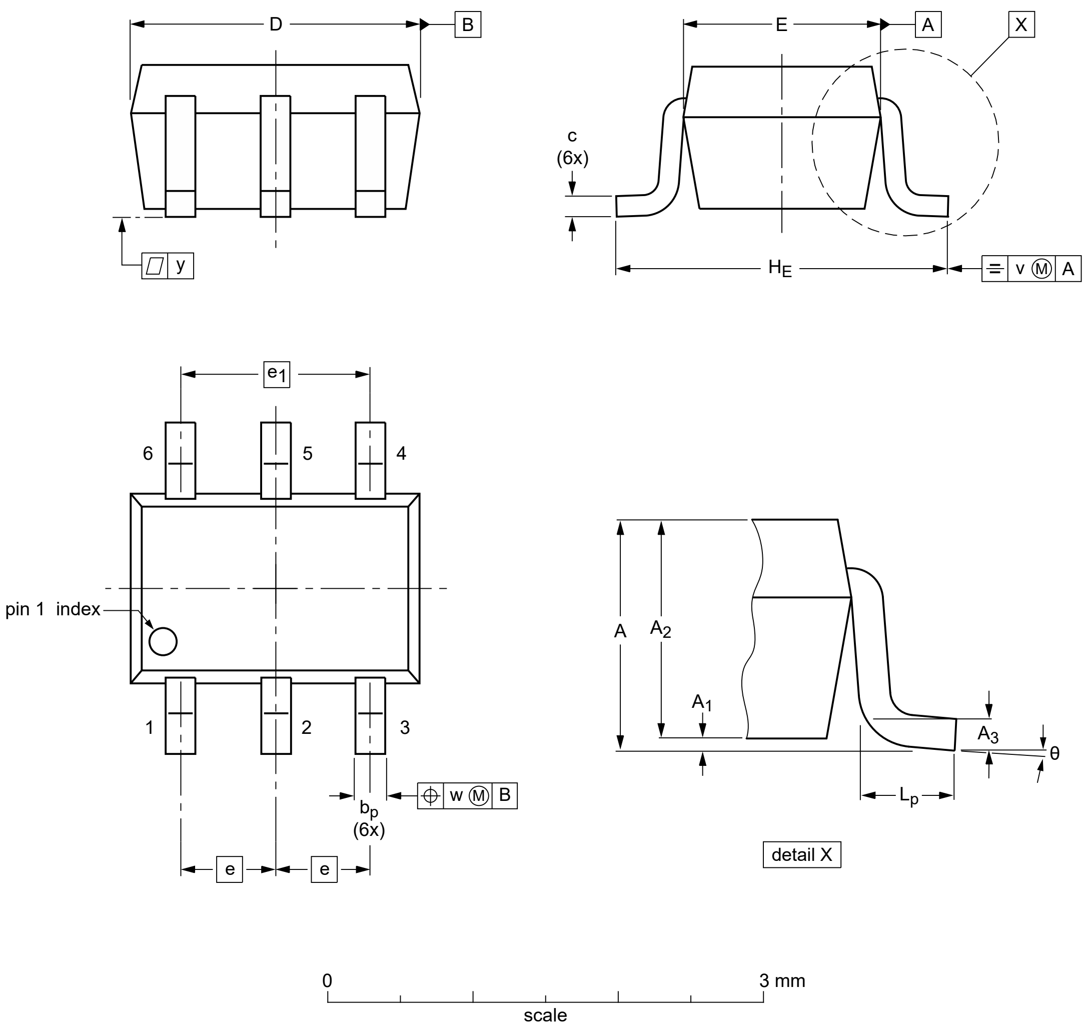
After the calculations are performed for a particular crystal, the oscillator circuit should be tested. The following simple checks verify the prototype design of a crystal controlled oscillator circuit. Perform the checks after laying out the board:

- Test the oscillator over worst-case conditions (lowest supply voltage, worst-case crystal and highest operating temperature). Adding series and parallel resistors can simulate a worst-case crystal.
- Insure that the circuit does not oscillate without the crystal.
- Check the frequency stability over a supply range greater than that which is likely to occur during normal operation.
- Check that the start-up time is within system requirements.

As the 74LVC1GX04 isolates the system loading, once the design is optimized, the single layout may work in multiple applications for any given crystal.

13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm **SOT363-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

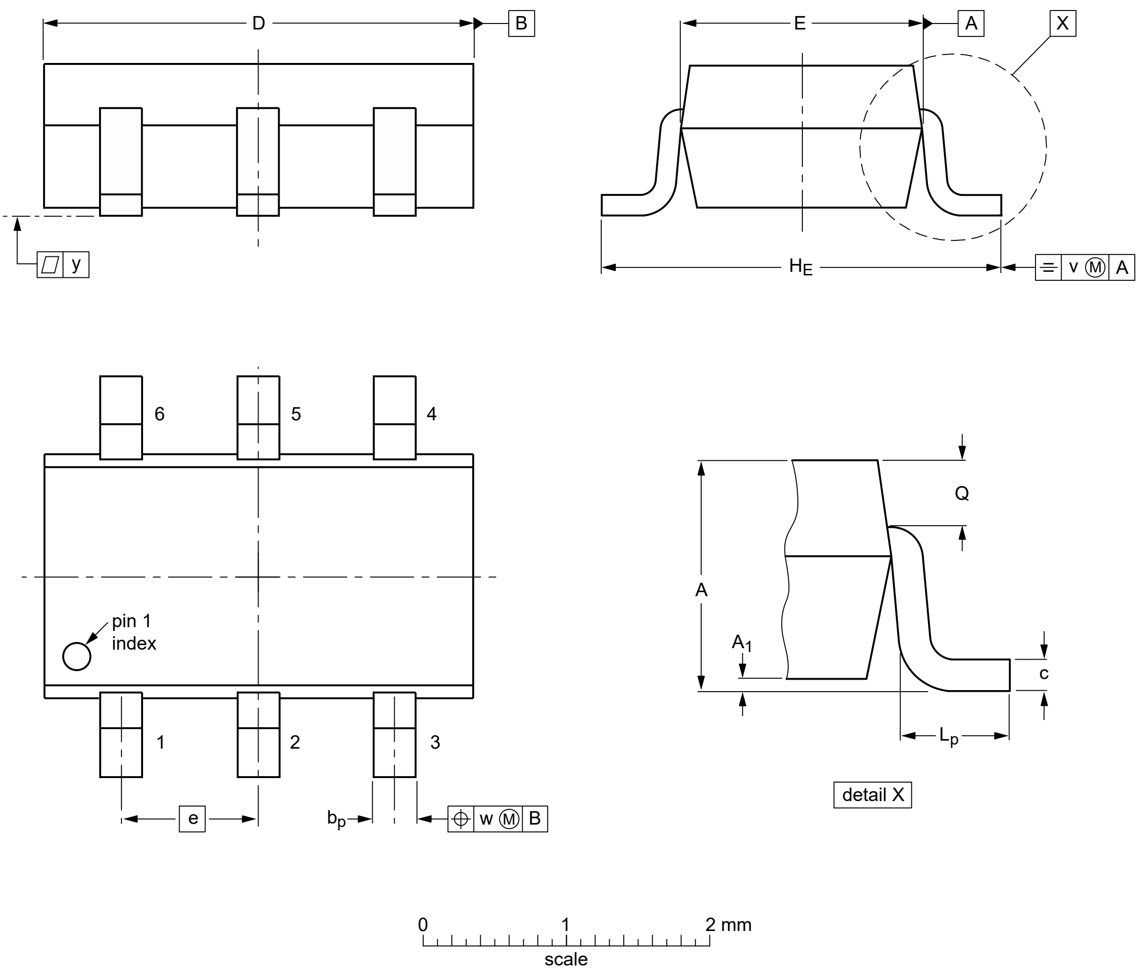
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot363-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT363-2		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 10. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads **SOT457**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	max	1.1	0.1	0.40	0.26	3.1	1.7		3.0	0.6	0.33			
	nom							0.95				0.2	0.2	0.1
	min	0.9	0.013	0.25	0.10	2.7	1.3		2.5	0.2	0.23			

sot457_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~06-03-16~~ 18-11-27

Fig. 11. Package outline SOT457 (SC-74; TSOP6)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1GX04 v.6	20230907	Product data sheet	-	74LVC1GX04 v.5
Modifications:	• Section 1 and Section 2 updated.			
74LVC1GX04 v.5	20220126	Product data sheet	-	74LVC1GX04 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). • Section 1 and Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated. • Fig. 11: Package outline drawing SOT457 (SC-74; TSOP6) has been updated.			
74LVC1GX04 v.4	20161212	Product data sheet	-	74LVC1GX04 v.3
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1GX04 v.3	20130821	Product data sheet	-	74LVC1GX04 v.2
Modifications:	• Table 2: Table note added.			
74LVC1GX04 v.2	20130819	Product data sheet	-	74LVC1GX04 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 10 Changed: Conditions for input leakage and supply current.			
74LVC1GX04 v.1	20030813	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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