4-Channel SMBus and I²C Switch

Features

- Compatible with SMBus and I²C communication protocols
- Support multi-channel bidirectional data transmission:

  PCA9546: supports 4-channel downstream slaves
- With active low reset pin $\overline{\text{RESET}}$: PCA9546
- With slave address selection pin:

  PCA9546: 3 address selection pins
- Allow data transfer across voltage domains
- Low on-resistance, low idle current
- Supply voltage: 1.65V ~ 5.5V
- Support hot-swappable devices

Applications

- Servers
- Routers
- I²C Devices with slave address conflicts

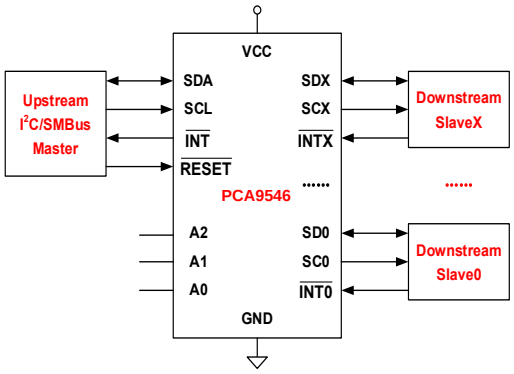
Description

The PCA9546 series are a 4-channel bidirectional data transmission switch controlled by the I²C bus. The upstream host selects one or more downstream slaves through the SCL and SDA pins of the chip and performs specified data transmission. PCA9546 series support selecting any combination of downstream channel slaves.

PCA9546 provide a low-active reset pin $\overline{\text{RESET}}$. If the I²C bus of a downstream slave is locked, the $\overline{\text{RESET}}$ pin can be pulled low to reset the PCA9546 series, thereby no longer selecting the downstream slave and releasing the locked I²C bus.

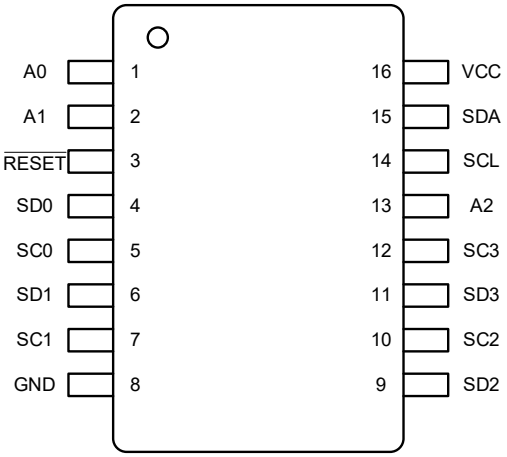
The PCA9546 series allow the upstream host and downstream slave to transfer data across voltage domains. At this time, the power supply voltage VCC of the PCA9546 series limits the minimum voltage V_{PASS} allowed for upstream and downstream transmission. This function allows upstream and downstream devices to interact with each other in the 1.8V, 3.3V, and 5.0V voltage domains without additional protection. When using this function, it is necessary to ensure that the I²C bus of each upstream and downstream channel is connected to the respective power supply voltage by the pull-up resistor RP. The withstand voltage value of all pins of the PCA9546 series is 5.5V.

Figure 1 Diagram of PCA9546 Series Application

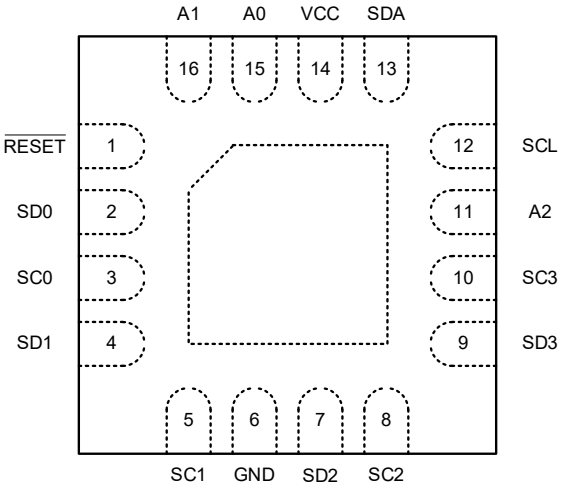


Pin Configuration and Functions

PCA9546 16-PIN TSSOP/SOP Top View



PCA9546 16-PIN QFN Top View



Pin Functions of Package TSSOP / SOP

PIN		DESCRIPTION
NAME	NO.	
	PCA9546	
A0	1	Slave address pin 0, can be connected to VCC or GND
A1	2	Slave address pin 1, can be connected to VCC or GND
A2	13	Slave address pin 2, can be connected to VCC or GND
$\overline{\text{RESET}}$	3	Active low reset input pin. Connect to VCC or V_{DPUM} through a pull-up resistor, if not used.
$\overline{\text{INT0}}$	/	Active low interrupt input pin 0. Connect to V_{DPU0} through a pull-up resistor.
SD0	4	Serial data pin 0. Connect to V_{DPU0} through a pull-up resistor.
SC0	5	Serial clock pin 0. Connect to V_{DPU0} through a pull-up resistor.
$\overline{\text{INT1}}$	/	Active low interrupt input pin 1. Connect to V_{DPU1} through a pull-up resistor.
SD1	6	Serial data pin 1. Connect to V_{DPU1} through a pull-up resistor.
SC1	7	Serial clock pin 1. Connect to V_{DPU1} through a pull-up resistor.
GND	8	Ground.
$\overline{\text{INT2}}$	/	Active low interrupt input pin 2. Connect to V_{DPU2} through a pull-up resistor.
SD2	9	Serial data 2. Connect to V_{DPU2} through a pull-up resistor.
SC2	10	Serial clock 2. Connect to V_{DPU2} through a pull-up resistor.
$\overline{\text{INT3}}$	/	Active low interrupt input pin 2. Connect to V_{DPU2} through a pull-up resistor.
SD3	11	Serial data 3. Connect to V_{DPU3} through a pull-up resistor. SC2 10 8 Serial clock 2. Connect to VDPU2 (1) through a pull-up resistor
SC3	12	Serial clock 3. Connect to V_{DPU3} through a pull-up resistor. SC2 10 8 Serial clock 2. Connect to VDPU2 (1) through a pull-up resistor
$\overline{\text{INT}}$	/	Active low interrupt output pin, connected to V_{DPUM} through a pull-up resistor.
SCL	14	Serial clock pin. Connect to V_{DPUM} through a pull-up resistor.
SDA	15	Serial data pin. Connect to V_{DPUM} through a pull-up resistor.
VCC	16	Power supply.

Pin Functions of Package QFN

PIN		DESCRIPTION
NAME	NO.	
	PCA9546	
A0	**15**	Slave address pin 0, can be connected to VCC or GND
A1	**16**	Slave address pin 1, can be connected to VCC or GND
A2	**11**	Slave address pin 2, can be connected to VCC or GND
$\overline{\text{RESET}}$	**1**	Active low reset input pin. Connect to VCC or V_{DPUM} through a pull-up resistor, if not used.
$\overline{\text{INT0}}$	**/**	Active low interrupt input pin 0. Connect to V_{DPU0} through a pull-up resistor.
SD0	**2**	Serial data pin 0. Connect to V_{DPU0} through a pull-up resistor.
SC0	**3**	Serial clock pin 0. Connect to V_{DPU0} through a pull-up resistor.
$\overline{\text{INT1}}$	**/**	Active low interrupt input pin 1. Connect to V_{DPU1} through a pull-up resistor.
SD1	**4**	Serial data pin 1. Connect to V_{DPU1} through a pull-up resistor.
SC1	**5**	Serial clock pin 1. Connect to V_{DPU1} through a pull-up resistor.
GND	**6**	Ground.
$\overline{\text{INT2}}$	**/**	Active low interrupt input pin 2. Connect to V_{DPU2} through a pull-up resistor.
SD2	**7**	Serial data 2. Connect to V_{DPU2} through a pull-up resistor.
SC2	**8**	Serial clock 2. Connect to V_{DPU2} through a pull-up resistor.
$\overline{\text{INT3}}$	**/**	Active low interrupt input pin 2. Connect to V_{DPU2} through a pull-up resistor.
SD3	**9**	Serial data 3. Connect to V_{DPU3} through a pull-up resistor. SC2 10 8 Serial clock 2. Connect to VDPU2 (1) through a pull-up resistor
SC3	**10**	Serial clock 3. Connect to V_{DPU3} through a pull-up resistor.
$\overline{\text{INT}}$	**/**	Active low interrupt output pin, connected to V_{DPUM} through a pull-up resistor.
SCL	12	Serial clock pin. Connect to V_{DPUM} through a pull-up resistor.
SDA	13	Serial data pin. Connect to V_{DPUM} through a pull-up resistor.
VCC	14	Power supply.

Note: In the above table, VCC is the power supply voltage of the PCA9546 series V_{DPUM} is the power supply voltage of the upstream host, and V_{DPU3} ~ V_{DPU0} are the power supply voltages of the downstream channel 3 ~ channel 0 slaves.

Specifications

Absolute Maximum Ratings

	MIN	MAX	UNIT
Supply voltage VCC	-0.5	7	V
Input pin voltage V_I	-0.5	7	V
Input current I_I		±20	mA
Output current I_O		±25	mA
Continuous current through VCC/GND pin		±100	mA
Total power consumption		400	mW
Operating temperature range	-40	85	℃
Storage temperature range	-60	150	℃

Unless otherwise specified, the specifications in the above table apply within the atmospheric temperature range.

Stresses beyond the range may cause permanent damage to the device.

ESD Ratings

		Value	UNIT
Electrostatic Discharge Voltage VESD	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±8000	V
	Machine Mode (MM), per JEDEC-STD Classification	±100	V
Latch-up Effect	Latch-Up, per JESD 78, Class IA	±200	mA

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage VCC		1.65		5.5	V
High-level input V_{IH}	SCL，SDA	0.7*VCC		6	V
	A2，A1，A0，$\overline{INTX}$,$\overline{RESET}$	0.7*VCC		VCC+0.5	
Low-level input V_{IL}	SCL，SDA	-0.5		0.3*VCC	V
	A2，A1，A0，$\overline{INTX}$,$\overline{RESET}$	-0.5		0.3*VCC	
Operating temperature range		-40		85	℃

Unless otherwise specified, the specifications in the above table apply within the atmospheric temperature range.

Electrical Characteristics

Unless otherwise specified, the following data are characteristics of the chip at +25℃ and the power supply voltage IS in the range of 1.65 V to 5.5 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-on reset voltage V_{PORR}	No load, V_I = VCC/GND		1.20	1.50	V
Power-off reset voltage V_{PORF}	No load, V_I = VCC/GND	0.80	1.05		V
VCC when transmitting across voltage domains	V_{PASS}=1V, R_P=4.7kohm (1)			2.2	V
	V_{PASS}=1.8V, R_P=4.7kohm			3.2	
	V_{PASS}=2.5V, R_P=4.7kohm			4.1	
	V_{PASS}=3.3V, R_P=4.7kohm			5.1	
Low-level output current I_{OL}	SDA / $\overline{INT}$, V_{OL}=0.4V		6.5		mA
	SDA / $\overline{INT}$, V_{OL}=0.6V		9.7		
Bus communication frequency F_{SCL}		1		400	kHz
On-resistance R_{ON}	V_O=0.4V, I_O=10mA, VCC=1.8V		52		ohm
	V_O=0.4V, I_O=10mA, VCC=3.3V		10		
	V_O=0.4V, I_O=10mA, VCC=5.5V		7		
	V_O=0.4V, I_O=15mA, VCC=3.3V		10		
	V_O=0.4V, I_O=15mA, VCC=5.5V		7		
Working current I_{CC}	VCC=1.65V, F_{SCL}=100kHz		2		μA
	VCC=3.3V, F_{SCL}=100kHz		4		
	VCC=5.5V, F_{SCL}=100kHz		10		
	VCC=1.65V, F_{SCL}=400kHz		3		
	VCC=3.3V, F_{SCL}=400kHz		6		
	VCC=5.5V, F_{SCL}=400kHz		17		
	VCC=1.65V, SCL=SDA=VDPUM		0.4	0.6	
	VCC=2.7V, SCL=SDA=VDPUM		0.7	1.1	
	VCC=3.3V, SCL=SDA=VDPUM		1.0	1.3	
	VCC=5.5V, SCL=SDA=VDPUM		1.6	2	
$\overline{RESET}$ Pin reset pulse time	PCA9546	20			ns

Note: (1) For details on data transmission across voltage domains, see Section 7.2.3 ;

(2) R_P is the pull-up resistor of the corresponding channel. Here the pull-up resistor values of all channels are equal in default.

Detailed Description

I²C Serial Interface

Bus Overview

I²C interface uses the serial data line SDA and the serial clock line SCL to achieve bidirectional data transmission between different IC devices. Both the SDA and SCL buses need to be connected to the power line through a pull-up resistor R_P. Data transmission only occurs when the bus is not occupied (SDA=SCL=1). In the I²C interface protocol, only one data bit is transmitted during each SCL clock pulse; during the high level of the clock pulse, the data on the SDA bus must remain stable, and any changes in the SDA bus will be recognized as controlling signals. When the bus is not occupied and the SCL bus is high, the change of the SDA bus from high level to low level is defined as start condition, and the change of the SDA bus from low level to high level is defined as stop condition, as shown in Figure 2.

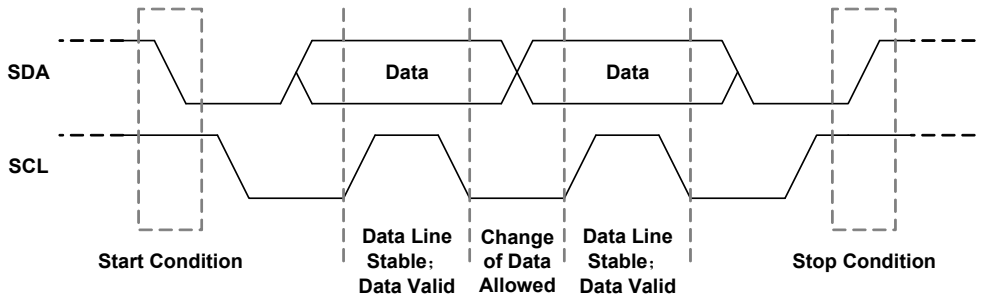


Figure 2. Start Condition, Stop Condition, and Data Bit Transmission in I²C Communication

During I²C communication, a device generating a message is a transmitter and receiving is the receiver. The device that controls the message is the master, and that are controlled by the master are the slaves.

Between the start condition and the stop condition, the data bytes transmitted between the host and the slave are not restricted, and each data byte (8 bits) must be followed by an ACK bit. When the host sends data to the slave, after sending a byte, the host must release the SDA bus so that the slave to respond to the data can pull down the SDA bus to generate an ACK bit and successfully respond to the sent byte. When the slave returns data to the host, the SDA bus also needs to be released after the slave returns a byte so that the host can generate an ACK bit to successfully respond to the returned data byte. During the high pulse of the ninth SCL clock when sending ACK, the SDA bus must maintain a stable low level, and the setup time and hold time of the I²C communication protocol should be met here.

When the slave returns the last byte to the host, the host must send a NACK bit, releases the SDA bus and pulls it high. After that, the host generates a termination condition, and the data transmission ends.

Control Register

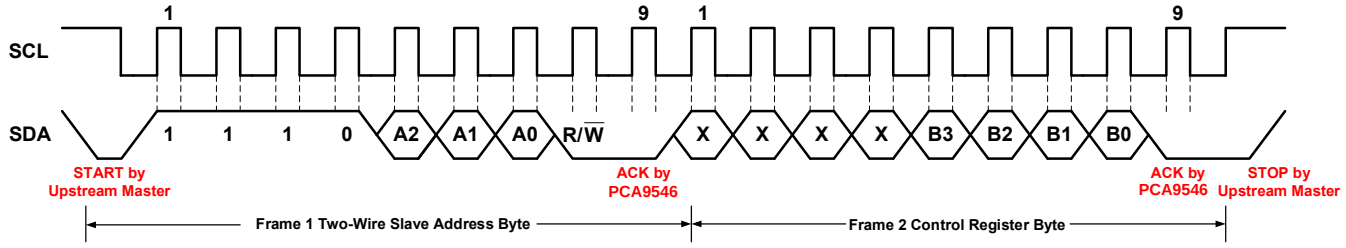


Figure 3 Diagram of Control Register Write Operation

During the use of the chip, the upstream host can configure the Control register inside the PCA9546 to determine the data transmission between the upstream host and one or more downstream slaves. Figure 3 shows the diagram of the upstream host's write operation to the Control register. The upstream host first sends a slave address byte with LSB=0 (i.e., read/write bit $R/\overline{W}=0$) to address the corresponding PCA9546 on the bus.The last 2/3 bits of the slave address byte are address selection bits. PCA9546 can be configured with a total of 8 different slave addresses through A2, A1 and A0 bits. The values of A2, A1 and A0 bits are determined by the connection relationship of the chip's A2, A1 and A0 address pins; if the corresponding address pin is connected to the power supply voltage, the value of the corresponding address bit is 1; if the corresponding address pin is connected to the ground voltage, the value is 0.

After the addressed PCA9546 successfully responds to the slave address byte, the upstream host continues to send the Control register configuration byte; PCA9546, the upper 4 bits of this byte are not writable.

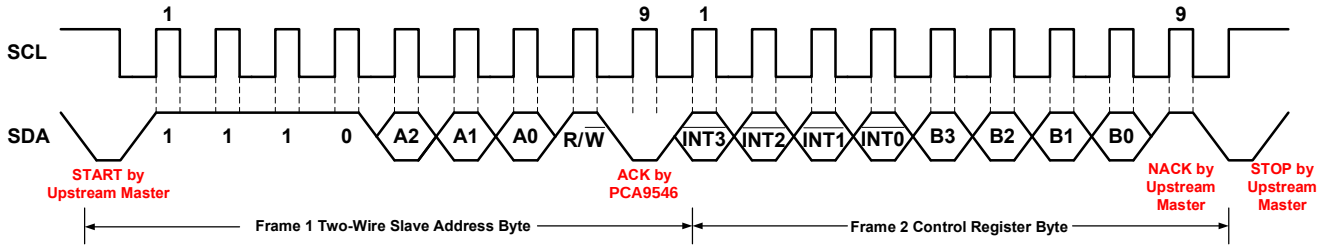


Figure 4 Diagram of Control Register Read Operation

Figure 4 shows a diagram of the upstream host performing a read operation on the Control register of the for PCA9546 , $\overline{INT3}=\overline{INT2}=\overline{INT1}=\overline{INT0}=0$.

Table 1 gives the bit description of the lower four bits of the Control register of the PCA9546 series These four bits are read-write bits and are used to control the data transmission between the upstream slave and one or more downstream channel slaves. When a bit in B3~B0 is written to 1, the switch between the SDX and SCX buses of the corresponding downstream channel slave and the SDA and SCL buses of the upstream host will be opened at the Stop Condition when the write operation to the Control register ends.

Table 1 The definition of the lower 4 bits of Control register

Series	B3	B2	B1	B0	Description
PCA9546	X	X	X	0	Channel 0 Close
				1	Channel 0 Open
	X	X	0	X	Channel 1 Close
			1		Channel 1 Open
	X	0	X	X	Channel 2 Close
		1			Channel 2 Open
	0	X	X	X	Channel 3 Close
	1				Channel 3 Open

Device Functional Modes

Power-On Reset

When the power supply voltage of the VCC pin of the PCA9546 series is powered on, the Control register and I²C state machine inside the chip remain in the initial state. At this time, all downstream channels are in the closed state, all bits in the Control register are reset to 0, and the chip's $\overline{INT}$ pins are pulled high to 1. The above initial state will be maintained until VCC＞V_{PORR}, after which the PCA9546 series will perform corresponding functions according to actual usage. When the power supply voltage of the VCC pin decreases to VCC＜V_{PORF}, the PCA9546 series will be reset to the initial state again.

RESETN

The active-low reset pin $\overline{RESET}$ of PCA9546 can be used to globally reset the chip when meeting a bus-fault condition. To ensure smooth chip reset, the low pulse time applied to the $\overline{RESET}$ pin must be more than 20ns. When the reset pin is not needed, please connect the pin to the power supply voltage through a pull-up resistor to prevent accidental chip reset.

Data Transmission Across Voltage Domains

The PCA9546 allow the upstream host and the downstream channel slaves to transmit data across voltage domains. At this time, the power supply voltage VCC of the series limits the lowest voltage allowed for upstream and downstream transmission. This function can achieve data interaction between upstream and downstream without additional protection in the 1.8V, 3.3V, and 5.0V voltage domains. When using this function, it is necessary to ensure that the I²C bus of each upstream and downstream channel is connected to the required power supply voltage through the pull-up resistor R_P, as shown in Figure 5.

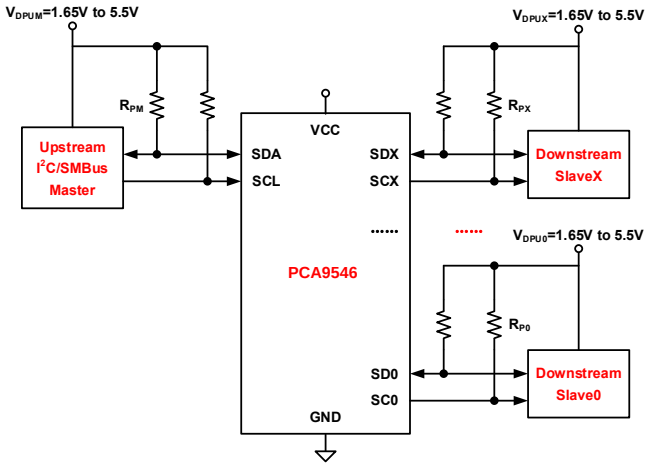


Figure 5 Diagram of Data Transmission Across Voltage Domains

In Figure 5, the power supply voltage of the upstream host is V_{DPUM}, and the supply voltage of each downstream channel slave is $V_{DPUX;}$ SDA and SCL are connected to V_{DPUM} through pull-up resistors R_{PM}; SDX

and SCX are connected to V_{DPUX} through the pull-up resistor $R_{PX.}$ The minimum transmission voltage V_{PASS} = min (V_{DPUM} , V_{DPU0} , ⋯, V_{DPUX}) is defined.

When the Control register of PCA9546 is configured to open channel X, the data transmission on the bus is shown in Figure 6 and Figure 7 (taking SDA and SDX buses as examples), where Figure 6 is the diagram of high-level transmission on the bus and Figure 7 is the diagram of low-level transmission on the bus. Since the circuit system is symmetrical, only the case of V_{DPUM} ＞V_{DPUX} is discussed, that is, V_{PASS} =V_{DPUX}, and V_{DPUM} is always 5.5V.

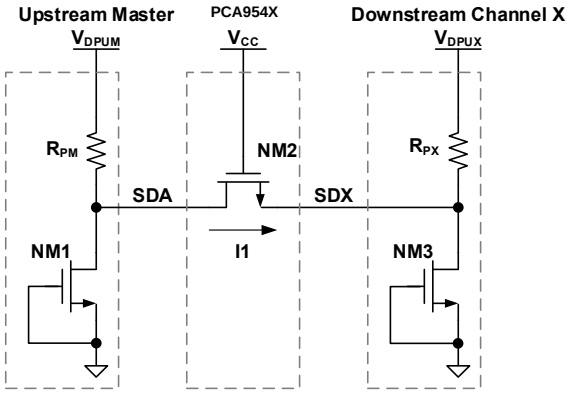


Figure 6 Diagram of High-level Bus Transmission

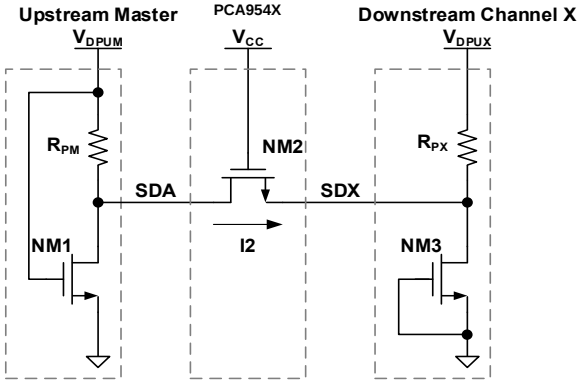


Figure 7 Diagram of Low-level Bus Transmission

When high-level transmission is performed, the following conditions must be met to ensure that the system in Figure 6 works normally:

1) SDA＞0.7*VDPUM, that means SDA will always be recognized as high-level by the upstream host;

2) SDX＜1.1*VDPUX, that means SDX will not exceed the port withstand voltage value of the downstream channel slave;

When V_{PASS}=V_{DPUX}, 2) is the main limitation factor, from which the maximum value of VCC of PCA9546 under various V_{PASS} values can be obtained, as shown in Figure 8, assuming that R_P =R_{PM} =$R_{PX,}$ V_{DPUM} =5.5V.

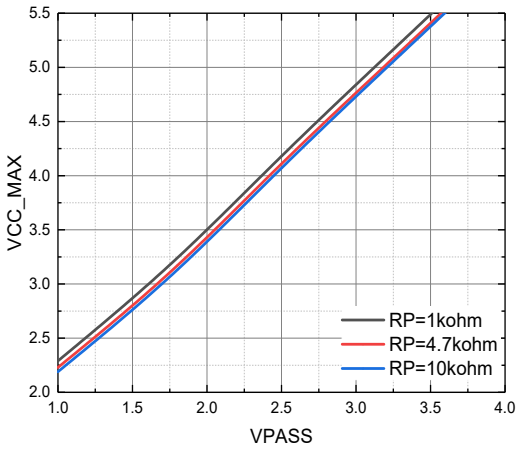
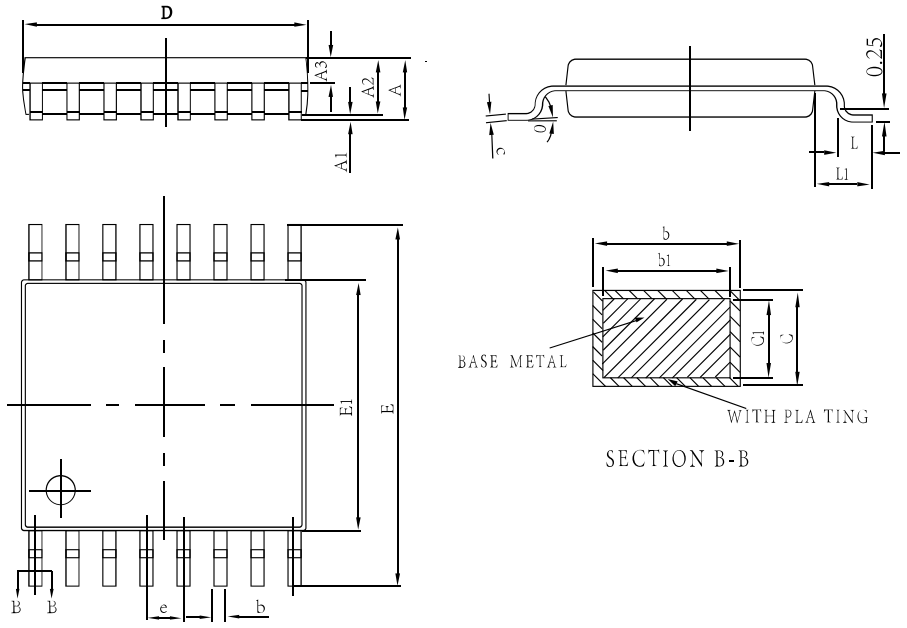


Figure 8 Relation Between Maximum VCC and V_{PASS} During Cross-Voltage Data Transmission

When low-level transmission is performed , the value of |SDA-SDX| mainly depends on the on-resistance R_{ON} of NM2 in Figure 7, as shown in Section 6.4 for details.

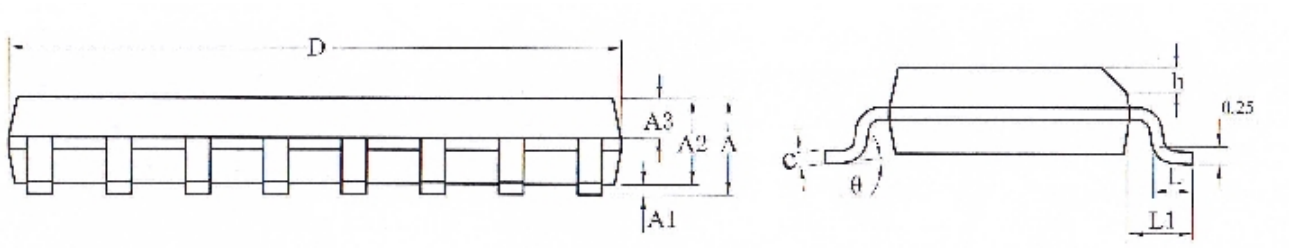
Encapsulation information

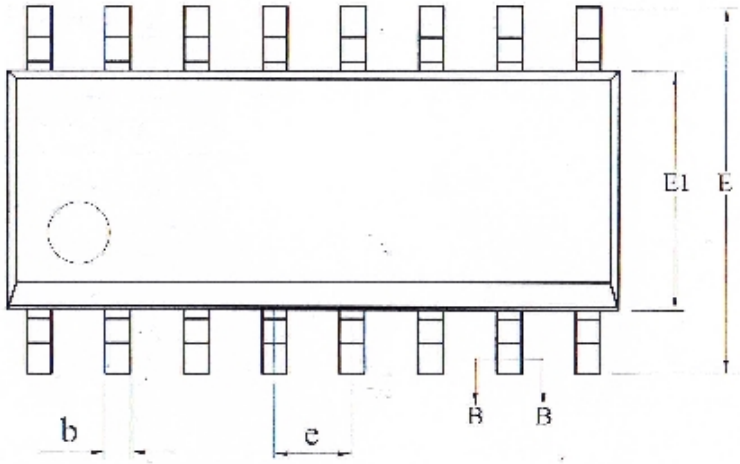
TSSOP-16

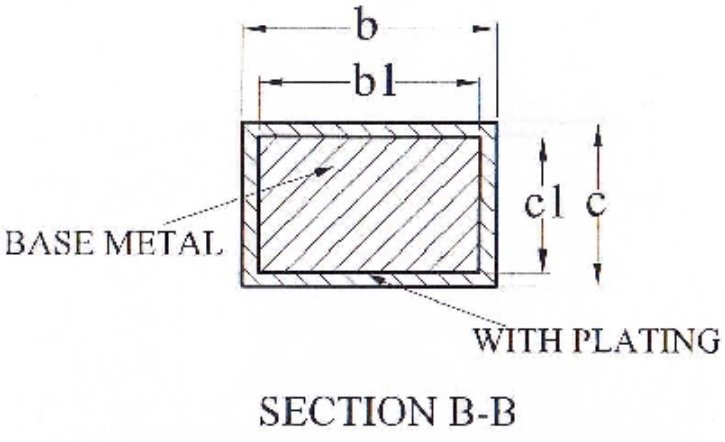


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A 1	0.05	—	0.15
A 2	0.90	1.00	1.05
A 3	0.39	0.44	0.49
b	0.20	—	0.28
b 1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0		8°

SOP-16





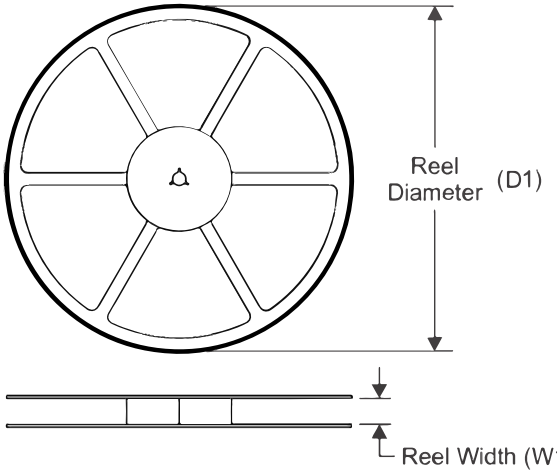


SECTION B-B

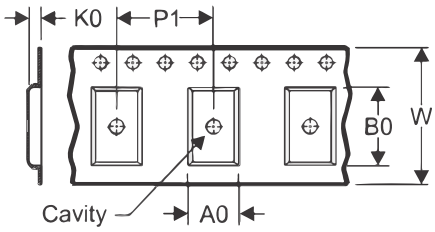
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Reel and Tape Information

REEL DIMENSIONS

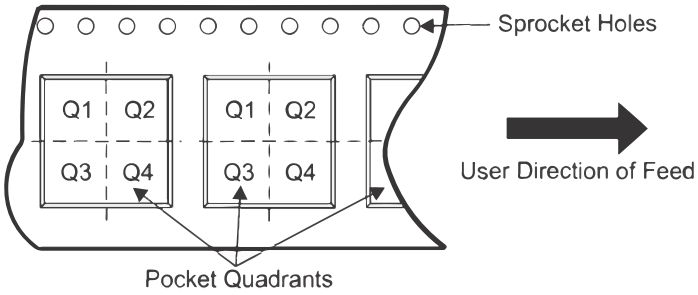


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SOP-16	330	16.40	6.70	10.40	2.10	8.00	16.00	Q1
TSSOP-16	329	12.80	6.80	5.40	1.30	8.00	12.00	Q1

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW PCA9546ADR	SOP-16	3000	Tape and reel	PCA9546AD
UMW PCA9546APWR	TSSOP-16	5000	Tape and reel	PCA9546A