芯伯乐®
XINBOLE

# Product Specification

## XBLW CD4052

Dual 4-channel Analog Multiplexer/Demultiplexer

WEB | www.xinboleic.com

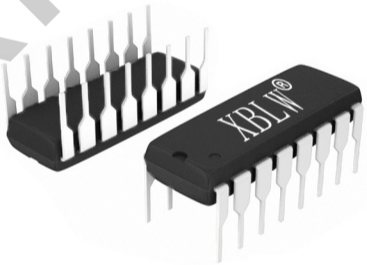
## Description

The CD4052 is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logic includes two select inputs (S1 and S2) and an active LOW enable input ($\overline{E}$). Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY0 to nY3) and the other side connected to a common input/output (nZ). With $\overline{E}$ LOW, one of the four switches is selected (low-impedance ON-state) by S1 and S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 and S2. If break before make is needed, then it is necessary to use the enable input.

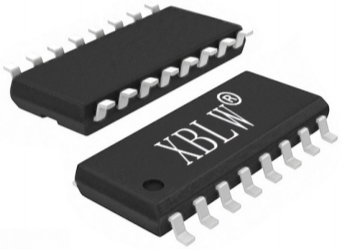
$V_{DD}$ and $V_{SS}$ are the supply voltage connections for the digital control inputs (S1 and S2, and $\overline{E}$). The $V_{DD}$ to $V_{SS}$ range is 3V to 9V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between $V_{DD}$ as a positive limit and $V_{EE}$ as a negative limit. $V_{DD}$-$V_{EE}$ may not exceed 9V. Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input. For operation as a digital multiplexer/demultiplexer, $V_{EE}$ is connected to $V_{SS}$ (typically ground). $V_{EE}$ and $V_{SS}$ are the supply voltage connections for the switches.

## Features

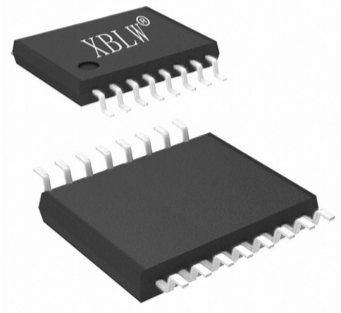
- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16




DIP-16




SOP-16




TSSOP-16

## Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors

## Ordering Information

| Product Model | Package Type | Marking | Packing | Packing Qty |
|---|---|---|---|---|
| XBLW CD4052BE | DIP-16 | CD4052BE | Tube | 1000Pcs/Box |
| XBLW CD4052BDTR | SOP-16 | CD4052B | Tape | 2500Pcs/Reel |
| XBLW CD4052BTDTR | TSSOP-16 | CD4052B | Tape | 3000Pcs/Reel |

## Block Diagram

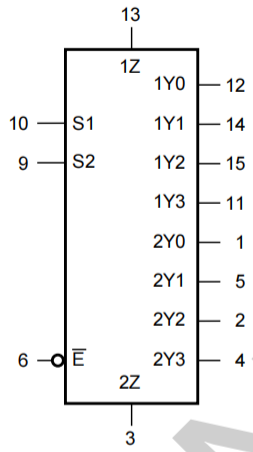



Figure 1. Logic symbol

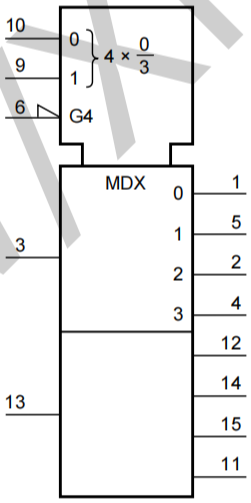



Figure 2. IEC logic symbol

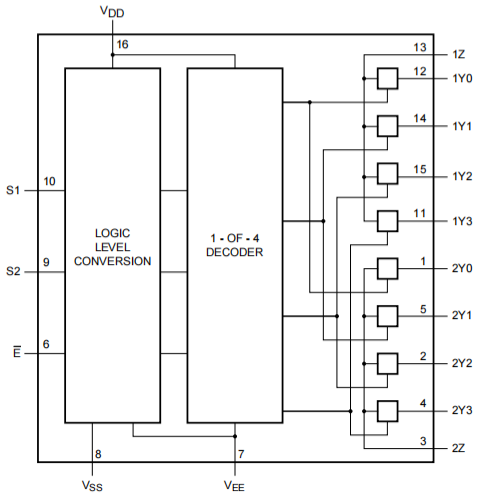



Figure 3. Functional diagram

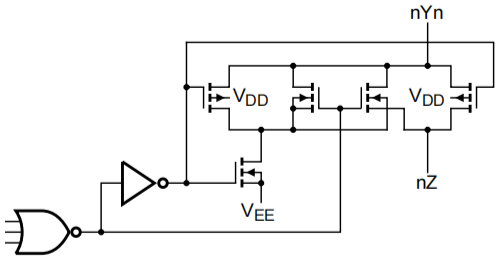



Figure 4. Schematic diagram (one switch)

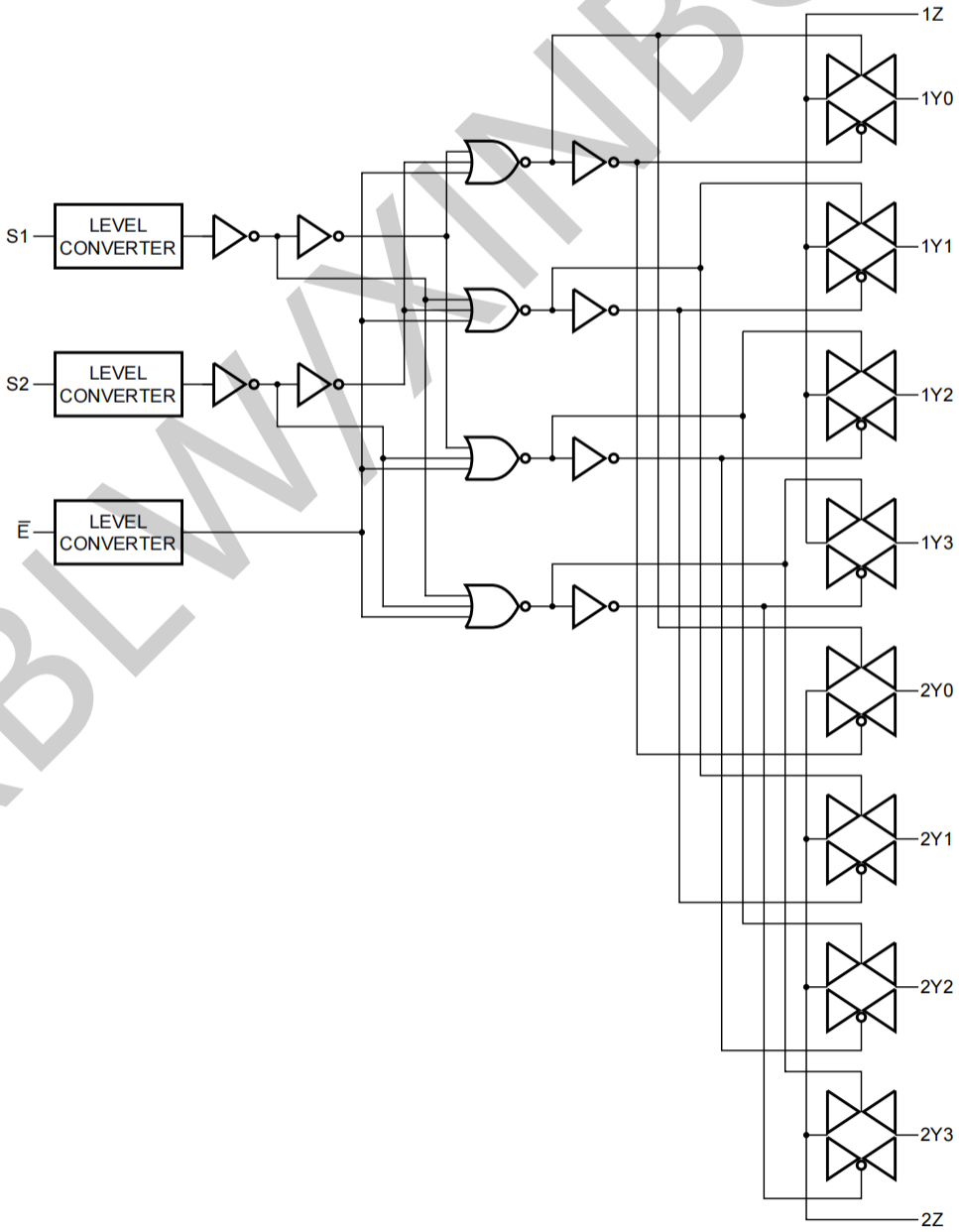
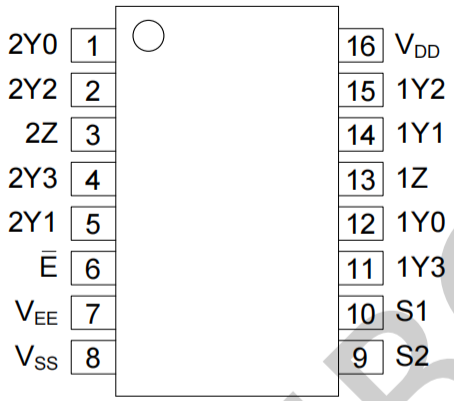



Figure 5. Logic diagram

## Pin Configurations




## Pin Description

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | 2Y0 | independent input or output |
| 2 | 2Y2 | independent input or output |
| 3 | 2Z | common output or input |
| 4 | 2Y3 | independent input or output |
| 5 | 2Y1 | independent input or output |
| 6 | $\bar{E}$ | enable input (active LOW) |
| 7 | $V_{EE}$ | supply voltage |
| 8 | $V_{SS}$ | ground (0V) |
| 9 | S2 | select input |
| 10 | S1 | select input |
| 11 | 1Y3 | independent input or output |
| 12 | 1Y0 | independent input or output |
| 13 | 1Z | common output or input |
| 14 | 1Y1 | independent input or output |
| 15 | 1Y2 | independent input or output |
| 16 | $V_{DD}$ | supply voltage |

## Function Table

| Input | | | Channel ON |
|---|---|---|---|
| $\bar{E}$ | S2 | S1 | |
| L | L | L | nY0 to nZ |
| L | L | H | nY1 to nZ |
| L | H | L | nY2 to nZ |
| L | H | H | nY3 to nZ |
| H | X | X | switches off |

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

# Electrical Parameter

## Absolute Maximum Ratings

(Voltages are referenced to $V_{SS}$ (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| supply voltage | $V_{DD}$ | - | -0.5 | +12 | V |
| power supply range | $V_{DD}$-$V_{EE}$ | - | -0.5 | +12 | V |
| static current | $I_Q$ | $V_{DD}$-$V_{EE}$=12V | - | 2 | uA |
| input voltage | $V_I$ | - | -0.5 | $V_{DD}$+0.5 | V |
| output high voltage current | $\|I_{IH}\|$ | $V_{DD}$=5V, $V_I$=$V_{DD}$ | - | 1 | uA |
| output low voltage current | $\|I_{IL}\|$ | $V_{DD}$=5V, $V_I$=0V | - | 1 | uA |
| input and output voltage rage | $V_{IO}$ | - | $V_{EE}$-0.5 | $V_{DD}$+0.5 | V |
| input clamping current | $I_{IK}$ | $V_I$<-0.5V or $V_I$>$V_{DD}$+0.5V | - | ±20 | mA |
| input and output clamp current | $I_{IOK}$ | $V_{IO}$<$V_{EE}$-0.5V or $V_{IO}$>$V_{DD}$+0.5V | - | ±20 | mA |
| switch conduction current | $I_T$ | $V_O$=-0.5V to $V_{DD}$+0.5V | - | ±25 | mA |
| VDD or GND current | $I_{DD}$, $I_{GND}$ | - | - | ±50 | mA |
| storage temperature | $T_{stg}$ | - | -65 | +150 | ℃ |
| total power dissipation | $P_{tot}$ | - | - | 500 | mW |
| Soldering temperature | $T_L$ | 10s, DIP | 245 | | ℃ |
| | | 10s, SOP/TSSOP | 260 | | ℃ |

## Recommended Operating Conditions

($T_{amb}$=25℃; $R_L$=10kΩ; $C_L$=50pF; $\overline{E}$=$V_{DD}$; Vis=$V_{DD}$=5V.)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| supply voltage | $V_{DD}$ | - | 3 | 5 | 9 | V |
| ambient temperature | $T_{amb}$ | in free air | -40 | - | +125 | ℃ |
| supply voltage | $V_{EE}$ | - | -6.0 | - | 0 | V |
| supply voltage | $V_{DD}$-$V_{EE}$ | - | 3.0 | - | 9.0 | V |
| input voltage | $V_I$ | - | 0 | - | $V_{DD}$ | V |
| input and output voltage | $V_{IO}$ | - | $V_{EE}$ | - | $V_{DD}$ | V |
| Input rise and fall time | $t_r$, $t_f$ | - | - | - | 1000 | ns |
| | | - | - | - | 500 | ns |
| | | - | - | - | 400 | ns |
| input capacitance | $C_I$ | - | - | - | 7.5 | pF |

## Electrical Characteristics

### DC Characteristics 1

($T_{amb}$=25°C, voltages are referenced to $V_{SS}$ (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions (V) | | $T_{amb}$=25°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| supply current | $I_{DD}$ | $V_I$=$V_{DD}$ or $V_{SS}$, $I_O$=0A | $V_{DD}$=5V | - | - | 20 | uA |
| | | | $V_{DD}$=9V | - | - | 40 | uA |
| HIGH-level input voltage | $V_{IH}$ | \|$I_O$\|<1uA | $V_{DD}$=5V | 3.5 | - | - | V |
| | | | $V_{DD}$=9V | 7.0 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | \|$I_O$\|<1uA | $V_{DD}$=5V | - | - | 1.5 | V |
| | | | $V_{DD}$=9V | - | - | 3.0 | V |
| input leakage current | $I_I$ | $V_I$=0V or 9V, $V_{DD}$=9V | | - | - | 1.0 | uA |
| 3 state output leakage current | $I_{OZ}$ | $V_{DD}$=9V | output to $V_{DD}$ | - | - | 1.6 | uA |
| | | | output to $V_{SS}$ | - | - | -1.6 | uA |
| ON resistance (rail) | $R_{ON}$ | $V_I$=0V to $V_{DD}$-$V_{EE}$ | $V_{DD}$-$V_{EE}$=5V | - | 350 | 2500 | Ω |
| | | | $V_{DD}$-$V_{EE}$=9V | - | 80 | 245 | Ω |
| | | $V_I$=0V | $V_{DD}$-$V_{EE}$=5V | - | 115 | 340 | Ω |
| | | | $V_{DD}$-$V_{EE}$=9V | - | 50 | 160 | Ω |
| | | $V_I$=$V_{DD}$-$V_{EE}$ | $V_{DD}$-$V_{EE}$=5V | - | 120 | 365 | Ω |
| | | | $V_{DD}$-$V_{EE}$=9V | - | 65 | 200 | Ω |
| ON resistance mismatch between channels | $\Delta R_{ON}$ | $V_I$=0V to $V_{DD}$-$V_{EE}$ | $V_{DD}$-$V_{EE}$=5V | - | 25 | - | Ω |
| | | | $V_{DD}$-$V_{EE}$=9V | - | 10 | - | Ω |
| OFF-state leakage current | $I_{S(OFF)}$ | $V_{SS}$=$V_{EE}$, $V_{DD}$-$V_{EE}$=9V | all channel off; $\overline{E}$=$V_{DD}$ | - | - | 1.0 | uA |
| | | | any channel; $\overline{E}$=$V_{SS}$ | - | - | 1.0 | uA |

Note: On resistance waveform and test circuit see Figure 13 and Figure 14.

**DC Characteristics 2**

($T_{amb}$=-40°C to +125°C, voltages are referenced to $V_{SS}$ (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions (V) | | $T_{amb}$=-40°C | | $T_{amb}$=+85°C | | $T_{amb}$=+125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| supply current | $I_{DD}$ | $V_I$=$V_{DD}$ or $V_{SS}$, $I_O$=0A | $V_{DD}$=5V | - | 20 | - | 150 | - | 150 | uA |
| | | | $V_{DD}$=9V | - | 40 | - | 300 | - | 300 | uA |
| HIGH-level input voltage | $V_{IH}$ | $\|I_O\|$<1uA | $V_{DD}$=5V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | $V_{DD}$=9V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| LOW-level input voltage | $V_{IL}$ | $\|I_O\|$<1uA | $V_{DD}$=5V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | $V_{DD}$=9V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| input leakage current | $I_I$ | $V_I$=0V or 9V, $V_{DD}$=9V | | - | 1.0 | - | 1.0 | - | 1.0 | uA |
| 3 state output leakage current | $I_{OZ}$ | $V_{DD}$=9V | output to $V_{DD}$ | - | 1.6 | - | 12.0 | - | 12.0 | uA |
| | | | output to $V_{SS}$ | - | -1.6 | - | -12.0 | - | -12.0 | uA |

**AC Characteristics 1**

($T_{amb}$=25°C, $V_{EE}$=$V_{SS}$=0V, $t_r$, $t_f$≤20ns, $C_L$=50pF, $R_L$=10kΩ, unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH to LOW propagation delay time | $t_{PHL}$ | Yn to Z; Z to Yn; see Figure 7 | $V_{DD}$=5V | - | 10 | 20 | ns |
| | | | $V_{DD}$=9V | - | 5 | 10 | ns |
| | | Sn to Yn, Z; see Figure 8 | $V_{DD}$=5V | - | 150 | 305 | ns |
| | | | $V_{DD}$=9V | - | 65 | 135 | ns |
| LOW to HIGH propagation delay | $t_{PLH}$ | Yn to Z; Z to Yn; see Figure 7 | $V_{DD}$=5V | - | 10 | 20 | ns |
| | | | $V_{DD}$=9V | - | 5 | 10 | ns |
| | | Sn to Yn, Z; see Figure 8 | $V_{DD}$=5V | - | 150 | 300 | ns |
| | | | $V_{DD}$=9V | - | 75 | 150 | ns |
| HIGH to OFF-state Propagation delay | $t_{PHZ}$ | $\overline{E}$ to Yn, Z; see Figure 9 | $V_{DD}$=5V | - | 95 | 190 | ns |
| | | | $V_{DD}$=9V | - | 90 | 180 | ns |
| LOW to OFF-state Propagation delay | $t_{PLZ}$ | $\overline{E}$ to Yn, Z; see Figure 9 | $V_{DD}$=5V | - | 100 | 205 | ns |
| | | | $V_{DD}$=9V | - | 90 | 180 | ns |
| OFF-state to HIGH Propagation delay | $t_{PZH}$ | $\overline{E}$ to Yn, Z; see Figure 9 | $V_{DD}$=5V | - | 130 | 260 | ns |
| | | | $V_{DD}$=9V | - | 55 | 115 | ns |
| OFF-state to LOW Propagation delay | $t_{PZL}$ | $\overline{E}$ to Yn, Z; see Figure 9 | $V_{DD}$=5V | - | 120 | 240 | ns |
| | | | $V_{DD}$=9V | - | 50 | 100 | ns |

**AC Characteristics 2**

($T_{amb}$=25°C, $V_{EE}$=$V_{SS}$=0V, $V_I$=0.5$V_{DD}$ (p-p), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Square wave distortion | $d_{sin}$ | see Figure 10; $R_L$=10kΩ; $C_L$=15pF; channel ON; $f_i$=1kHz | $V_{DD}$=5V | 0.25 | - | - | % |
| | | | $V_{DD}$=9V | 0.04 | - | - | % |
| any two channel crosstalk | $f_{ct}$ | $V_{DD}$=9V, see note2 | | 1 | - | - | MHz |
| crosstalk voltage ($\overline{E}$ to Sn or Yn to Z) | $V_{ct}$ | see Figure 11; $R_L$=10kΩ; $C_L$=15pF; $\overline{E}$ or Sn=$V_{DD}$ (square-wave) | | 50 | - | - | mV |
| OFF frequency | $f_{OFF}$ | $V_{DD}$=9V, see note3 | | 1 | - | - | MHz |
| conduction frequency | $f_{ON}$ | $V_{DD}$=5V, see note4 | | 13 | - | - | MHz |
| | | $V_{DD}$=9V, see note4 | | 40 | - | - | MHz |

Note:

[1] $f_i$ is biased at 0.5$V_{DD}$; $V_I$=0.5$V_{DD}$ (p-p).

[2] $R_L$=1kΩ; 20logVos/Vis=-50dB, see Figure 12.

[3] $R_L$=1kΩ; $C_L$=5pF, channel off, 20logVos/Vis=-50dB, see Figure 10.

[4] $R_L$=1kΩ; $C_L$=5pF, channel on, 20logVos/Vis=-3dB, see Figure 10.

## Testing Circuit

### AC Testing Circuit

1

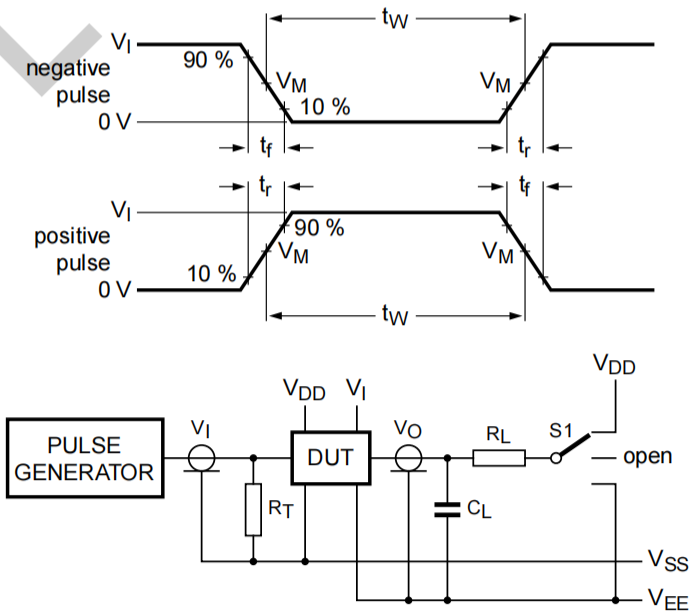



Figure 6. Test circuit for switching times

Definitions for test circuit:DUT=Device Under Test.

$C_L$=Load capacitance including jig and probe capacitance.

$R_T$=Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

$R_L$=Load resistance.

**AC Testing Waveforms**

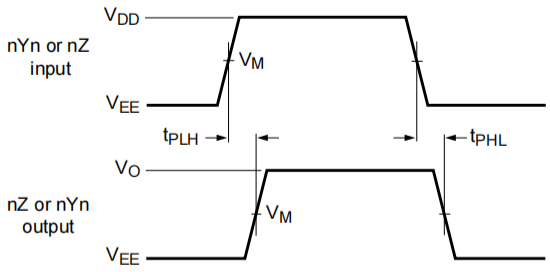



Figure 7. nYn, nZ to nZ, nYn propagation delays

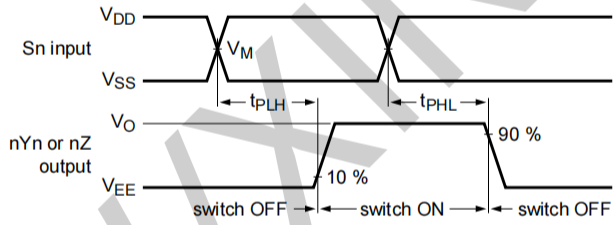



Figure 8. Sn tonYn, nZ propagation delays

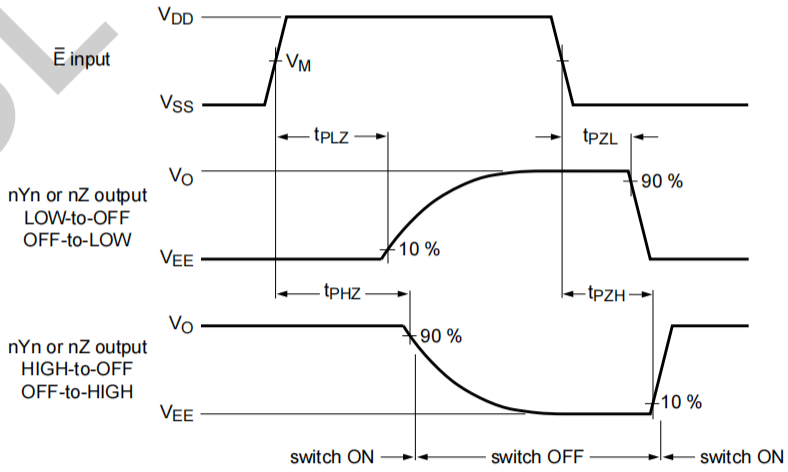



Figure 9. Enable and disable times

**AC Testing Circuit 2**

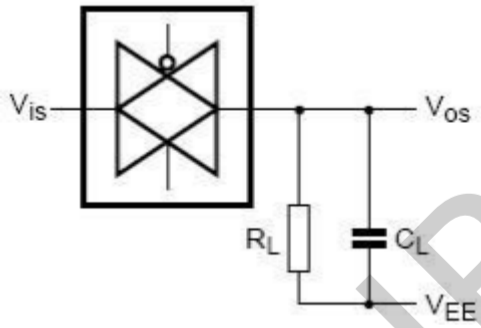



Figure 10. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

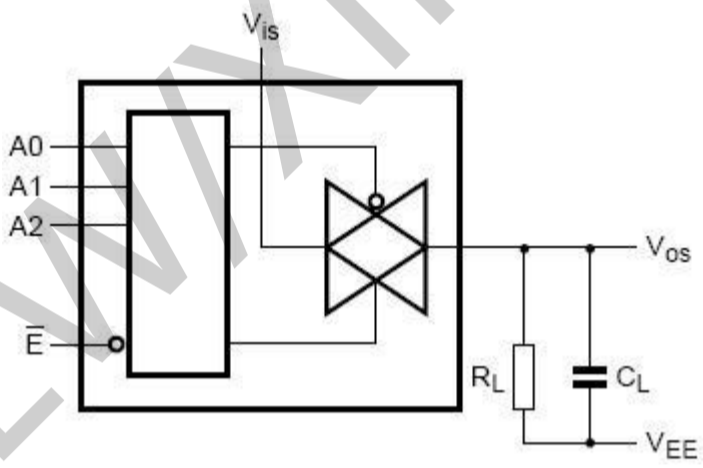



Figure 11. Crosstalk logical input/output test

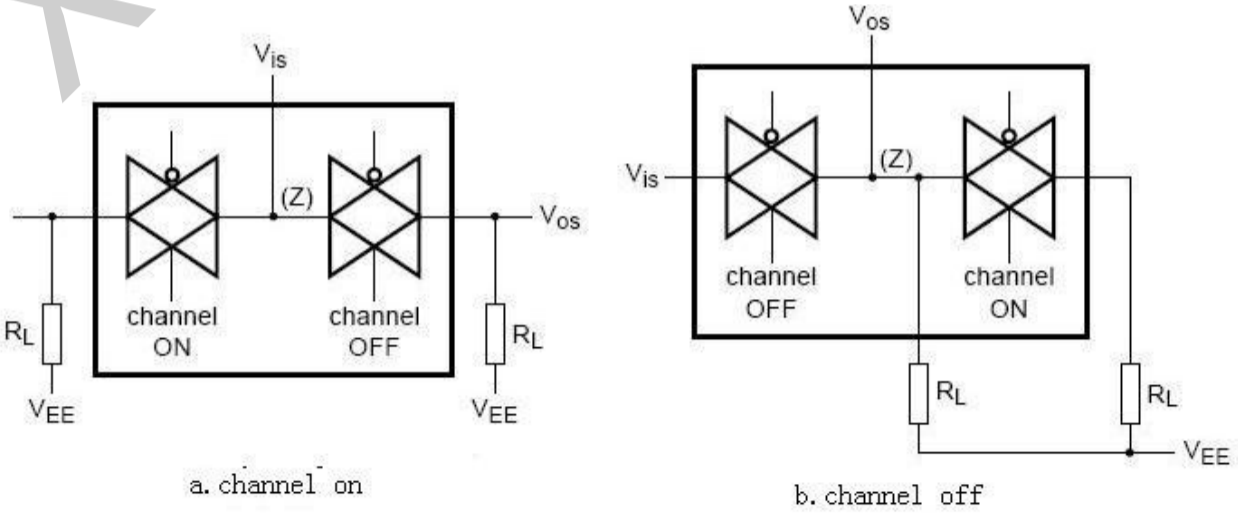



Figure 12. Inter channel Crosstalk

**On Resistance Waveform And Test Circuit**

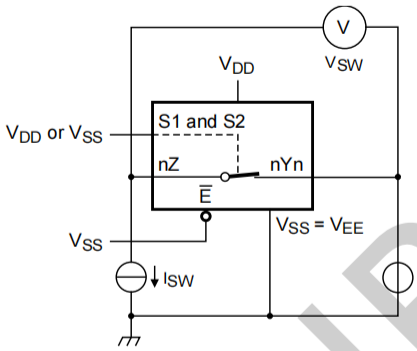



Figure 13. Test circuit for measuring $R_{ON}$

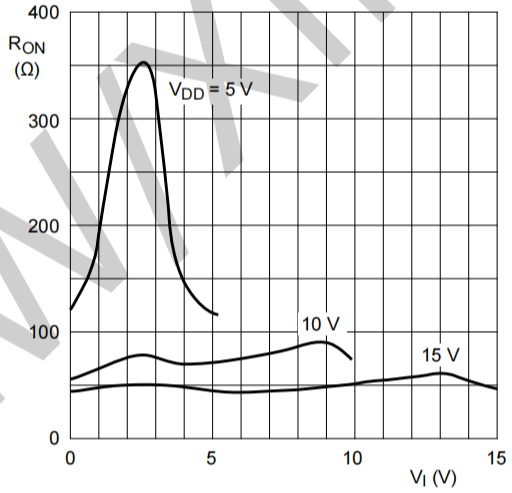



Figure 14. Typical $R_{ON}$ as a function of input voltage

**Measurement Points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{DD}$ | $V_M$ | $V_M$ |
| 3V to 9V | $0.5\times V_{DD}$ | $0.5\times V_{DD}$ |

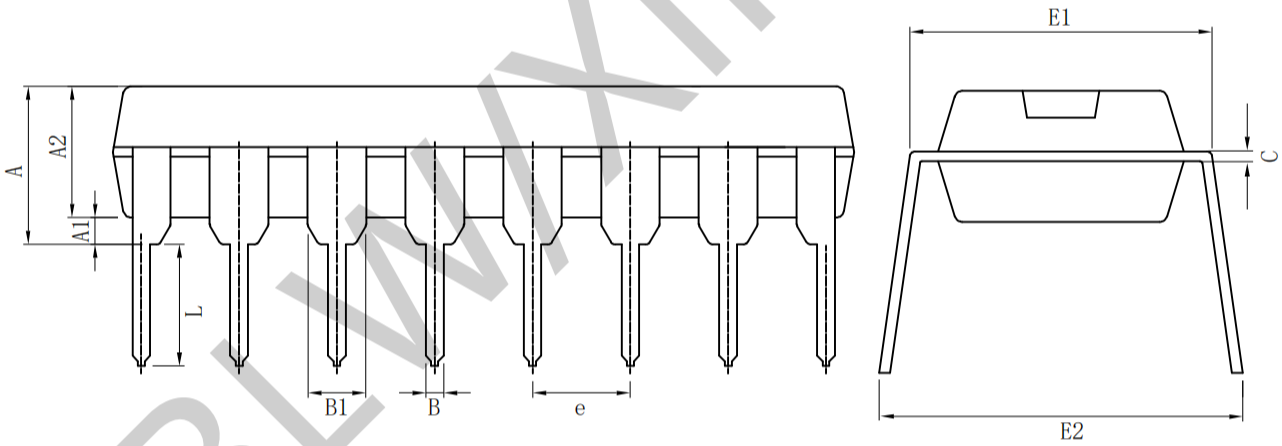
**Test Data**

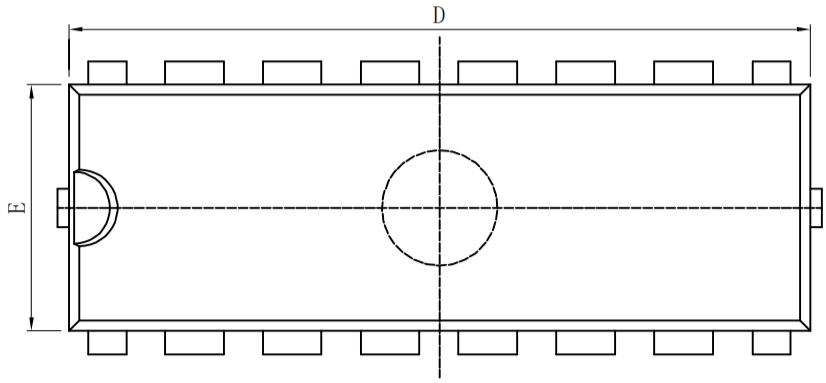
| Test | Input | | Load | | Switch |
|---|---|---|---|---|---|
| | $V_{is}$ | $t_r, t_f$ | $C_L$ | $R_L$ | |
| $t_{PHL}$ | $V_{EE}$ | 20ns | 50pF | 10kΩ | $V_{DD}$ |
| $t_{PLH}$ | $V_{DD}$ | 20ns | 50pF | 10kΩ | $V_{EE}$ |
| $t_{PZH}$, $t_{PHZ}$ | $V_{DD}$ | 20ns | 50pF | 10kΩ | $V_{EE}$ |
| $t_{PZL}$, $t_{PLZ}$ | $V_{EE}$ | 20ns | 50pF | 10kΩ | $V_{DD}$ |
| others | pulse | 20ns | 50pF | 10kΩ | open |

## Package Information

· DIP-16

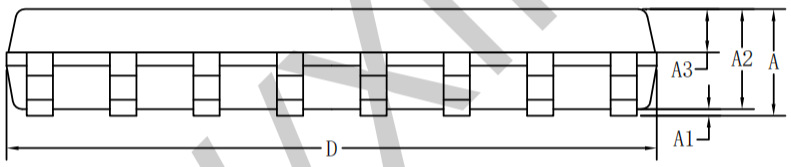
| Size / Symbol | Dimensions In Millimeters | | Size / Symbol | Dimensions In Inches | |
|---|---|---|---|---|---|
| | Min( mm) | Max( mm) | | Min( in) | Max( in) |
| A | 3.710 | 4.310 | A | 0.146 | 0.170 |
| A1 | 0.510 | | A1 | 0.020 | |
| A2 | 3.200 | 3.600 | A2 | 0.126 | 0.142 |
| B | 0.380 | 0.570 | B | 0.015 | 0.022 |
| B1 | 1.524(BSC) | | B1 | 0.060(BSC) | |
| C | 0.204 | 0.360 | C | 0.008 | 0.014 |
| D | 18.80 | 19.20 | D | 0.740 | 0.756 |
| E | 6.200 | 6.600 | E | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | E1 | 0.288 | 0.312 |
| e | 2.540(BSC) | | e | 0.100(BSC) | |
| L | 3.000 | 3.600 | L | 0.118 | 0.142 |
| E2 | 8.400 | 9.000 | E2 | 0.331 | 0.354 |

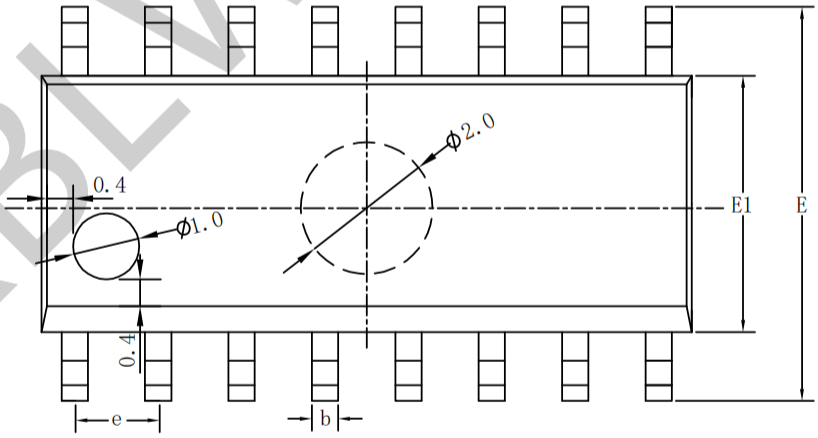


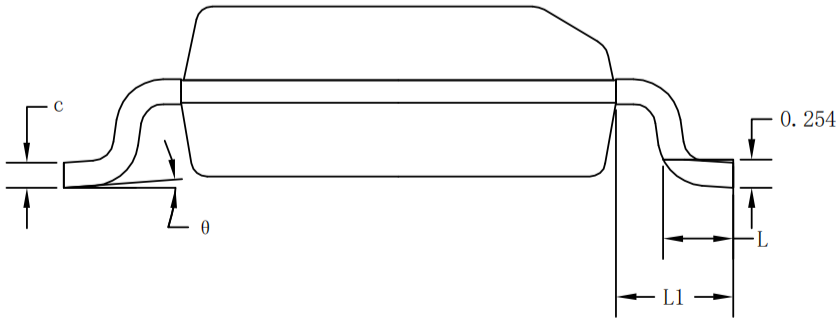



## · SOP-16

| Size / Symbol | Dimensions In Millimeters | | | Size / Symbol | Dimensions In Inches | | |
|---|---|---|---|---|---|---|---|
| | Min(mm) | Nom(mm) | Max(mm) | | Min(in) | Nom(in) | Max(in) |
| A | 1.500 | 1.600 | 1.700 | A | 0.059 | 0.063 | 0.067 |
| A1 | 0.100 | 0.150 | 0.250 | A1 | 0.004 | 0.006 | 0.010 |
| A2 | 1.400 | 1.450 | 1.500 | A2 | 0.055 | 0.057 | 0.059 |
| A3 | 0.600 | 0.650 | 0.700 | A3 | 0.024 | 0.026 | 0.028 |
| b | 0.300 | 0.400 | 0.500 | b | 0.012 | 0.016 | 0.020 |
| c | 0.150 | 0.200 | 0.250 | c | 0.006 | 0.008 | 0.010 |
| D | 9.800 | 9.900 | 10.00 | D | 0.386 | 0.390 | 0.394 |
| E | 5.800 | 6.000 | 6.200 | E | 0.228 | 0.236 | 0.244 |
| E1 | 3.850 | 3.900 | 3.950 | E1 | 0.152 | 0.154 | 0.156 |
| e | | 1.27(BSC) | | e | | 0.050(BSC) | |
| L | 0.500 | 0.600 | 0.700 | L | 0.020 | 0.024 | 0.028 |
| L1 | | 1.05(BSC) | | L1 | | 0.041(BSC) | |
| θ | 0° | 4° | 8° | θ | 0° | 4° | 8° |

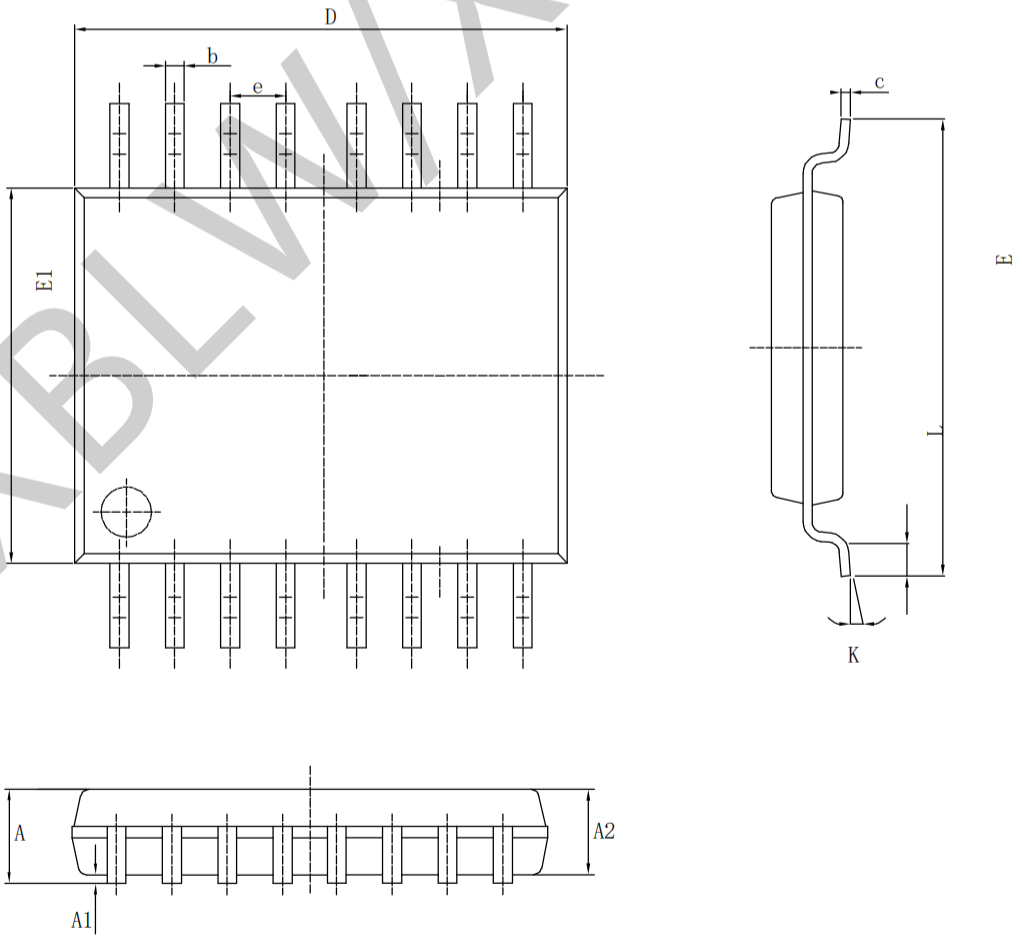


## · TSSOP-16

| Size / Symbol | Dimensions In Millimeters | | Size / Symbol | Dimensions In Inches | |
|---|---|---|---|---|---|
| | Min(mm) | Max(mm) | | Min(in) | Max(in) |
| A | | 1.200 | A | | 0.047 |
| A1 | 0.050 | 0.150 | A1 | 0.002 | 0.006 |
| A2 | 0.800 | 1.050 | A2 | 0.031 | 0.041 |
| b | 0.190 | 0.300 | b | 0.007 | 0.012 |
| c | 0.090 | 0.200 | c | 0.004 | 0.0089 |
| D | 4.900 | 5.100 | D | 0.193 | 0.201 |
| E | 6.200 | 6.600 | E | 0.244 | 0.260 |
| E1 | 4.300 | 4.480 | E1 | 0.169 | 0.176 |
| e | 0.65(BSC) | | e | 0.0256(BSC) | |
| K | 0° | 8° | K | 0° | 8° |
| L | 0.450 | 0.750 | L | 0.018 | 0.030 |



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