## General Description

The EA3327 is a dual channel power management IC. It integrates two synchronous buck converters and can provide high efficiency. The internal compensation architecture simplifies the application circuit design and the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes. All converters feature complete protection functions, including cycle-by-cycle current limit, short circuit protection, OTP and UVLO protection. The EA3327 is available in a tiny 12 pin DFN 3x3 package and can save the PCB area.

## Features

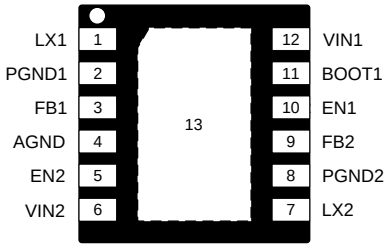
- 1CH DC/DC Buck Converter (CH1)
  - 5V to 40V Input Voltage Range
  - Fixed 3.3V Output Voltage
  - Fixed 700KHz Switching Frequency
  - PWM Mode at Light Load Operation
  - 1A Continuous Load Current
  - Internal Soft Start Function
  - Independent Enable Control
  - Cycle-by-Cycle Current Limit
  - Input UVLO
  - Hiccup Mode Short Circuit Protection
- 1CH DC/DC Buck Converter (CH2)
  - 2.7V to 5.5V Input Voltage Range
  - Fixed 1.4MHz Switching Frequency
  - High Efficiency at Light Load Operation
  - 1A Continuous Load Current
  - 100% Duty Cycle Low Dropout Operation
  - Internal Soft Start Function
  - Independent Enable Control
  - Cycle-by-Cycle Current Limit
  - Short Circuit Protection
  - Input UVLO
- Auto Recovery OTP Protection
- Reducing the External Components
- Available in 12-pin 3mm x 3mm DFN Package

## Applications

- Smart Meters
- CVRs
- Netcom Products
- Video Doorbell

## Pin Configurations

(TOP VIEW)




DFN 3x3-12

## Pin Description

| Pin Name | Function Description | Pin No. |
|---|---|---|
| LX1 | Internal MOSFET switching output of CH1. Connect LX1 pin with a low pass filter circuit to obtain a stable DC output voltage. | 1 |
| PGND1 | Power ground pin of CH1. | 2 |
| FB1 | Feedback input of CH1. Connect FB1 pin to the output node. | 3 |
| AGND | Analog ground pin. | 4 |
| EN2 | CH2 turns on/turns off control input. Don't leave this pin floating. | 5 |
| VIN2 | Power input pin of CH2. Recommended to use a 10uF MLCC capacitor between VIN2 pin and PGND2 pin. | 6 |
| LX2 | Internal MOSFET switching output of CH2. Connect LX2 pin with a low pass filter circuit to obtain a stable DC output voltage. | 7 |
| PGND2 | Power ground pin of CH2. | 8 |
| FB2 | Feedback input of CH2. Connect to output voltage with a resistor divider. | 9 |
| EN1 | CH1 turns on/turns off control input. Leave this pin floating will turn off the device automatically. | 10 |
| BOOT1 | The power input of the internal high side N-MOSFET gate driver of CH1. Connect a 100nF ceramic capacitor from BOOT1 pin to LX1 pin. | 11 |
| VIN1 | Power input pin of CH1. Recommended to use a 10uF MLCC capacitor between VIN1 pin and PGND pin. | 12 |
| Exposed Pad | The Exposed Pad must be soldered to a large PCB copper plane and connected to GND for appropriate dissipation. | 13 |

## Function Block Diagram

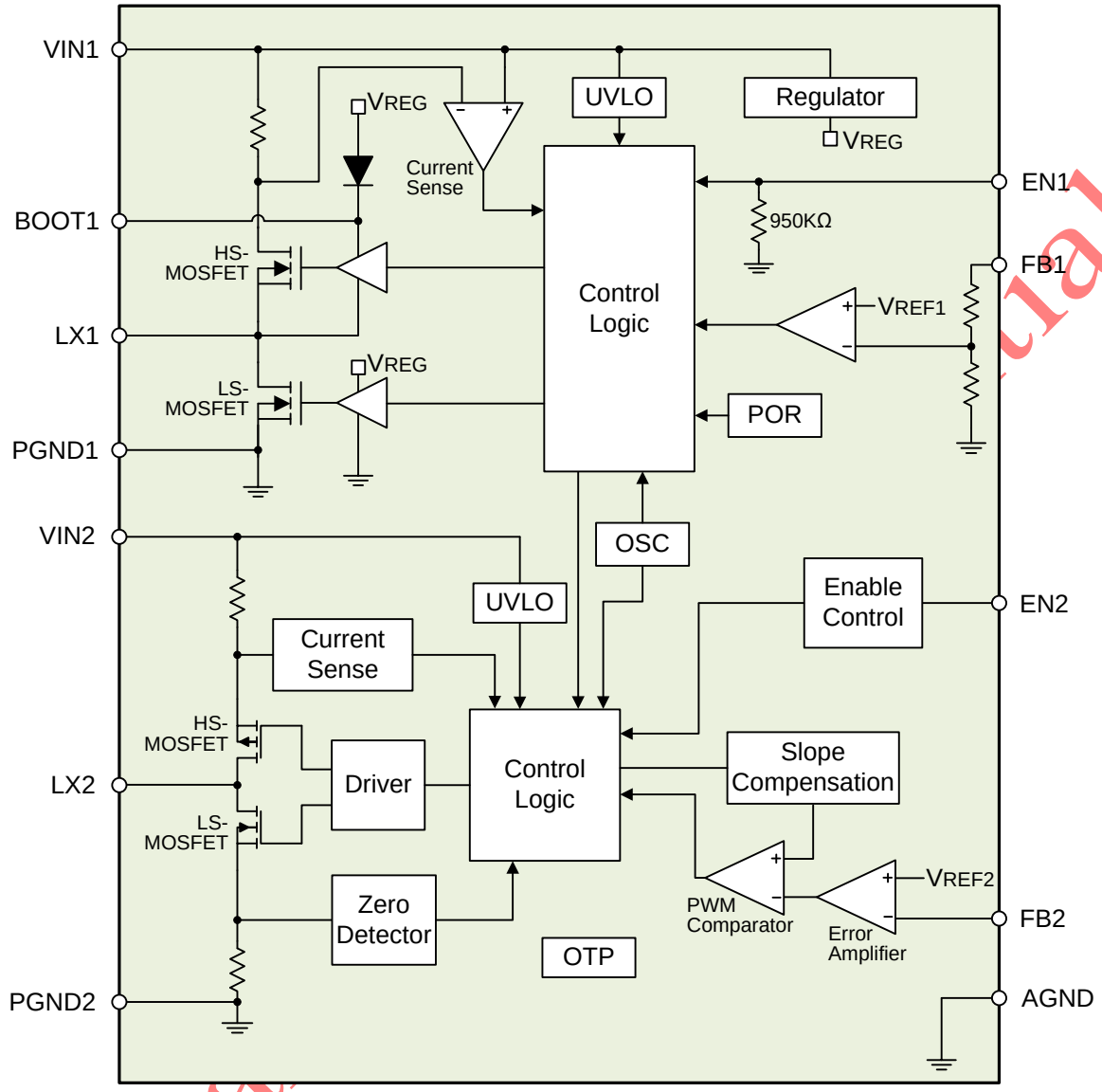



Figure 1. EA3327 internal function block diagram

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| CH1 Input Voltage ($V_{VIN1}$) | -0.3V to +42V |
| CH1 EN Pin Voltage ($V_{EN1}$) | -0.3V to +42V |
| CH1 LX Pin Voltage ($V_{LX1}$) | -0.3V to $V_{VIN1}$+0.3V |
| CH1 BOOT Pin Voltage ($V_{BOOT1}$) | $V_{LX1}$-0.3V to $V_{LX1}$+6V |
| CH2 Input Voltage ($V_{VIN2}$) | -0.3V to +6.5V |
| CH2 EN Pin Voltage ($V_{EN2}$) | -0.3V to +6.5V |
| CH2 LX Pin Voltage ($V_{LX2}$) | -0.3V to $V_{VIN2}$+0.3V |
| All Other Pins Voltage | -0.3V to +6.5V |
| Ambient Temperature operating Range ($T_A$) | -40°C to +85°C |
| Maximum Junction Temperature ($T_{Jmax}$) | +150°C |
| Lead Temperature (Soldering, 10 sec) | +260°C |
| Storage Temperature Range ($T_S$) | -65°C to +150°C |

Note (1):Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability and lifetime.

## Package Thermal Characteristics

| Parameter | Value |
|---|---|
| DFN 3x3-12 Thermal Resistance ($\theta_{JC}$) | 15°C/W |
| DFN 3x3-12 Thermal Resistance ($\theta_{JA}$) | 70°C/W |
| DFN 3x3-12 Power Dissipation at $T_A$=25°C ($P_{Dmax}$) | 1.79W |

Note (1): $P_{Dmax}$ is calculated according to the formula: $P_{DMAX}=(T_{JMAX}-T_A)/\theta_{JA}$.

## Recommended Operating Conditions

| Parameter | Value |
|---|---|
| CH1 Input Voltage ($V_{VIN1}$) | -0.3V to +40V |
| CH2 Input Voltage ($V_{VIN2}$) | -0.3V to +5.5V |
| Junction Temperature Range ($T_J$) | -40°C to +125°C |

## Electrical Characteristics

$V_{VIN1}$=12V, $V_{VIN2}$=3.3V, $T_A$=25°C, unless otherwise noted

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Buck Converter 1** | | | | | | |
| Input Voltage | $V_{VIN1}$ | | 5 | | 40 | V |
| Input UVLO Threshold | $V_{UVLO1}$ | | 4.5 | 4.7 | 5 | V |
| Input UVLO Hysteresis | $V_{UV1-HYST}$ | | | 0.3 | | V |
| Shutdown Supply Current | $I_{SD1}$ | $V_{EN1}$ = 0V | | 0.1 | 1 | uA |
| Quiescent Current | $I_{Q1}$ | $V_{FB1}$ = 3.5V, $V_{REF2}$ = 0.7V, No Load | | 500 | | uA |
| Feedback Voltage | $V_{FB1}$ | 5V ≤ $V_{VIN1}$ ≤ 40V | 3.3 | 3.35 | 3.4 | V |
| Switching Frequency | $F_{SW1}$ | $I_{OUT1}$ = 200mA | 525 | 700 | 875 | KHz |
| High Side MOSFET On-Resistance | $R_{DS(ON)1-HM}$ | | | 500 | | mΩ |
| Low Side MOSFET On-Resistance | $R_{DS(ON)1-LM}$ | | | 200 | | mΩ |
| High Side MOSFET Current Limit | $I_{LIM1-HM}$ | | 1.5 | 2 | | A |
| Minimum On Time | $T_{ON(MIN)1}$ | | | 100 | | ns |
| Enable Pin Input Low Voltage | $V_{EN1-L}$ | | | | 0.4 | V |
| Enable Pin Input High Voltage | $V_{EN1-H}$ | | 2.5 | | | V |
| Enable Pin Pull-Low Resistance | $R_{EN1}$ | | | 950 | | KΩ |
| **Buck Converter 2** | | | | | | |
| Input Voltage | $V_{VIN2}$ | | 2.7 | | 5.5 | V |
| Input UVLO Threshold | $V_{UVLO2}$ | | 2.3 | 2.5 | 2.7 | V |
| Input UVLO Hysteresis | $V_{UV2-HYST}$ | | | 0.1 | | V |
| Shutdown Supply Current | $I_{SD2}$ | $V_{EN2}$ = 0V | | 0.1 | 1 | uA |
| Reference Voltage | $V_{REF2}$ | | 0.588 | 0.6 | 0.612 | V |
| Switching Frequency | $F_{SW2}$ | $I_{OUT2}$ = 200mA | 1.05 | 1.4 | 1.75 | MHz |
| P-MOS On-Resistance | $R_{DS(ON)2-P}$ | | | 250 | | mΩ |
| N-MOS On-Resistance | $R_{DS(ON)2-N}$ | | | 250 | | mΩ |
| P-MOS Current Limit | $I_{LIM2-P}$ | | 1.5 | 2 | | A |
| Maximum Duty Cycle | $D_{MAX2}$ | | 100 | | | % |

## Electrical Characteristics

$V_{VIN1}$=12V, $V_{VIN2}$=3.3V, $T_A$=25°C, unless otherwise noted

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold | $T_{OTP}$ | | | 165 | | °C |
| Thermal Shutdown Hysteresis | $T_{HYST}$ | | | 45 | | °C |

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
(2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

## Application Circuit & Power On Sequence Diagram

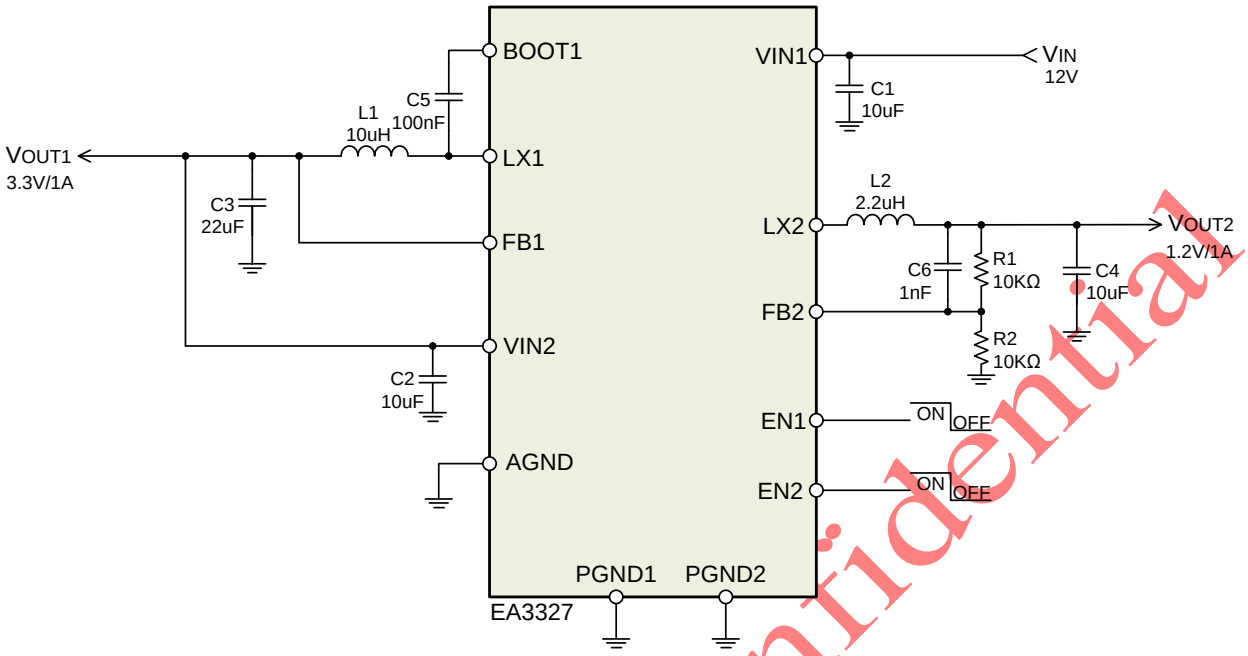



Figure 2. Typical application circuit diagram

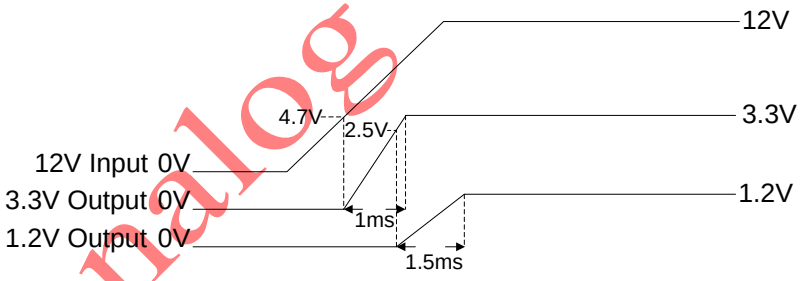



Figure 3. Power On Sequence diagram

## Ordering Information

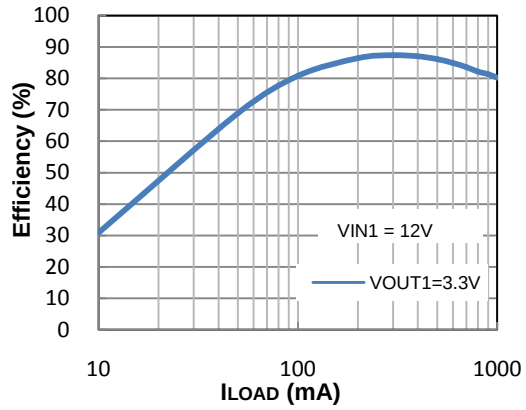
| Part Number | Package Type | Packing Information |
|---|---|---|
| EA3327DFR | DFN 3mm x 3mm-12 | Tape & Reel / 3000 |

Note (1):"DF": Package type code.
(2):"R": Tape & Reel.

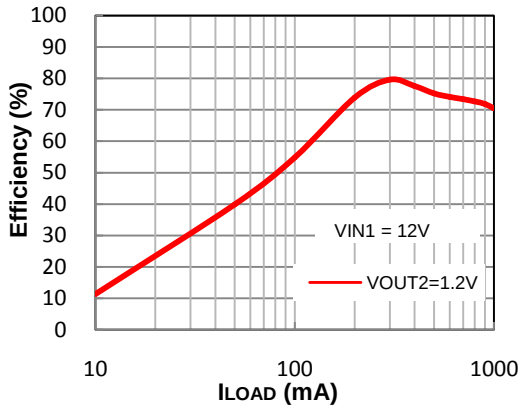
## Typical Operating Characteristics

$V_{IN1}$=12V, $V_{OUT2}$=1.2V, L1=10uH, L2=2.2uH, $C_{OUT1}$=22uF, $C_{OUT2}$=10uF, $T_A$=25°C, unless otherwise noted

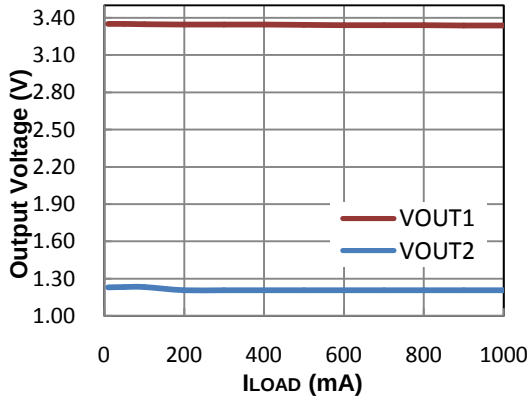
**Efficiency vs. Load Current**



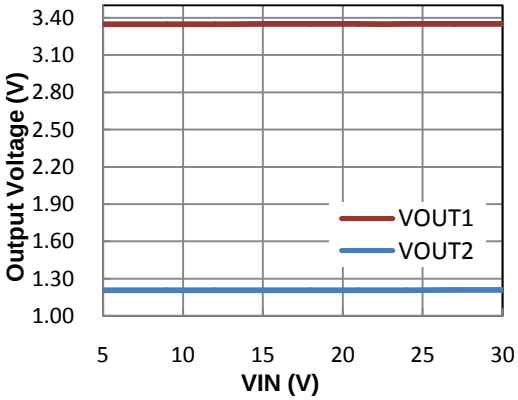

**Efficiency vs. Load Current**

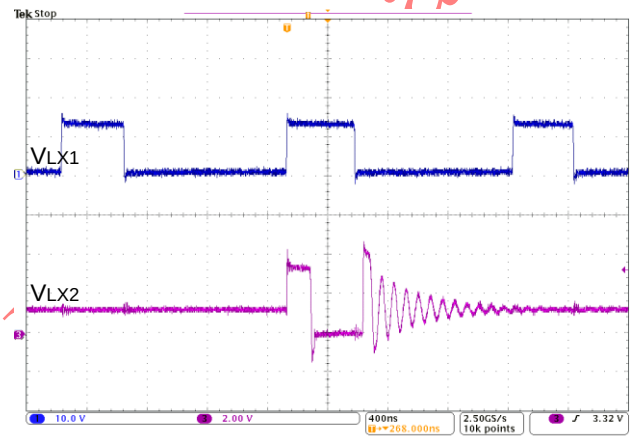



**Load Regulation**

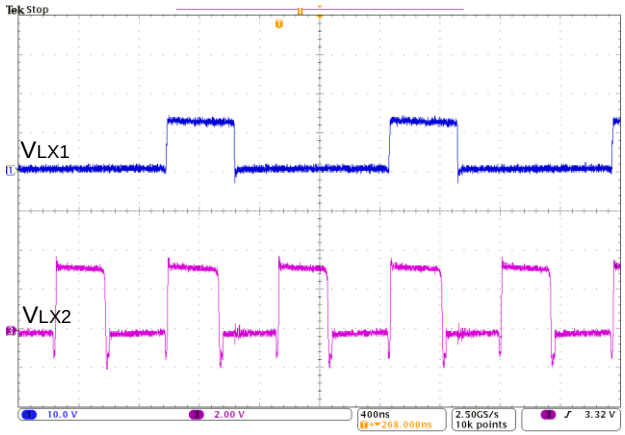



**Line Regulation**



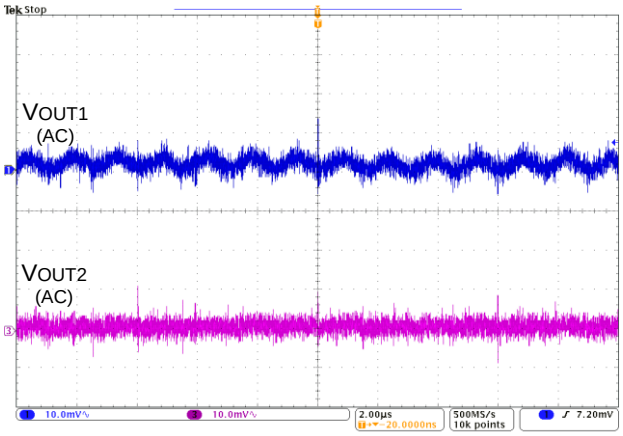

$I_{LOAD1}$=0A, $I_{LOAD2}$=0A Switching Waveform



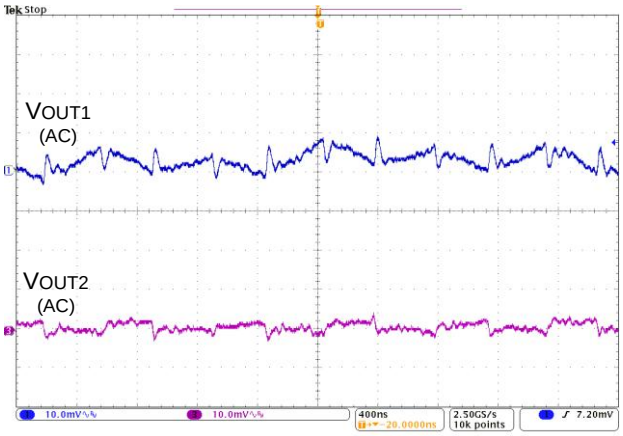

$I_{LOAD1}$=0A, $I_{LOAD2}$=1A Switching Waveform

## Typical Operating Characteristics

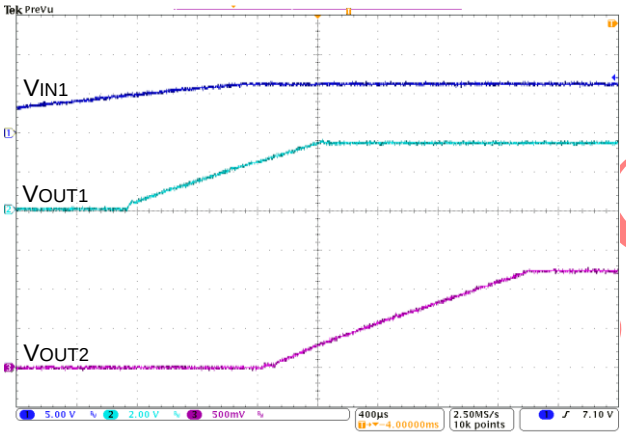
$V_{IN1}$=12V, $V_{OUT2}$=1.2V, L1=10uH, L2=2.2uH, $C_{OUT1}$=22uF, $C_{OUT2}$=10uF, $T_A$=25°C, unless otherwise noted



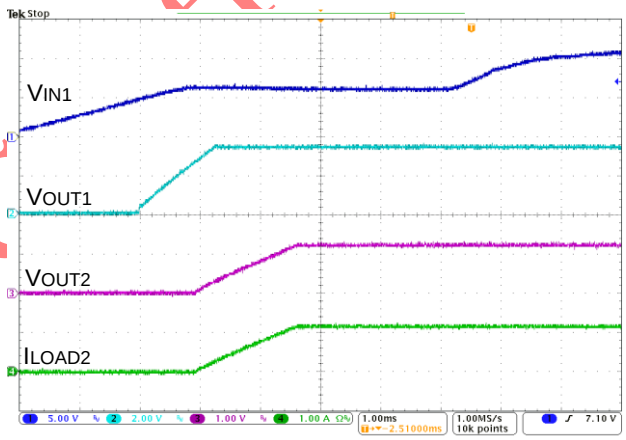

$I_{LOAD1}$=0A, $I_{LOAD2}$=0A Output Ripple Waveform



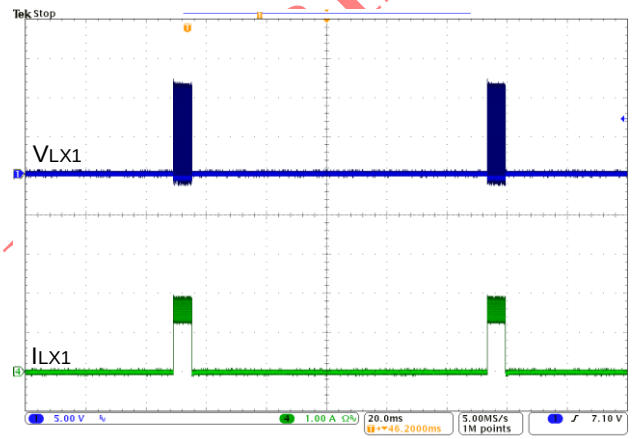

$I_{LOAD1}$=0A, $I_{LOAD2}$=1A Output Ripple Waveform



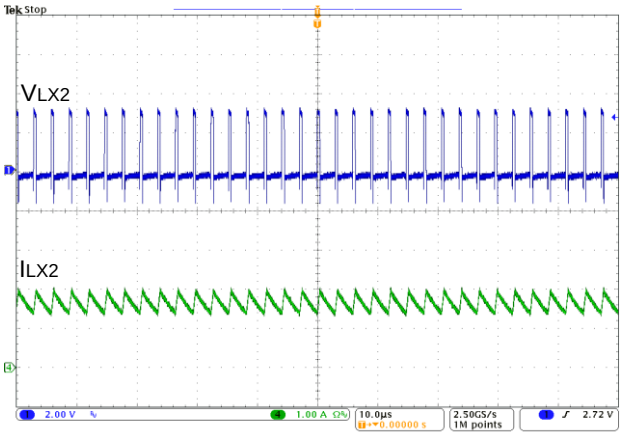

$I_{LOAD1}$=0A, $I_{LOAD2}$=0A Power On Waveform




$I_{LOAD1}$=0A, $I_{LOAD2}$=1A Power On Waveform




$V_{OUT1}$ Short Waveform




$V_{OUT2}$ Short Waveform

# Functional Description

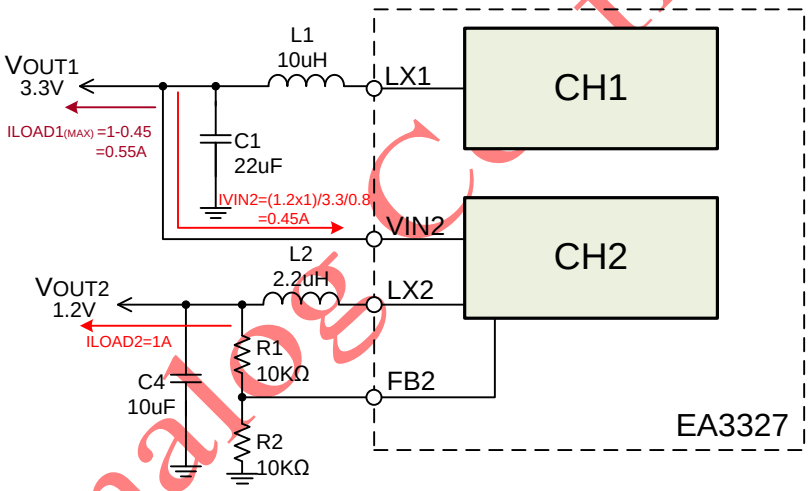
## Overview

The EA3327 is a PMIC which integrates a 40V input voltage range buck regulator (CH1) and a 5.5V input voltage range buck regulator (CH2). The CH1 buck regulator works in PWM mode at whole current range, which can provide the minimum voltage ripple. Each buck regulator has individual protection mechanism which includes cycle-by-cycle current limit, short circuit protection and UVLO.

The EA3327 has channel lock mechanism. The CH2 buck regulator will not work unless the CH1 buck regulator turn on firstly. But the CH1 buck regulator can work independently.

| | | VIN1 | |
|---|---|---|---|
| | | With Power | Without Power |
| VIN2 | With Power | CH1 On, CH2 On | CH1 Off, CH2 Off |
| | Without Power | CH1 On, CH2 Off | CH1 Off, CH2 Off |

Both of the buck regulators are 1A load current spec. If the VIN2 is conected with VOUT1, the CH1 total load current capacity must reduce VIN2 input current, shown as bellow:




## Short Circuit Protection

Both of the buck regulators have short circuit protection. The CH1 buck regulator implements hiccup mode short circuit protection and can reduce the short current substantially. The CH2 buck regulator implements frequency reduced short circuit protection. When the VOUT2 short condition happens, the CH2 switching frequency will reduce to 350KHz.

## Delayed Start-Up

The EA3327 has internal soft-start and delayed start-up function. The delay time between CH1 power on and CH2 power on is about 1ms.

## OTP Protection

The EA3327 implements an internal OTP function. The device will shutdown if the internal junction temperature exceeds 165°C. Once the junction temperature decreases below 120°C, the device will restart automatically.

# Application Information

### Output Voltage Setting

The EA3327 VOUT1is fixed 3.3V output. And the VOUT2 output voltage can be set via a resistor divider (R1, R2). The output voltage is calculated by following equation:

$$V_{OUT} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$

The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

| CH2 Output Voltage | R1 Resistance | R2 Resistance | Tolerance |
|---|---|---|---|
| 1.8V | 20KΩ | 10KΩ | 1% |
| 1.5V | 15KΩ | 10KΩ | 1% |
| 1.2V | 10KΩ | 10KΩ | 1% |

### Input / Output Capacitors Selection

The input capacitors are used to suppress the noise amplitude of the input voltage and provide a stable and clean DC input to the device. Because the ceramic capacitor has low ESR characteristic, so it is suitable for input capacitor use. It is recommended to use X5R or X7R MLCC capacitors in order to have better temperature performance and smaller capacitance tolerance. In order to suppress the output voltage ripple, the MLCC capacitor is also the best choice.

### Output Inductor Selection

The output inductor selection mainly depends on the amount of ripple current through the inductor $\Delta I_L$. Large $\Delta I_L$ will cause larger output voltage ripple and loss, but the user can use a smaller inductor to save cost and space. On the contrary, the larger inductance can get smaller $\Delta I_L$ and thus the smaller output voltage ripple and loss. But it will increase the space and the cost. The inductor value can be calculated as:

$$L = \frac{V_{PWR} - V_{OUT}}{\Delta I_L \times F_{SW}} \times \frac{V_{OUT}}{V_{PWR}}$$

For most applications, 6.8uH to 10uH inductors are suitable for CH1. 1.5uH to 2.2uH inductors are suitable for CH2.

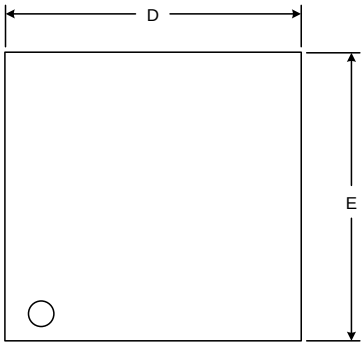
### PCB Layout Recommendations

Layout is very critical for PMIC designs. For EA3327 PCB layout considerations, please refer to the following suggestions to get best performance.

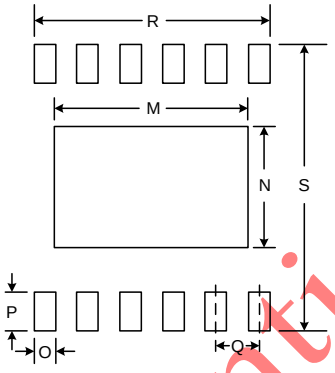
- The top layer SMD input and output capacitors ground plane should be connected to the internal ground layer and bottom ground plane individually by using vias.
- The AGND should be connected to inner ground layer directly by using via.
- High current path traces need to be widened.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.
- Keep the feedback path (from $V_{OUTX}$ to FBx) away from the noise node (ex. LXx). LXx is a high current noise node. Complete the layout by using short and wide traces.
- The top layer exposed pad ground plane should be connected to the internal ground layer and bottom ground plane by using a number of vias to improve thermal performance.

## Package Information

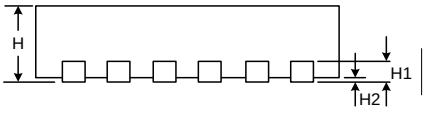
**DFN 3mm x 3mm-12 Package**



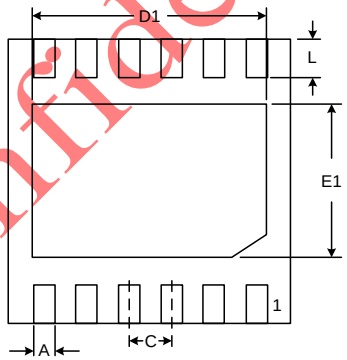

Top View




Recommended Layout Pattern




Side View




Bottom View

Unit: mm

| Symbol | Dimension Min | Dimension Max | Symbol | Dimension Typ |
|---|---|---|---|---|
| A | 0.16 | 0.28 | M | 2.50 |
| C | 0.40 | 0.50 | N | 1.50 |
| D | 2.90 | 3.10 | O | 0.30 |
| E | 2.90 | 3.10 | P | 0.80 |
| D1 | 2.40 | 2.60 | Q | 0.45 |
| E1 | 1.45 | 1.65 | R | 2.55 |
| L | 0.30 | 0.50 | S | 3.70 |
| H | 0.70 | 0.80 | | |
| H1 | 0.18 | 0.25 | | |
| H2 | 0.00 | 0.05 | | |