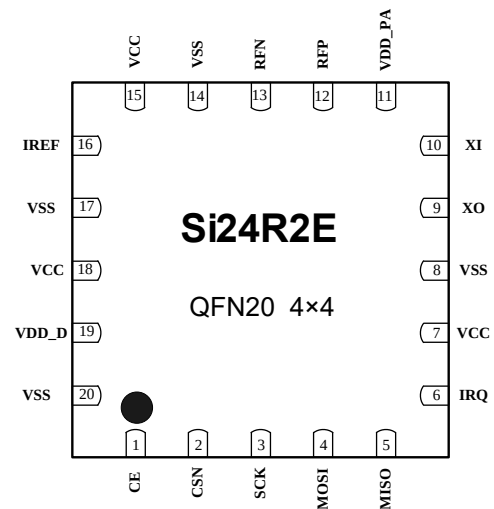


2.4GHz Ultra-low Power Active RFID System SOC Single Chip

Key Features

- 2.4GHz ISM band operation
- Built-in 128 programmable NVM memory
- Ultra-low power automatic transmission
- Low voltage automatic alarm function
- Tamper alarm function
- Integrated conflict prevention communication mechanism
- Built-in 3KHz RCOSC and hardware watchdog
- 3.3V programming voltage
- Modulation: GFSK
- Data rate: 2Mbps/1Mbps/250Kbps
- Ultra low shutdown current: 700nA
- Ultra low standby current: 15uA
- Start-up time: $\leq 130\mu\text{s}$
- Wide supply range: 1.9-3.6V
- Wide digital I/O voltage range: 1.9-5.25V
- Low-cost Crystal: 16MHz $\pm 60\text{ppm}$
- Maximum transmission power: 7dBm
- TX supply current (2Mbps): 13.5mA (0dBm)
- Maximum 10MHz, 4-pin hardware SPI
- Transmit data hardware interrupt output
- QFN20 package
- Compatible with Si24R1 and Si24R2 transmission function
- ◆ Electric bicycle anti-theft system
- ◆ Fixed assets regulatory system
- ◆ Smart parking lot management system

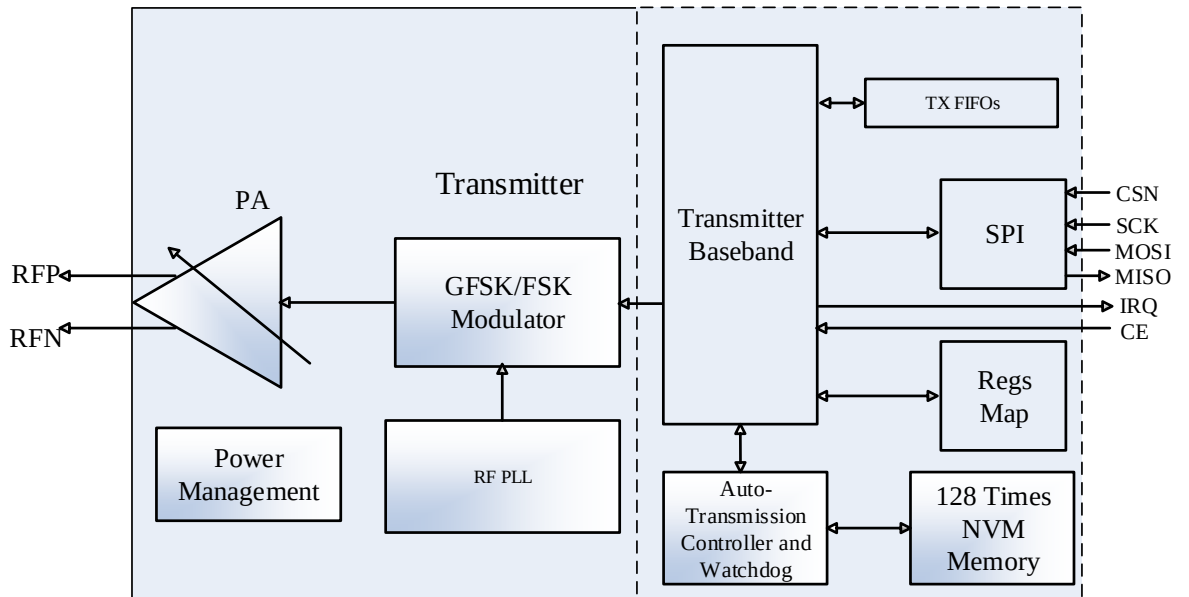
Pin Assignments



Applications

- ◆ Ultra low power active RFID system
- ◆ Smart campus card management system

Block diagram





Abbreviations

Abbreviations	Description
ARQ	Auto Repeat-reQuest
ART	Auto ReTransmission
ARD	Auto Retransmission Delay
ATR	Auto Transmission
BER	Bit Error Rate
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select
DPL	Dynamic Payload Length
GFSK	Gaussian Frequency Shift Keying
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
Mbps	Megabit per second
MCU	Micro Controller Unit
MHz	Mega Hertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
NVM	Non-volatile Memory
PA	Power Amplifier
PID	Packet Identity
PLD	Payload
RX	RX
TX	TX
PWR_DWN	Power Down
PWR_UP	Power UP
RF_CH	Radio Frequency Channel
RCOSC	RC Oscillator
RSSI	Received Signal Strength Indicator



Si24R2E

RX	Receiver
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TX	Transmitter
TX_DS	Transmit Data Sent
XTAL	Crystal
Watchdog	Hardware Watchdog



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1 Introduction

Si24R2E is a wireless transmission chip with embedded transmission baseband, operating in the 2.45GHz ISM frequency band, suitable for ultra-low power active RFID applications, integrated embedded 2.45GHz wireless RF transmitter, 128 programmable NVM memory, automatic transmission controller etc. The operating frequency band from 2400MHz to 2525MHz is divided into 126 RF channels. Integrated high PSRR LDO supply ensures that Si24R2E is stable within a wide voltage range of 1.9-3.6V.

Si24R2E uses GFSK digital modulation and demodulation. The air data rate can be programmed to 2Mbps, 1Mbps and 250Kbps. The higher data rate contributes the lower power consumption because it takes less time to transmit or receive signals. The output power of Si24R2E can be adjusted and it can base on actual application to configure the appropriate output power, thus saving the power of system.

Si24R2E is especially optimized for low power applications. All the register values and FIFO values are maintained in Shutdown mode and the shutdown supply current is 700nA. In Standby mode, the clock still works and the standby supply current is 15uA. It takes less than 130us to start data transmitting.

When Si24R2E enables automatic transmission function, internal watchdog and internal RCOSC clock works, internal timer starts timing and the chip works in Sleep state with only 700nA standby current. When internal timer is full, automatic transmission controller loads and transmits the data of NVM automatically. After transmitting data, chip enters Sleep state. The average power consumption of Si24R2E is very low, especially suitable for the application system of button cell power supply.

Si24R2E is easy to use, and it can automatically load and transmit data without external MCU. NVM memory can store the configuration of registers and data transmitted. The data will not be lost after power failure and can be maintained for more than 10 years. Under the 3.3V power supply voltage, the external MCU can complete the NVM configuration programming through the four-line interface of the chip without external high voltage. The maximum programmable number of the chip is 128 times. The chip supports the NVM locked to prevent the NVM configuration data back to read and ensure data security.

Si24R2E has very low cost of system application. To design an active RFID wireless

data transmission system, there are a few external passive components and no external MCU needed.

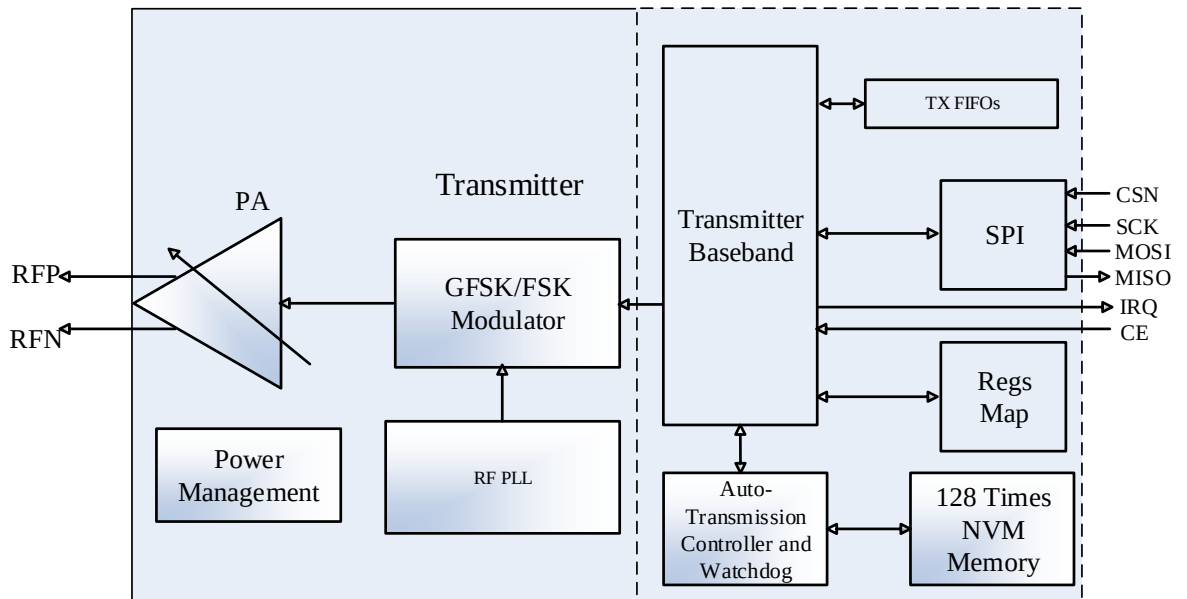


Figure 1-1 block diagram

2 Pin Information

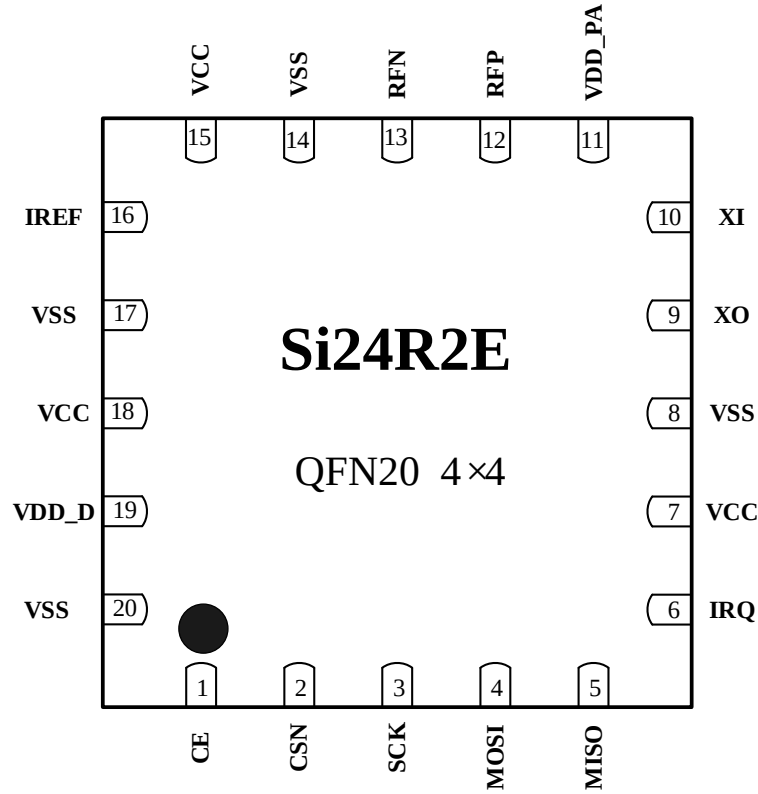


Figure 2-1 Si24R42E pin information (QFN20 4×4 package)

Table 2.1 pin function

Pin	Name	Type	Pin function
1	CE	DI	Turn the chip on, avoid disassembling
2	CSN	DI	SPI Chip Select
3	SCK	DI	SPI Clock
4	MOSI	DI	SPI Input
5	MISO	DO	SPI Output
6	IRQ	DO	Maskable interrupt pin. Active low
7/15/18	VCC	Power	Power supply (+1.9 ~ +3.6V, DC)
8/14/17/20	VSS	Power	Ground (0V)
9	XO	AO	Oscillator output
10	XI	AI	Oscillator input



Si24R2E

11	VDD_PA	Power	1.8V power supply output for the internal Power Amplifier
12	RFP	RF	Antenna port 1
13	RFN	RF	Antenna port 2
16	IREF	AI	Reference current
19	VDD_D	PO	Positive Digital Supply output for de-coupling purposes
	Die exposed	Power	Ground (0V), connect die exposed to PCB ground

3 Operational modes

3.1 State Control Diagram

The built-in state machine in Si24R2E controls the transitions between the chip's different operating modes.

The state transition diagram in Figure3-1 shows five operating modes of the Si24R2E. The five operating modes are: Shutdown、Standby、Idle-TX、TX and ATR.

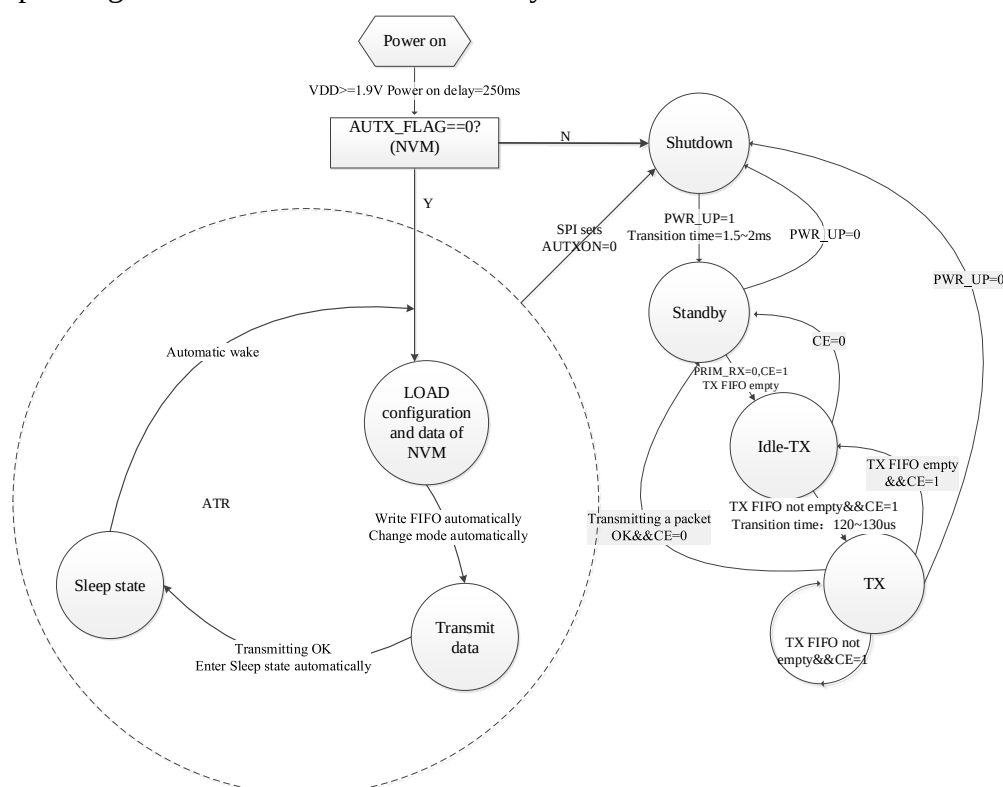


Figure 3-1 Si24R2E state control diagram

3.1.1 Shutdown Mode

When NVM makes the function of ATR inactive, AUTX_FLAG is high and the Si24R2E enters Shutdown mode directly after power-on. In Shutdown mode, Si24R2E is disabled and the current consumption is minimal. All register values available are maintained and can be written or read by SPI which is kept active. The shutdown supply current is 700nA. Shutdown mode is entered by clearing the PWR_UP bit in the CONFIG register.



3.1.2 Standby Mode

In Standby mode, only part of crystal oscillator is active. Standby mode ensures minimum average current consumption while maintaining short start-up time. Standby mode is entered after the crystal oscillator works stably by setting PWR_UP bit in the CONFIG register to 1. The crystal oscillator startup time is about 1.5~2ms, responding to the oscillator quality. The Si24R2E enters Idle-TX mode by setting CE high. When CE pin is set low, Si24R2E returns to Standby mode from Idle-TX mode or TX mode.

3.1.3 Idle-TX Mode

In Idle-TX mode, the crystal oscillator and clock buffers are active and more current is used compared to Standby mode. Idle-TX mode is entered when CE is set high and TX FIFO is empty on a PTX device. If a new packet is uploaded to the TX FIFO, the circuit inside the chip will be active immediately, TX mode is entered and the packet is transmitted.

Both in Standby and Idle-TX mode all register and FIFO values available are maintained and can be written or read by SPI.

3.1.4 TX Mode

The TX mode is an active mode for transmitting packets. When the PWR_UP is set high, the PRIM_RX is set low, a payload in the TX FIFO, and a high pulse on the CE pin for more than 10us, the Si24R2E enters this mode. Instead of switching directly from the Standby mode to the TX mode, Si24R2E should switch from the Standby mode to Idle-TX mode, and then switch to TX mode. The transition time from Idle-TX mode to TX mode takes 120us~130us, but will not exceed 130us. After transmitting a packet, if CE = 1, the status of TX FIFO determines the next mode. If the TX FIFO is not empty, the Si24R2E remains in TX mode and transmits the next packet. If the TX FIFO is empty, the Si24R2E returns to Idle-TX mode. If CE = 0, Si24R2E returns to Standby mode. The Si24R2E provides an interrupt after finishing a packet transmitting.

3.1.5 ATR Mode

When NVM makes the ATR active, AUTX_FLAG is low. When CSN is high, the Si24R2E will enter ATR mode after power-on, load the configuration of registers automatically from NVM and write data to FIFO. Data will be transmitted after the Si24R2E works stably, and then Si24R2E will enter Sleep state. In Sleep state, internal



hardware Watchdog, RCOSC and timer circuit work, all the register values are maintained, the current of the Si24R2E is about 700nA. Less time to transmit data and working mostly in Sleep state contribute to low average current consumption.

The retransmission of data can be configured in NVM, allows simple ALOHA protocol and automatic frequency hopping of three frequency points. It reduces the probability of conflict when multiple chips simultaneously transmit data.

When the ATR is active, external MCU writes the AUTX_ON command through SPI interface and then the function of ATR will be inactive. MCU can implement internal register configuration and data transmission through SPI interface. When MCU writes the same AUTX_ON command to reopen ATR, the Si24R2E will enter ATR mode.

AUTX_ON will be inactive after the software reset command executed or the Si24R2E power on, making the ATR active again.

When the ATR is active, the CSN of SPI must be pulled down and then pulled up (low voltage pulse) before external MCU writes the AUTX_ON command through SPI interface. Then CSN will be pulled down to write the AUTX_ON command.

In ATR mode, internal hardware Watchdog can be active automatically. If data is unsuccessfully sent three times in a row, the Si24R2E will reset automatically.

4 Packet processing protocol

Si24R2E is based on packet communication and uses the same packet format as Si24R1. Internal baseband engine can realize automatic packet handling without an extra MCU. Baseband supports the handling of 1 to 32 bytes dynamic payload length which is inside the packet. Besides, it supports static payload length which is set by registers. Baseband handling features automatic packet disassembly and assembly. It also has 3-stage FIFO for transmitting 3 packets of data at a time.

4.1 Packet format

A whole packet contains a preamble, address, packet control, payload and CRC field. Figure4-1 shows the whole packet.

Preamble	Address	Packet control	Payload	CRC
----------	---------	----------------	---------	-----

Figure 4-1 A whole packet

The preamble is used to synchronize the receiver demodulator to the incoming bit stream. It is automatically attached when transmitting and transparent to users.

The address field stores the packet address values for the receiver. A packet will be received only when the address of the packet matches the address of the receiver. The address field width in the AW register can be configured to be 3, 4 or 5 bytes.

Figure 4-2 shows the format of the 9 bit packet control field.

Payload length 6bit	PID 2bit	NO_ACK 1bit
---------------------	----------	-------------

Figure 4-2 Format of packet control field

The 6-bit payload length specifies the length of the payload in bytes ranges from 0 to 32 bytes.

For example: 000000 = 0 byte (no payload)

100000 = 32 byte (32 bytes of payload)

The PID field is used to tell the receiver if the received packet is new or retransmitted. PID prevents the PRX device from receiving the same payload more than once. The PID field is incremented at the PTX device when a new packet is written to FIFO through SPI.

The transmitter doesn't need to receive ACK. When NO_ACK equals 1, the RTX



device doesn't need to send ACK to the PTX device. The payload data field is transmission data content, which can be up to 32 bytes.

The CRC field is the CRC value in the packet. CRC supports either 8 or 16 bits, set by the CRCO bit in the CONFIG register.

A long string of 0 or 1 should be avoided in the packet. Otherwise it will disturb packet and affect the quality of communication.

4.2 Communication Mode

In the TX mode, the PTX device assembles the preamble, address, packet control field, payload and CRC to make a complete packet first and then it transmits the packet with RF module.

4.2.1 NO ACK Mode

The NO_ACK flag in control field will be set if using W_TX_PAYLOAD_NOACK to command the PTX writing TX PAYLOAD. After sending a packet of data, the PTX will generate TX_DS interrupt immediately, and start to prepare sending next packet of data. After receiving data, the PRX judge the NO_ACK flag setting and the data is valid, then generates RX_DR interrupt. Now a frame of data communication is done and the PRX needn't to transmit an ACK signal.

4.2.2 Dynamic payload length (DPL) and static payload length

A PTX device with DPL enabled must have the EN_DPL bit in FEATURE register and the DPL_P0 bit in DYNPD register set. The first 6 bits in the control field of the packaged data are the length of the data for sending.

The PRX set the EN_DPL bit in FEATURE register, and enable the pipe of DYNPD register. It will receive data according to the length control field. Thus, every time when receiving payload data, its length can be different. MCU can read out the payload length by using R_RX_PL_WID command. If it is static payload length by default, the payload length every time the PTX sending should be the same, and the value should be the same as RX_PW_PX registers set by the receiver.

4.3 Compatibility Mode

Si24R2E can provide another packet format, Figure4-3 shows the whole packet:

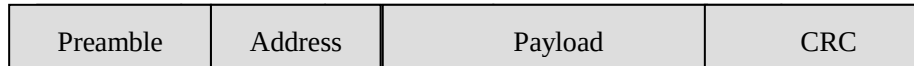


Figure 4-3 Another packet format

In Compatibility mode, EN_AA should be set low. DPL mode is inactive, DPL_PX and EN_DPL should be set low. The receiver should set RX_PW_PX for PTX sending the length of packet, set DPL_PX and EN_DPL to low. What's more, the data rate can only be set as 1Mbps or 250kbps.

5 SPI Interface

The SPI interface is a standard 4-wire SPI with a maximum data rate of 10 Mbps. MCU can configure the Si24R2E through SPI interface, including R/W register、read and write FIFO、read the status of Si24R2E、clear the interrupts etc.

5.1 SPI Commands

Table 5-1 shows the SPI commands, and every new command must be started by a high to low transition on CSN pin. Every time a SPI operation, the first byte output by MISO is the value of the STATUS register, then the command determines whether to output the value (never output HRS value).

- <Command byte: MSBit to LSBit > -- one byte
- <Data bytes: LSByte to MSByte, MSBbit to LSBbit of every byte first >

For details, please refer to SPI timing, Figure 5-1 & Figure 5-2.

ATTENTION: When ATR is active, AUTX_ON command should be executed firstly and ATR should be close before other command. The CSN of SPI must be pulled down and then pulled up (low voltage pulse) before executing the AUTX_ON command through SPI interface. Then CSN will be pulled down to execute the AUTX_ON command.

Table 5-1 SPI Commands

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read register command, AAAAA= 5bit Register address (refer to register table)
W_REGISTER	001A AAAA	1 to 5 LSByte first	write register command, AAAAA= 5bit Register address (refer to register table) Executable in Shutdown 、 Standby or Idle-TX modes only
FLUSH_TX	1110 0001	0	Flush TX FIFO , used in TX mode
REUSE_TX_PL	1110 0011	0	Used for PTX The command can't be used after flushing TX FIFO or writing new data to FIFO
W_TX_PAYLOAD _NO ACK	1011 0000	1 to 32 LSByte first	Used in TX mode. AUTOACK should be set 1 when using this command
SW_RST	01100011	0	Software Reset command, reset the registers which in NVM. If NVM is programmed and ATR is active, Si24R2E will enter ATR mode after



			software reset.
AUTX_ON	01011100	1	Write 0x5C command and send 0xA7 to force closing or open ATR function. The command can close ATR and allow MCU to operate register table. The command will fail after hardware or software reset. AUTX_FLAG in NVM determines whether the ATR function is open.
NOP	1111 1111	0	No operation. Can be used to get the value of STATUS register

5.2 SPI Timing

SPI operation includes basic read or write operation and other command operation. Figure 5-1 & Figure 5-2 show the SPI timing.

Attention: The configuration registers can only be written in Shutdown/Standby/Idle-TX mode and ATR mode.

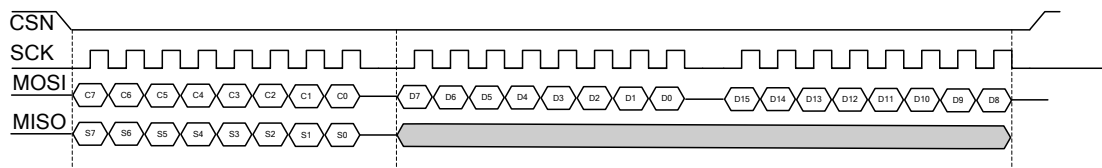


Figure 5-1 SPI write operation

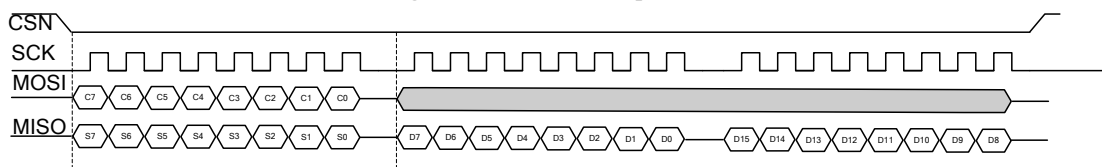


Figure 5-2 SPI read operation

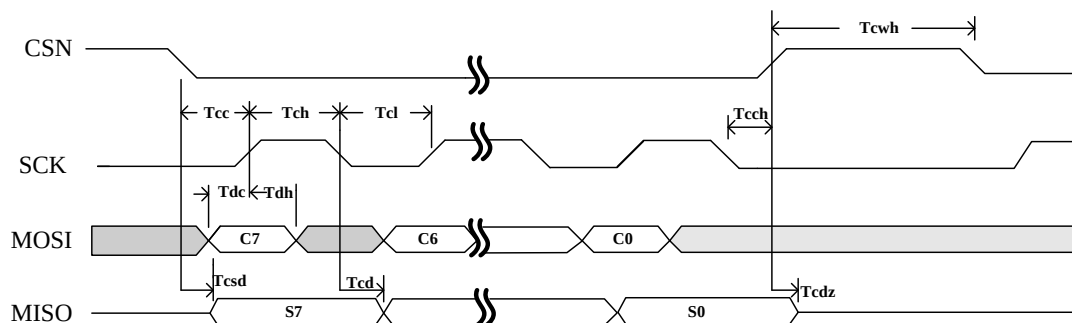


Figure 5-3 SPI typical timing



Table 5-2 shows SPI Interface typical timing parameter

Table 5-2 SPI Interface typical timing parameter

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

6 Register Table

Attention: Register is valid for accessing only when ATR function is turned off. When ATR function is active, register table can't affect ATR function.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Reserved, Only '0' allowed
	Reserved	6	0	R/W	Reserved, Only '0' allowed
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	Reserved	4	0	R/W	Reserved, Only '0' allowed
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high 0: close CRC 1: open CRC
	CRCO	2	0	R/W	CRC encoding scheme 0: 1 byte 1: 2 bytes
	PWR_UP	1	0	R/W	Power up/down control 1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	0
01	EN_AA				
	7: 6		Reserved	R	
	5:0		111111	R/W	In NOCRC, all bits are low. In Compatibility mode, all bits are low, set ARC to 0
02	Reserved				
03	SETUP_AW				Setup of Address Widths
	Reserved	7:2	000000	R/W	Reserved, only '000000' allowed
	AW	1:0	11	R/W	TX Address field width 00: illegal 01:3 bytes 10:4 bytes



Si24R2E

					11: 5 bytes
04	Reserved				
05	RF_CH				RF channel
	Reserved	7	0	R/W	Reserved, only '0' allowed
	RF_CH	6:0	0000010	R/W	Set channel when Si24R2E works, corresponding to 0~125 channels respectively. The space of channels is 1MHz. The default is 02, which is 2402MHz.
06	RF_SETUP				RF Setup
	CONT_WAVE	7	0	R/W	1: Continuous carrier transmit, for test only
	Reserved	6	0	R/W	Reserved, only '0' allowed
	RF_DR_LOW	5	0	R/W	Set RF data rate to 250kbps、1Mbps or 2Mbps together with RF_DR_HIGH
	PLL_LOCK	4	0	R/W	Reserved, only '0' allowed
	RF_DR_HIGH	3	1	R/W	Set RF data rate [RF_DR_LOW, RF_DR_HIGH]: 00: 1Mbps 01: 2Mbps 10: 250kbps 11: reserved
	RF_PWR	2:0	110	R/W	Set RF output power in TX mode 111: 7dBm 110: 4dBm 101: 3dBm 100: 1dBm 011: 0dBm 010: -4dBm 001: -6dBm 000: -12dBm
07	STATUS				Status Register (The first byte operated by SPI, the STATUS register is shifted serially out on the MISO pin)
	Reserved	7	0	R/W	Reserved, only '0' allowed
	Reserved	6	0	R/W	Reserved, only '0' allowed
	TX_DS	5	0	R/W	Data sent TX FIFO interrupt Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received Write 1 to clear bit
	Reserved	4:1	0	R/W	Reserved, only '0' allowed
	TX_FULL	0	0	R	TX FIFO full flag



Si24R2E

08	Reserved				
09	Reserved				
0A	Reserved				
0B	Reserved				
0C	Reserved				
0D	Reserved				
0E	Reserved				
0F	Reserved				
10	TX_ADDR	39:0	0xE7E7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSB byte is written first) Set RX_ADDR_P0 equal to this address and enable ARQ if PTX needs to receive ACK signal.
11	Reserved				
12	Reserved				
13	Reserved				
14	Reserved				
15	Reserved				
16	Reserved				
17	FIFO_STATUS				FIFO state
	Reserved	7	0	R/W	Reserved, only '0' allowed
	TX_REUSE	6	0	R	Used for PTX, Reuse last transmitted data packet by the SPI command REUSE_TX_PL, and is reset by the SPI command W_TX_PAYLOAD or FLUSH_TX
	TX_FULL	5	0	R	TX FIFO full flag 1: TX FIFO full 0: TX FIFO not full
	TX_EMPTY	4	1	R	TX FIFO empty flag 1: TX FIFO empty 0: TX FIFO not empty
	Reserved	3:0	00	R/W	Reserved, only '0000' allowed



Si24R2E

1C	DYNPD				Enable dynamic payload length
	Reserved	7:1	0000000		
	DPL_P0	0	0		1: Enable dynamic payload length
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Reserved, only '00000' allowed
	EN_DPL	2	0	R/W	1: Enable dynamic payload length
	Reserved	1:0	0	R/W	Reserved, only '01' allowed



7 Electrical specification

7.1 Limitation parameter

Operating Condition	Min.	Max.	Unit
Supply Voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input Voltage			
VI	-0.3	5.25	V
Output Voltage			
VO	VSS to VDD	VSS to VDD	V
Power Dissipation			
		100	mW
Temperatures			
Operation Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C
ESD Performance	HBM(Human Body Model): Class 1C		

7.2 Electrical specification

Conditions: VDD = 3V, VSS = 0V , TA = 27°C , crystal oscillator CL=12pF

Symbol	parameter	Min.	Typ.	Max.	Unit.	Comment
OP Parameters						
VDD	Supply voltage	1.9		3.6	V	
ISHD	Supply current in Shutdown mode		0.7		μA	
Isleep	Supply current in Sleep mode		0.7		uA	RCOSC, Watchdog and ATR Timer are active
ISTB	Supply current in Standby mode		15		μA	
IDLE	Supply current in		380		μA	



Si24R2E

	Idle-TX mode					
$I_{TX@7dBm}$	TX mode supply current @7 dBm output power		25		mA	
$I_{TX@4dBm}$	TX mode supply current @4 dBm output power		17		mA	
$I_{TX@0dBm}$	TX mode supply current @0 dBm output power		13.5		mA	
$I_{TX@-6dBm}$	TX mode supply current @-6 dBm output power		10		mA	
$I_{TX@-12dBm}$	TX mode supply current @-12 dBm output power		8.5		mA	
RF Parameter						
F_{OP}	RF operation frequency	2400		2525	MHz	
F_{CH}	RF channel space	1			MHz	2MHz at least when 2Mbps
$\Delta F_{MOD}(2Mbps)$	Frequency deviation		± 330		KHz	
$\Delta F_{MOD}(1M/250 Kbps)$	Frequency deviation		± 175		KHz	
R_{GFSK}	Data rate	250		2000	Kbps	
TX Parameter						
P_{RF}	RF Output Power	-30		7	dBm	
$P_{BW@2Mbps}$	Modulation Bandwidth		2.1		MHz	
$P_{BW@1Mbps}$	Modulation Bandwidth		1.1		MHz	
$P_{BW@250Kbps}$	Modulation Bandwidth		0.9		MHz	



Si24R2E

P _{RF1}	1 st Adjacent CH Power 2MHz			-20	dBm	
P _{RF2}	2 nd Adjacent CH Power 4MHz			-46	dBm	
Crystal Oscillator Parameter						
F _{XO}	Crystal frequency		16		MHz	
ΔF	Tolerance		±60		ppm	
ESR	Equivalent Series Resistance		100		Ω	

8 Package

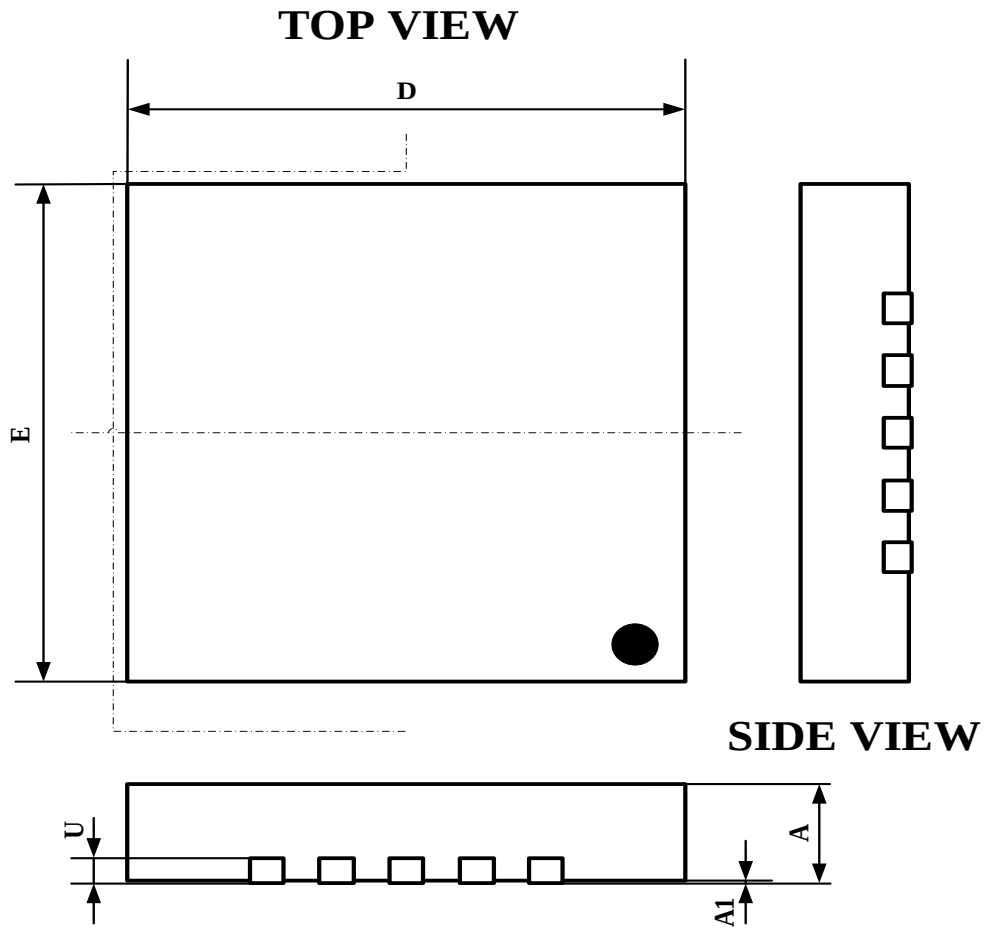


Figure 8-1 Top view

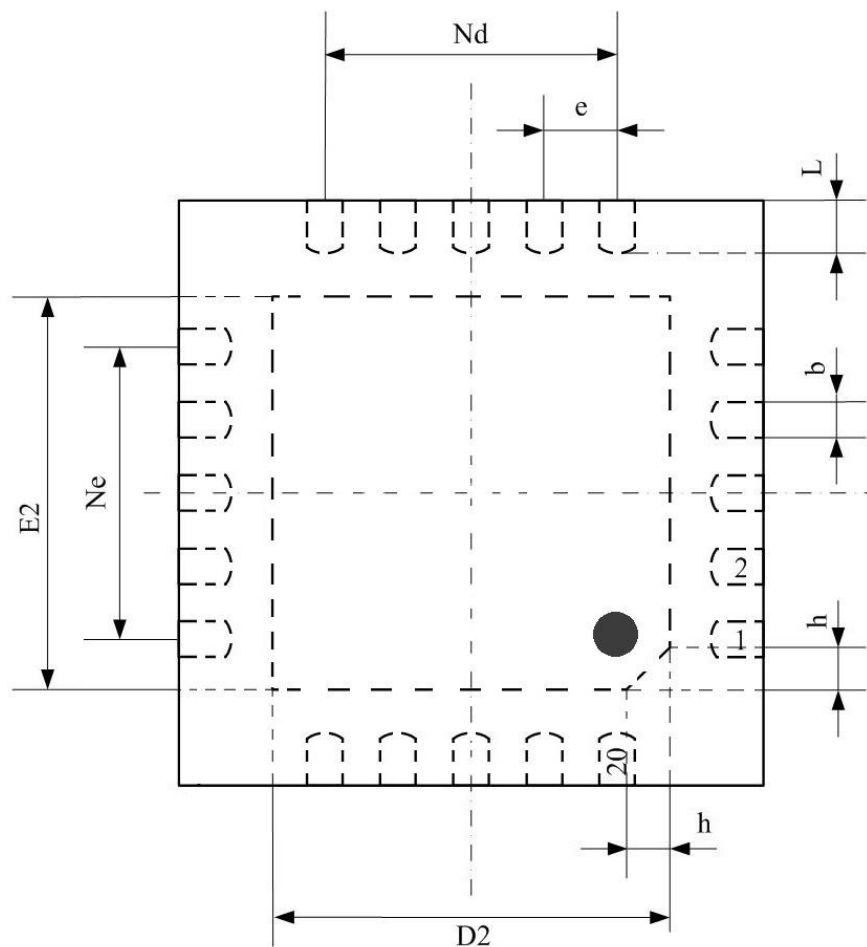


Figure 8-2 Package measurement (Top view)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
e	0.50BSC		
E2	2.55	2.65	2.75
E	3.90	4.00	4.10
Ne	2.00BSC		
Nd	2.00BSC		
L	0.35	0.40	0.45



Si24R2E

h	0.30	0.35	0.40
U	0.20 REF.		
L/F (mil)	114×114		

9 Typical Application Schematic

9.1 Typical Application Schematic

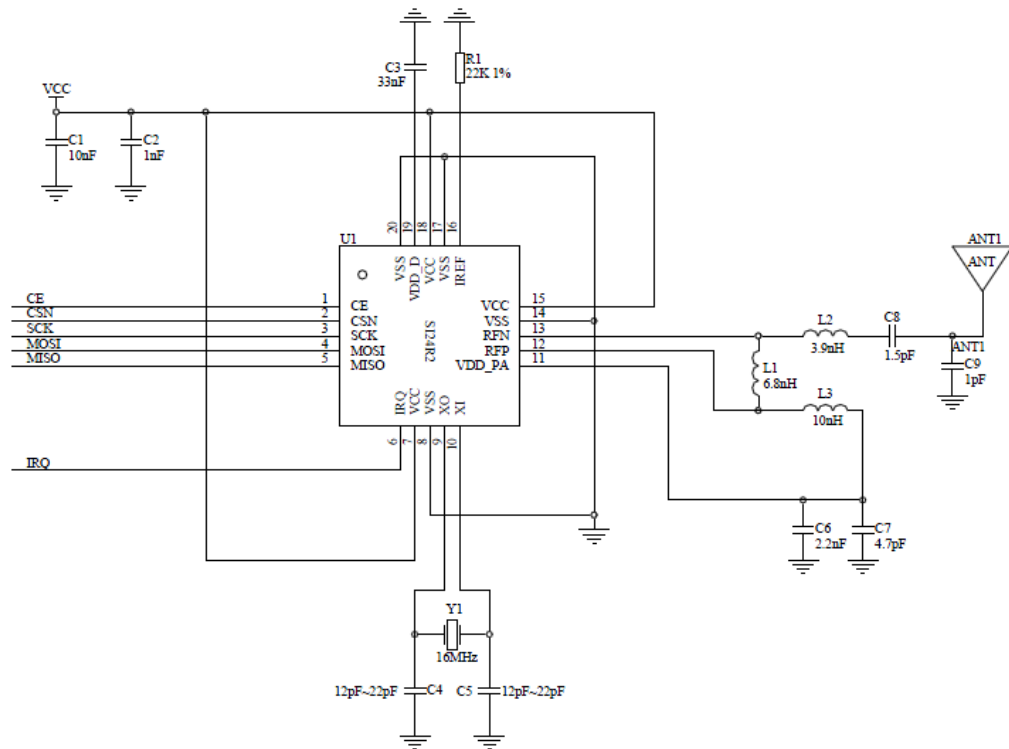


Figure 9-1 external MCU application schematic

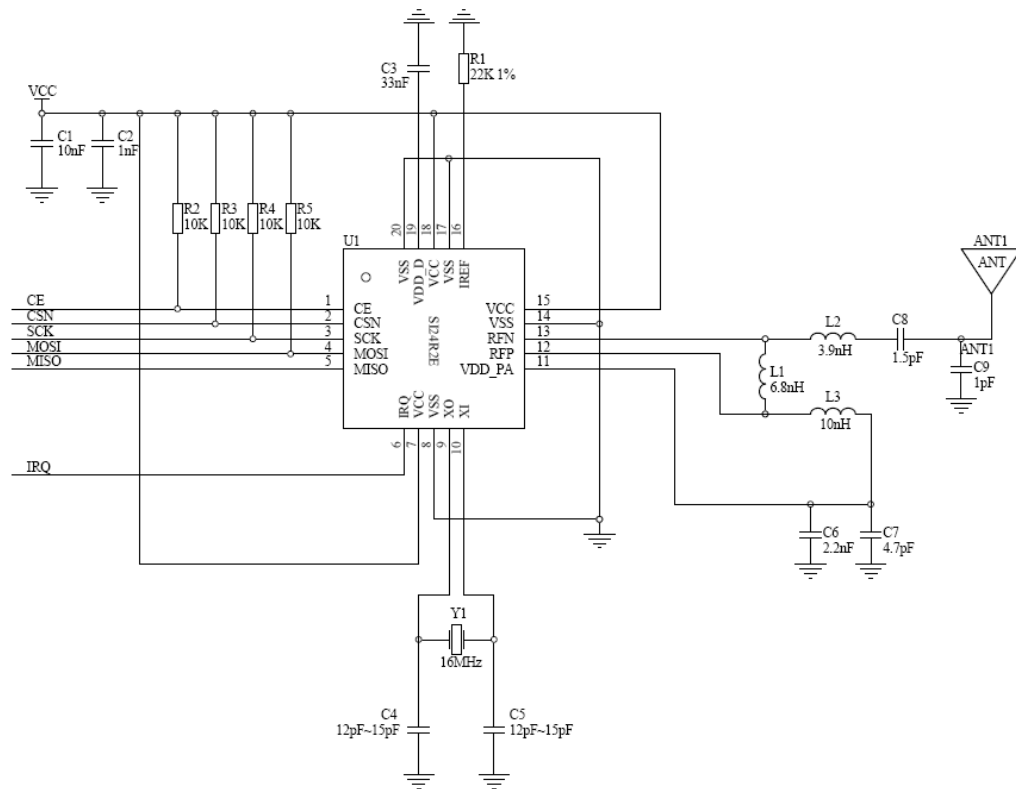


Figure 9-2 application schematic with ATR function

Table 9-1 Recommended components (BOM)

name	value	form	description
C1	10nF (100uF) *	0402	X7R, +/- 10%
C2	1nF	0402	X7R, +/- 10%
C3	33nF	0402	X7R, +/- 10%
C4	12~22pF	0402	NPO, +/- 2%
C5	12~22pF	0402	NPO, +/- 2%
C6	2.2nF	0402	X7R, +/- 10%
C7	4.7pF	0402	NPO, +/- 0.25pF
C8	1.5pF	0402	NPO, +/- 0.1pF
C9	1.0pF	0402	NPO, +/- 0.1pF
L1	6.8nH	0402	chip inductor, +/- 5%
L2	3.9nH	0402	chip inductor, +/- 5%
L3	10nH	0402	chip inductor, +/- 5%
R1	22KΩ	0402	+/- 1%
R2	10KΩ	0402	+/- 10%



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R3	10K Ω	0402	+/- 10%
R4	10K Ω	0402	+/- 10%
R5	10K Ω	0402	+/- 10%
Y1	16MHz		+/-60ppm, CL=12pF
U1		QFN20 04×04	

ATTENTION: When system can't provide stable supply voltage (e.g. powered by button batteries), 100nF capacitor is recommended to use to stabilize voltage. Meanwhile, large leakage current is not allowed in the capacitor.

The transmitter in Si24R2E will be controlled by external MCU after using AUTX_ON command through SPI, configuring AUTXON to 0 and close ATR function. AUTX_ON can be found in manual SI24R2E_NVM.

Pin CE, CSN, SCK, MOSI, MISO and IRQ is the programming interface. In ATR mode, output pins (MISO and IRQ) are hanging. Input pins (CE, CSN, SCK and MOSI) are connected to supply voltage through pull-up resistor.

9.2 PCB layout

As shown in the figure below is the PCB layout example for the typical application schematic above. A double-sided FR-4 board is used. There is a copper clad surface on the top and bottom layers respectively, the copper clad surfaces of the top and bottom layers are connected by a large number of vias, and there is no copper clad surface under the antenna. The bottom layer of PCB is the ground plane. To achieve better RF performance, the IC substrate die ground (die attach) should connect to PCB ground plane. It is strongly recommended to keep it connected.

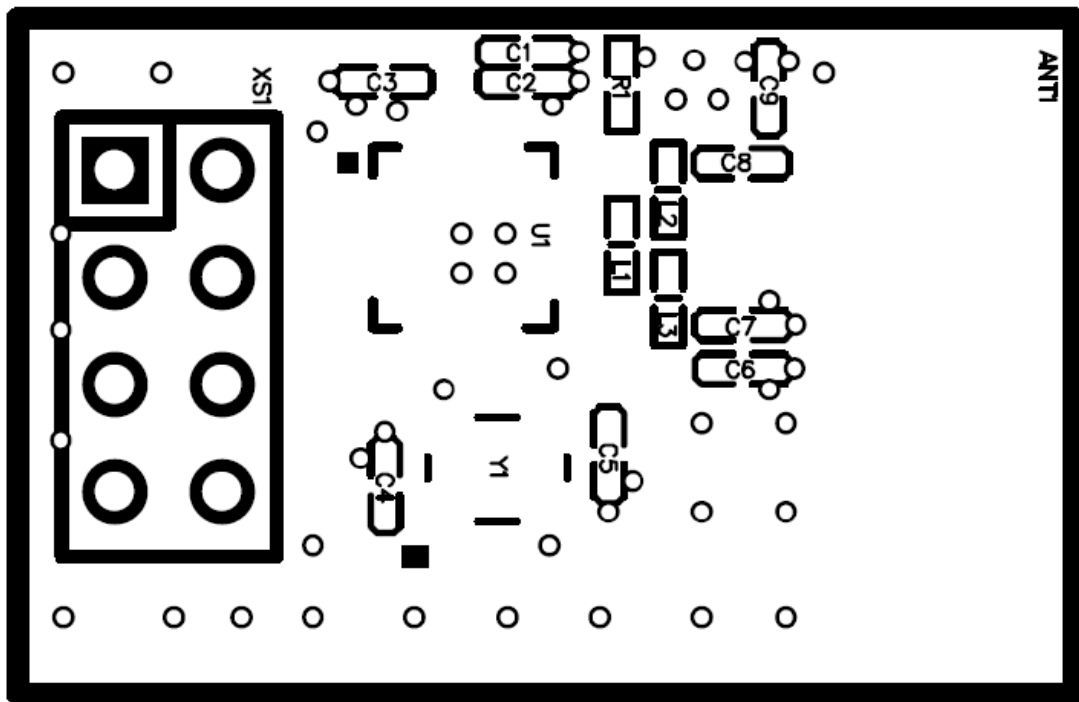


Figure 9-1 Top overlay (0402 size passive components)

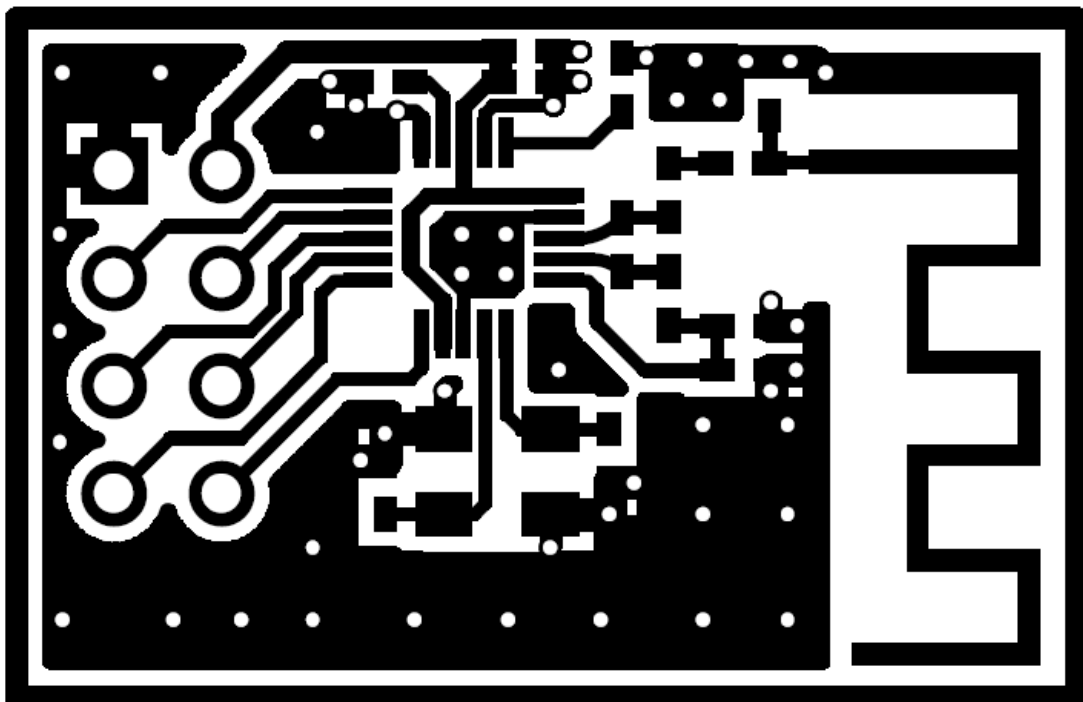


Figure 9-2 Top layer (0402 size passive components)

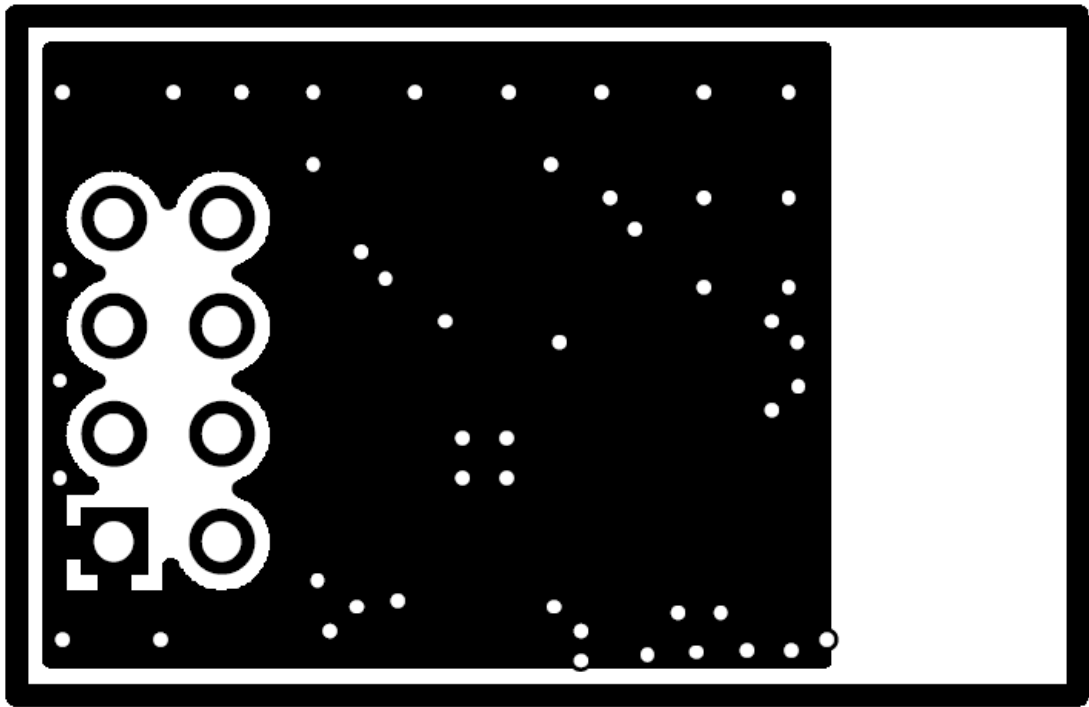


Figure 9-4 Bottom layer

10 Version Information

Version	Modified date	Modified content
V1.0	2021/12/02	Modifying contact information
V1.1	2022/10/24	Modifying order information
V1.2	2024/1/30	Modify the description of SW_RST command



11 Order Information

Package marking

Si24R2E
ABBCDEE

Si24R2E: chip code

A: package date code, 5 represents year 2020

BB: week of sending out processing, 42 represents in the year A the 42th week

C: package factory code, A、HT、NJ or WA, can also abbreviated as A、H、N or W

D: test factory code, A、Z or H

EE: production batch code

Table 11-1 Si24R2E order example

order code	package	container	minimum
SI24R2E-Sample	4×4mm 20-pin QFN	Box/Tube	5
SI24R2E	4×4mm 20-pin QFN	Tape and reel	4K



12 Technical Support and Contact Information

Nanjing Zhongke Microelectronic Industry Technology Research Institute Co., Ltd

Technical Support Center

Phone: 025-68517780

Address: Room 201, Building B, Research Zone 3, Xuzhuang Software Park, Xuanwu District, Nanjing,
Jiangsu, China

Website: <http://www.csm-ic.com>

Sales and Marketing

Phone: 13645157034, 13645157035

Email: sales@csmic.ac.cn

Technical Support

Phone: 13645157034

Email: supports@csmic.ac.cn



Appendix - Configuration and communication example

PTX Configuration (Si24R2E):

```
spi_write_buf( TX_ADDR, TX_ADDRESS, 5);      // write in TX address
spi_rw_reg( FEATURE, 0x01);    // Enable W_TX_PAYLOAD_NOACK
spi_write_buf(W_TX_PAYLOAD_NOACK, buf, TX_PLOAD_WIDTH); // write data in TX FIFO
spi_rw_reg(SETUP_AW, 0x03);      // 5 byte Address width
spi_rw_reg( RF_CH, 0x40);        // configure RF channel 0x40
spi_rw_reg(RF_SETUP, 0x08);      // configure TX data rate=2Mbps
spi_rw_reg( CONFIG, 0x0e);      // set TX MODE, enable CRC and CRC length is 2bytes
CE = 1;
```

PRX Configuration (Si24R1):

```
spi_write_buf( RX_ADDR_P0, TX_ADDRESS, 5);  // write in RX address
spi_rw_reg( EN_RXADDR, 0x01);    // Enable data pipe 0
spi_rw_reg( RF_CH, 0x40);        // configure RF channel
spi_rw_reg( RX_PW_P0, TX_PLOAD_WIDTH);      // configure pipe 0 payload length
spi_rw_reg( RF_SETUP, 0x08);      // configure TX data rate=2Mbps, TX power=-18dbm
spi_rw_reg( CONFIG, 0x0f);      // set RX MODE, enable CRC and CRC length is 2bytes
CE = 1;
```