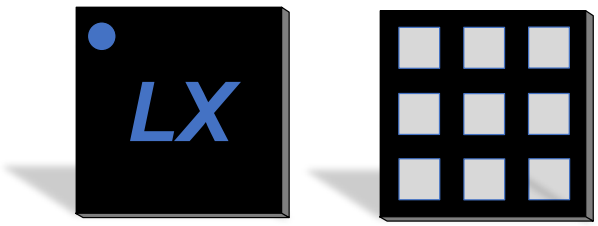

Product Features

- Excellent Insertion Loss and Isolation performance
- High Linearity
- RFFE 2.1 Control Interface
- Broadband frequency range: 0.1 to 6 GHz
- Small package: LGA-9 1.1mm x 1.1mm x 0.46mm
- No DC blocking capacitors required
- 1kV HBM ESD Protection on all pins

Product Applications

- 5G multimode cellular
- Diversity antenna switching

Product Description

The LX8648M is a Silicon On Insulator (SOI) Single Pole, Four-Throw (SP4T) antenna switch with a Mobile Industry Processor Interface (MIPI) which require very low insertion loss, high isolation and high linearity performance.

The high linearity performance and low insertion loss for 5G NR, UMTS, CDMA2000, and LTE applications.

The LX8648M is manufactured in a compact 1.1 x 1.1 x 0.46mm, 9-pin surface mount LGA package.

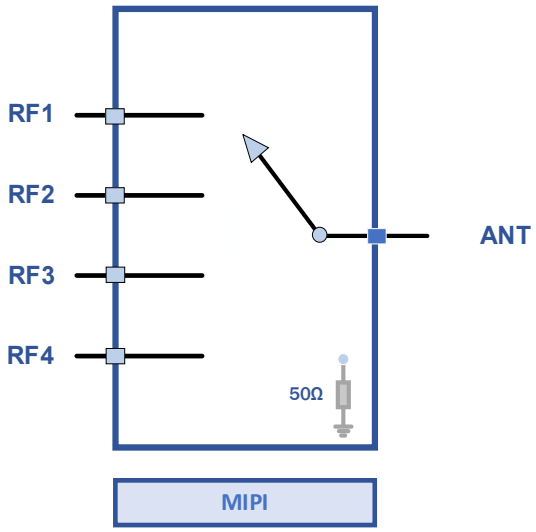

Figure 1 Functional Block Diagram

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Absolute Maximum Conditions

Parameters	Symbol	Minimum	Maximum	Units
Digital control signal	V_{IO}	-0.3	2.5	V
RF input power	Pin		+40	dBm
Storage temperature	T_{STG}	-55	+150	℃
Operating temperature	T_{OP}	-40	+90	℃
Human Body Model, Class 1C	ESD	1000		V

1: Test condition 50% duty cycle, VSWR=1:1, +25 ° C

Note: *Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.*

General Electrical Specifications

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Interface supply	VIO		1.65	1.80	1.95	V
Interface signal: High Low	 VIH VIL		 0.8 x VIO 0	 VIO 0	 VIO 0.2 x VIO	V
Control current: High Low	I_{CTL}		4		10	μA
Turn-on time	T_{ON}	Measured from 50% of final VDD supply voltage to 90% of RF power			20	μs
Switching time	T_{SW}	Measured from 50% of final VDD supply voltage to 90%/10% of RF power		1.2	1.5	μs

(VIO = 1.8 V, VIH = 1.8 V, VIL = 0 V, PIN=0dBm, TOP = +25 ℃, Characteristic Impedance [ZO] = 50 Ω, Unless Otherwise Noted)

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RF Specifications

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating frequency	f		0.1		6	GHz
Insertion loss	IL	Up to 1.0 GHz Up to 2.0 GHz Up to 3.0 GHz Up to 4.8 GHz Up to 6.0 GHz	0.33 0.45 0.48 0.50 0.75	0.37 0.50 0.55 0.58 0.90		dB
Isolation (ANT port to any receive port)	I_{SO}	Up to 1.0 GHz Up to 2.0 GHz Up to 3.0 GHz Up to 4.8 GHz Up to 6.0 GHz	35 30 25 16 12	40 35 30 20 15		dB
Return loss	RL	All ports, up to 3.0 GHz All ports, up to 6.0 GHz	12 9	15 12		dB
2nd Order harmonics	2fo	Pin = +26 dBm,900MHz Pin = +35 dBm,900MHz	-78 -58	-76 -56		dBm
3rd Order harmonics	3fo	Pin = +26 dBm,900MHz Pin = +35 dBm,900MHz	-82 -58	-80 -56		dBm
0.1 dB Compression Point 50% duty cycle, VSWR=1:1	P0.1dB	900M, 50Ω		+40		dBm

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Truth Table

Reg_1C	Reg_00								ANT-RFX
	D7	D6	D5	D4	D3	D2	D1	D0	
38	0	0	0	0	0	0	0	0	ISO
38	0	0	0	0	0	0	0	1	ANT-RF1 on
38	0	0	0	0	0	0	1	0	ANT-RF2 on
38	0	0	0	0	0	1	0	0	ANT-RF3 on
38	0	0	0	0	1	0	0	0	ANT-RF4 on

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Register definition

Register 0, Address: 0x00 (MODE_CTRL)				
Register 0	**Description**	**Default**	**Notes**	**Trig**
[7:0]	RF Control	0x0	Switch control. See Truth Table	Yes
Register 1B, Address: 0x1B				
Register 1B	**Description**	**Default**	**Notes**	**Trig**
[7:4]	Reserved	0x00	Reserved	No
[3:0]	GSID	0x00	Group slave ID	No
Register 1C Address: 0x1C (PM_TRIG)				
Register 1C	**Description**	**Default**	**Notes**	**Trig**
[7]	PWR_MODE_1	0b1	00 = Normal Operation (ACTIVE) 01 = Default Settings (STARTUP) 10 = Low Power (LOW POWER) 11 = Reserved	No
[6]	PWR_MODE_0	0b0	00 = Normal Operation (ACTIVE) 01 = Default Settings (STARTUP) 10 = Low Power (LOW POWER) 11 = Reserved	No
[5]	Trigger Mask 2	0b0	Trigger Enable: 0 Trigger Disable: 1	No
[4]	Trigger Mask 1	0b0	Trigger Enable: 0 Trigger Disable: 1	No
[3]	Trigger Mask 0	0b0	Trigger Enable: 0 Trigger Disable: 1	No
[2]	Trigger Register 2	0b0	1 = Latch Register 2 contents	No
[1]	Trigger Register 1	0b0	1 = Latch Register 1 contents	No
[0]	Trigger Register 0	0b0	1 = Latch Register 0 contents	No
Register1D, Address: 0x01D (PM_ID)				
Register1D	**Description**	**Default**	**Notes**	**Trig**
[7:0]	Product ID	0X72	Product ID = 0X72	No
Register 1E, Address: 0x01E (MAN_ID)				
Register1E	**Description**	**Default**	**Notes**	**Trig**
[7:0]	MANUFACTURER_ID	0x78	Manufacturer ID [7:0] = 0x78	No
Register 1F Address: 0x01F (USID)				
Register 1F	**Description**	**Default**	**Notes**	**Trig**
[7:4]	Manufacturer ID	0x2	Manufacturer ID [11:8] = 0x02	No
[3:0]	User ID	0x8	The default value at reset is selected via pin USID.	No

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Pin-out Information

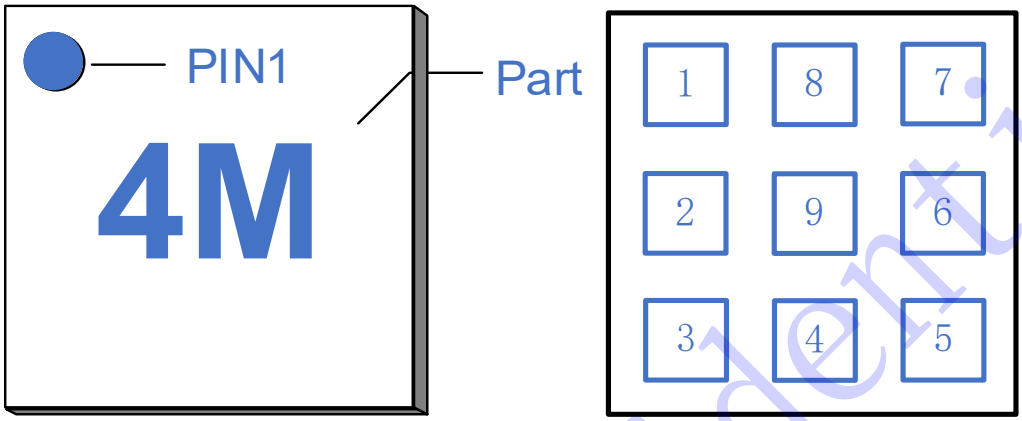

Figure 2 Pin-out Information

Table 1. Pin Description

Pin #	Name	Description	Pin #	Name	Description
1	VIO	Digital control signal	6	RF3	RF Port 3
2	RF4	RF Port 4	7	SDATA	MIPI data input/output
3	RF2	RF Port 2	8	SCLK	MIPI clock
4	ANT	Antenna Port	9	GND	Ground
5	RF1	RF Port 1			

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Application circuit

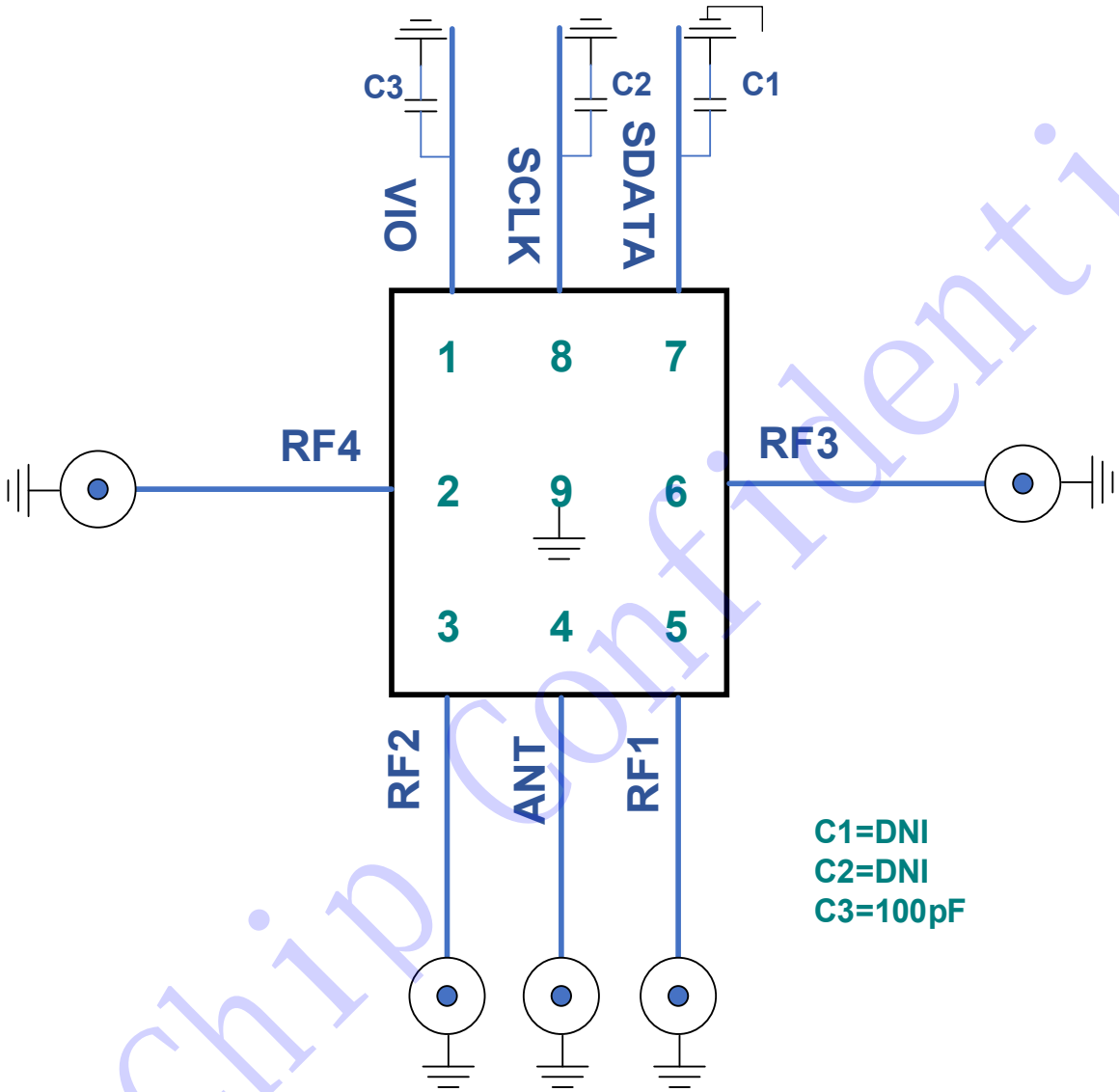

Figure 3 Application circuit

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Evaluation Board

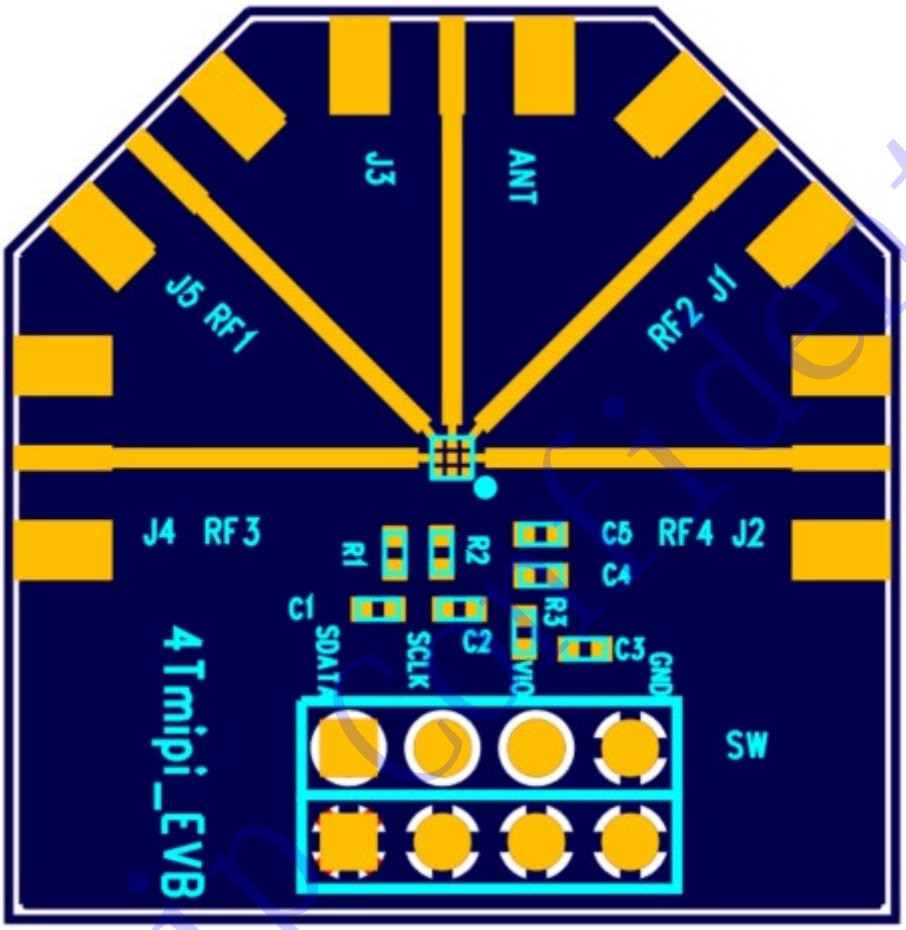

Figure 4 Evaluation Board Assembly Diagram

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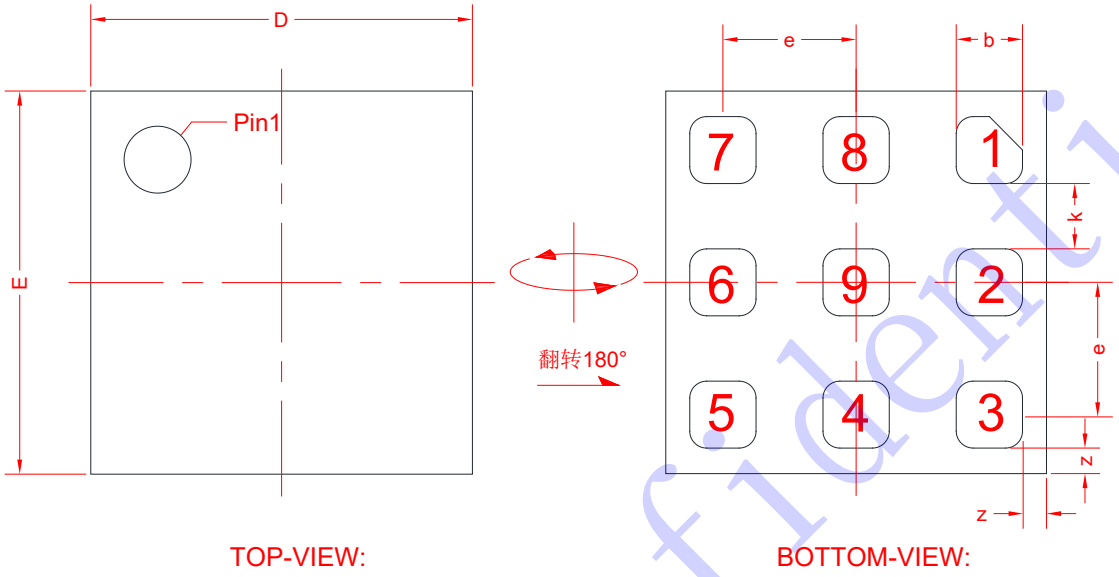
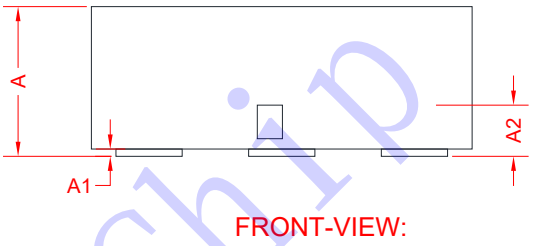
Package Outline Dimension





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.41	0.46	0.51
A1	0.00	0.02	0.05
A2		0.127REF	
b	0.17	0.20	0.23
D	1.05	1.10	1.15
E	1.05	1.10	1.15
e	0.35	0.40	0.45
k	0.17	0.20	0.23
z		0.05REF	

Figure 5 Package Outline Dimension

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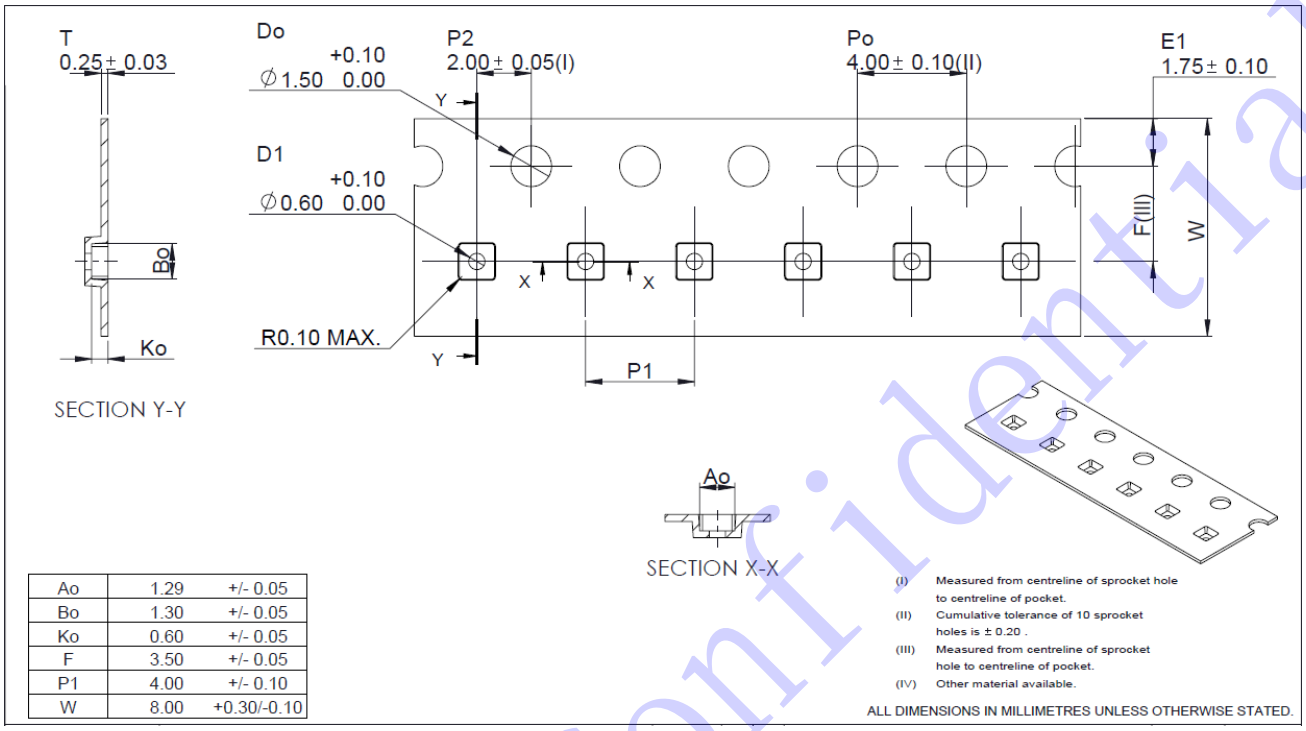
Package Dimensions (5000pcs)



Ao	1.29	+/- 0.05
Bo	1.30	+/- 0.05
Ko	0.60	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+0.30/-0.10

Figure 6 Tape and Reel Dimensions

Declaration of No Harmful Substances

This part is compliant with 2005/20/EC packaging directive, 1907/2006/EC REACH directive and the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

• Lead free

• Halogen Free (Chlorine, Bromine)

• SVHC Free

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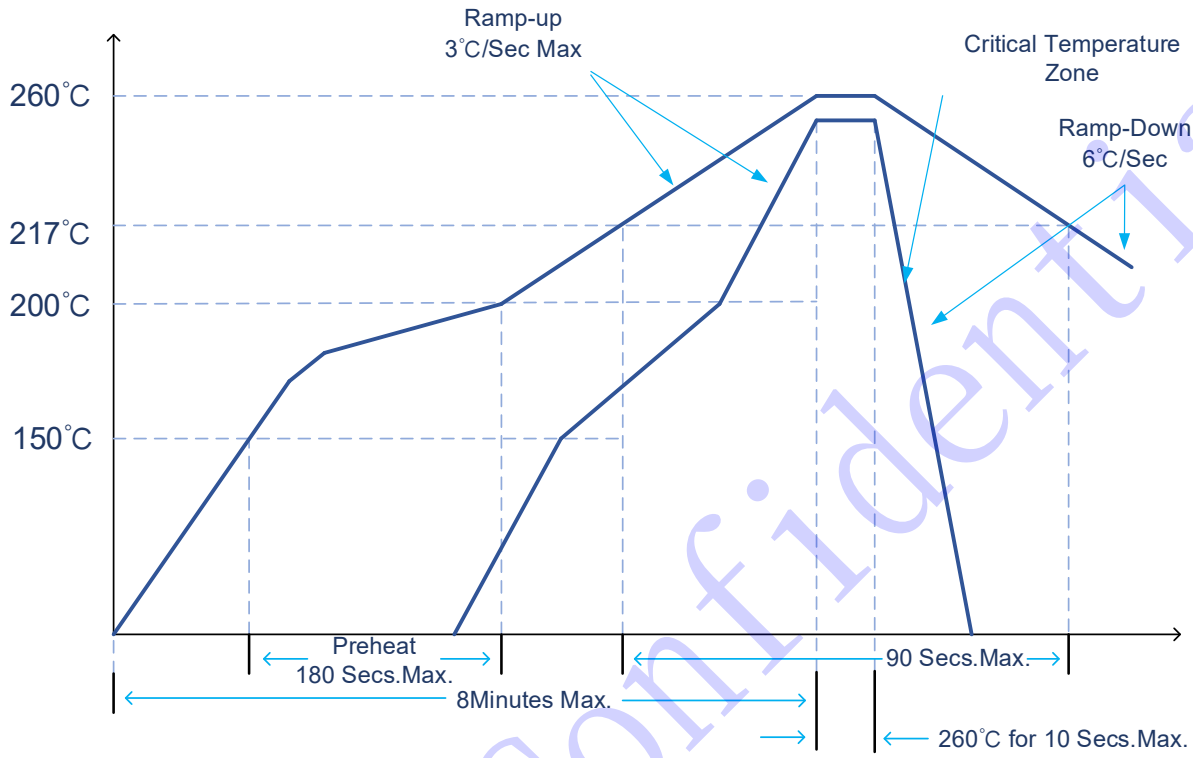
Reflow Chart



NOTE: Reflow Profile with 240°C peak also acceptable.

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