1. DESCRIPTION

The XD14016 quad bilateral switch is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each XD14016 consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

2. FEATURES

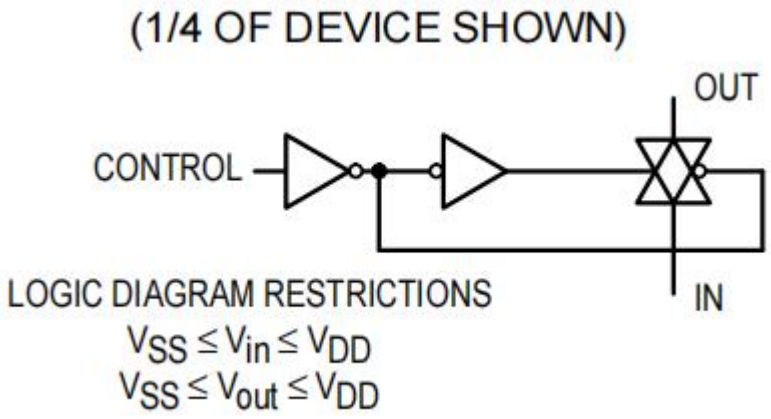
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection.Antistatic Precautions Must Be Taken.

3. MAXMUM RATINGS(Voltages Referenced to Vss)

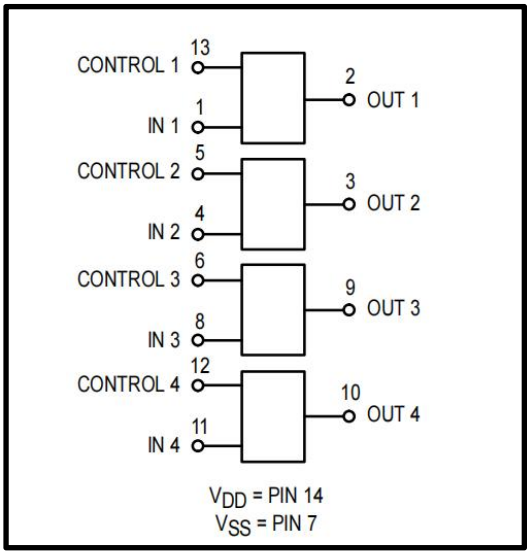
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}.V_{out}	Input or Output Voltage(DC or Transient)	-0.5 to VDD+0.5	V
I_{in}	Input Current(DC or Transient), per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation,per Packaget	500	mW
Tstg	Storage Temperature	-65 to + 150	℃
TL	Lead Temperature (8-Second Soldering)	260	℃

Note:Maximum Ratings are those values beyond which damage to the device may occur.

4. LOGIC DIAGRAM



5. BLOCK DIAGRAM



Control	Switch
0 = VSS	Off
1 = VDD	On

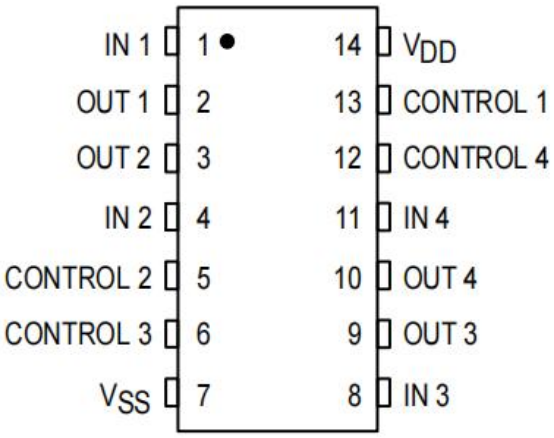
6. ELECTRICAL CHARACTERISTICS(Voltages Referenced to Vss)

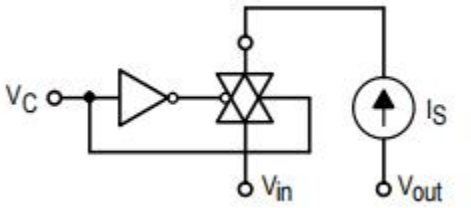
Characteristic	Figure	Symbol	V_{DD} Vdc	25℃			Unit
				Min	Typ	Max	
Input Voltage	1	V_{IL}	5.0	—	1.5	0.9	Vdc
Control Input			10	—	1.5	0.9	
			15	—	1.5	0.9	
		V_{IH}	5.0	3.0	2.0	—	Vdc
			10	8.0	6.0	—	
			15	13	11	—	
Input Current Control	—	I_{in}	15	—	±0.00001	±0.1	µAdc
Input Capacitance	—	C_{in}					pF
Control			—	—	5.0	—	
Switch Input			—	—	5.0	—	
Switch Output			—	—	5.0	—	
Feed Through			—	—	0.2	—	
Quiescent Current	2.3	I_{DD}	5.0		0.0005	0.25	µAdc
(Per Package)			10		0.0010	0.5	
			15		0.0015	1.0	
"ON"Resistance	4.5.6	R_{ON}		—			Ohms
(Vc= V_{DD},R_L=10 kΩ)				—			
(Vin=+5.0 Vdc)				—	300	660	
(Vin=-5.0 Vdc) Vss =-5.0 Vdc				—	300	660	
(Vin=±0.25 Vdc)			5.0	—	280	660	
(Vin=+7.5 Vdc)				—	240	400	
(Vin=-7.5 Vdc) Vss =- 7.5 Vdc				—	240	400	
(Vin=±0.25 Vdc)			7.5	—	180	400	
(Vin=+ 10 Vdc)				—	260	660	
(Vin=+ 0.25 Vdc) Vss = 0 Vdc				—	310	660	
(Vin=+5.6 Vdc)			10	—	310	660	
(Vin=+ 15 Vdc)				—	260	400	
(Vin=+0.25 Vdc) Vss = 0 Vdc				—	260	400	
(Vin=+9.3 Vdc)			15	—	300	400	
△"ON" Resistance	—	△R_{ON}					Ohms
Between any 2 circuits in a common package (V_C=V_{DD})							
(Vin=±5.0 Vdc,V_{SS}=-5.0 Vdc)			5.0	—	15	—	
(Vin=±7.5Vdc,V_{SS}=-7.5 Vdc)			7.5	—	10	—	
Input/Output Leakage Current	—	—					µAdc
(Vc=Vss)							
(Vin= + 7.5,Vout=- 7.5 Vdc)			7.5	—	±0.0015	±0.1	
(Vin=-7.5,Vout=+ 7.5 Vdc)			7.5	—	±0.0015	±0.1	

ELECTRICAL CHARACTERISTICS(CL= 50 pF,TA=25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Time (Vss =0 Vdc) Vin to Vout (Vc=VDD,RL= 10 kΩ)	7	tPLH, tPHL	5.0 10 15	— — —	15 7.0 6.0	45 15 12	ns
Control to Output (Vin≤ 10 Vdc,RL= 10 kΩ)	8	tPHZ, tPLZ, tPZH, tPZL	 5.0 10 15	 — — —	 34 20 15	 90 45 35	ns
Crosstalk, Control to Output (Vss =0Vdc) (Vc=V_{DD},Rin = 10 kΩ,R_{out} = 10 kΩ,f=1.0 kHz)	9	—	5.0 10 15		30 50 100		mV
Crosstalk between any two switches (Vss = 0Vdc) (RL= 1.0 kΩ,f = 1.0 MHz, crosstalk=20log$_{10}\frac{Vout1}{Vout2}$)	—	—	5.0		-80		dB
Noise Voltage (Vss =0 Vdc) (Vc=V_{DD},f=100 Hz) (Vc=V_{DD},f= 100 kHz)	10.11	—	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15		nv $\sqrt{\text{Cycle}}$
Second Harmonic Distortion (Vss=-5.0 Vdc) (V_{in}=1.77 Vdc, RMS Centered @0.0 Vdc, R_L= 10 kΩ,f= 1.0 kHz)	—	—			0.1 6		%
Insertion Loss (Vc =V_{DD}.Vin=1.77 Vdc, Vss=-5.0Vdc,RMS centered =0.0 Vdc,f=1.0 MHz) I_{loss} =20log$_{10}\frac{Vout}{Vin}$ (RL= 1.0 kΩ) (RL= 10 kΩ) (RL=100 kΩ) (RL=1.0 MΩ2)	12	—	5.0	 — — — —	 2.3 0.2 0.1 0.0 5	 — — — —	dB
Bandwidth (-3.0 dB) (Vc=VDD,Vin=1.77 Vdc,Vss=-5.0 Vdc, RMS centered @0.0 Vdc) (RL= 1.0 kΩ) (RL= 10 kΩ) (RL=100 kΩ) (RL= 1.0 MΩ)	12.13	BW	5.0	 — — — —	 54 40 38 37	 — — — —	MHZ
OFF Channel Feedthrough Attenuation (Vss=-5.0 Vdc) Vc=Vss,20 log$_{10}\frac{Vout}{Vin}$=-50db) Vout=-50dB) (RL=1.0kΩ) (RL= 10 kΩ) (RL=100 kΩ2) (RL=1.0MΩ)	—	—	5.0	 — — — —	 125 0 140 18 2.0	 — — — —	kHZ

7. PIN ASSIGNMENT





V_{IL}: V_C is raised from VSS until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10$ µA with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.
V_{IH}: When $V_C = V_{IH}$ to V_{DD}, the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

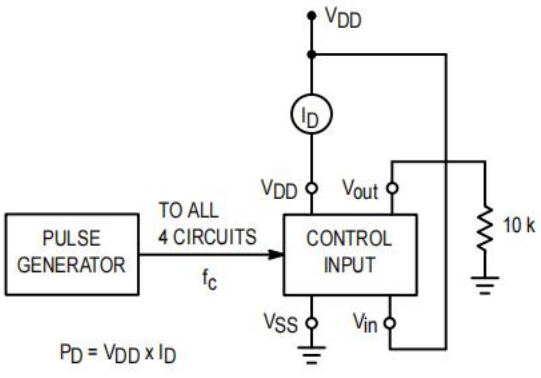


Figure 2. Quiescent Power Dissipation Test Circuit

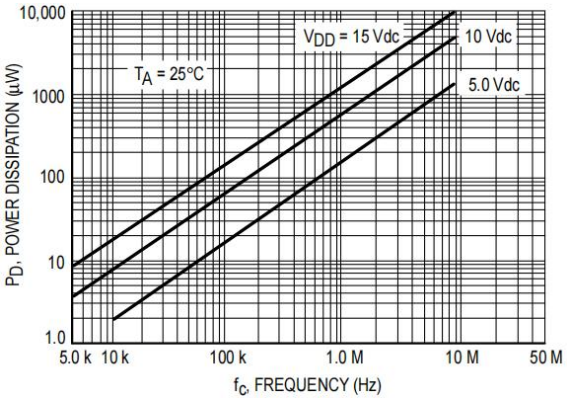


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

8. TYPICAL RON VERSUS INPUT VOLTAGE

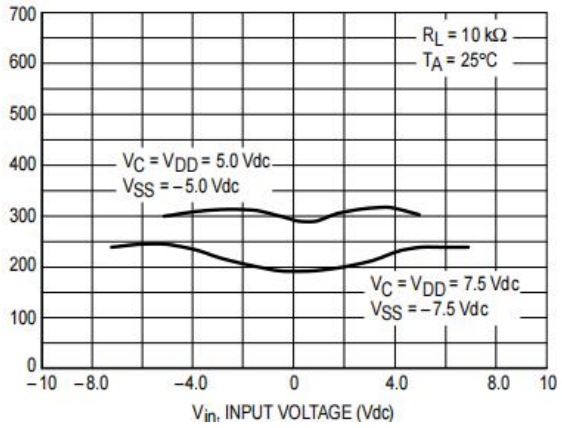


Figure 4. VSS = – 5.0 V and – 7.5 V

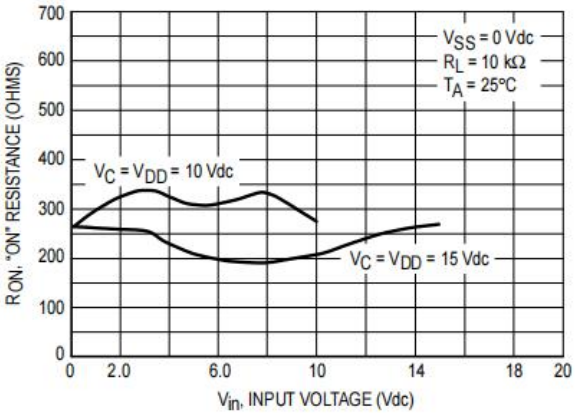


Figure 5. VSS = 0 V

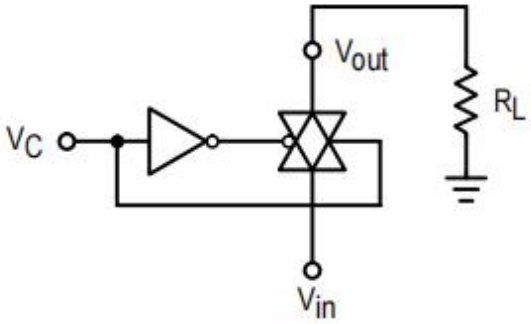


Figure 6. RON Characteristics Test Circuit

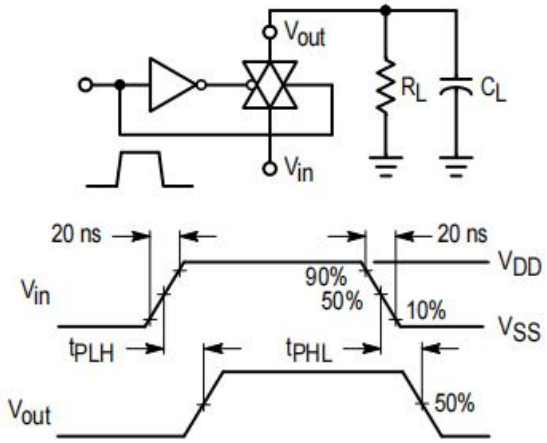


Figure 7. Propagation Delay Test Circuit and Waveforms

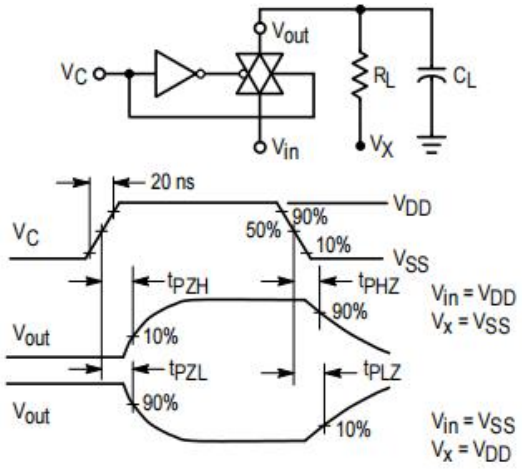


Figure 8. Turn–On Delay Time Test Circuit and Waveforms

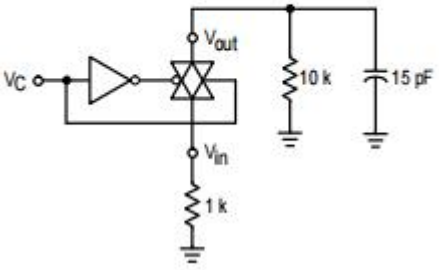


Figure 9. Crosstalk Test Circuit

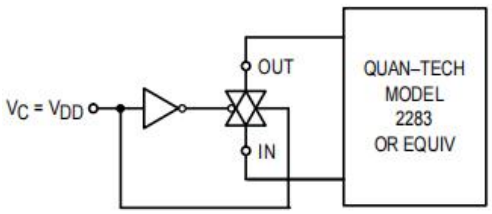


Figure 10. Noise Voltage Test Circuit

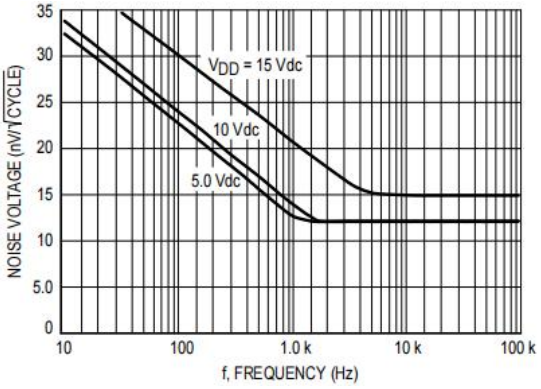


Figure 11. Typical Noise Characteristics

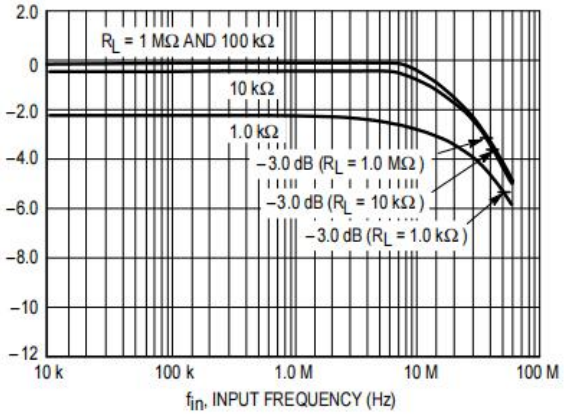


Figure 12. Typical Insertion Loss/Bandwidth Characteristics

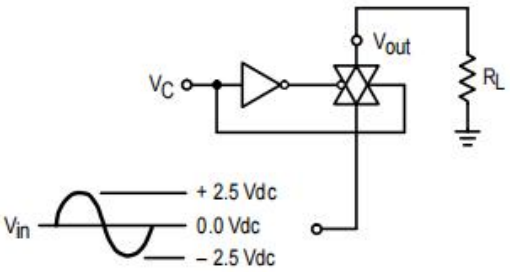


Figure 13. Frequency Response Test Circuit

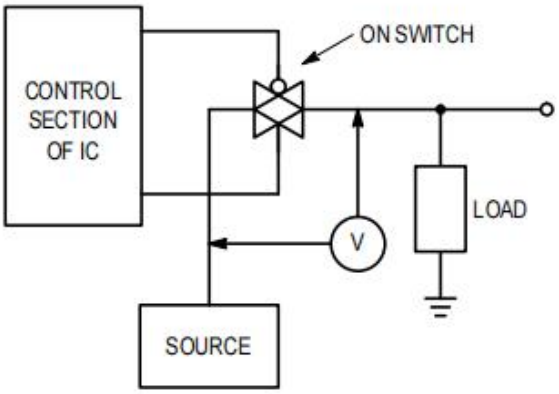


Figure 14. ΔV Across Switch

9. APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–to–5 V Digital Control signal is used to directly control a 5 Vp–p analog signal.

The digital control logic levels are determined by VDD and VSS. The VDD voltage is the logic high voltage; the VSS voltage is logic low. For the example, VDD = +5 V logic high at the control inputs; VSS = GND = 0 V logic low.

The maximum analog signal level is determined by VDD and VSS. The analog voltage must not swing higher than VDD or lower than VSS.

The example shows a 5 Vp–p signal which allows no margin at either peak. If voltage transients above VDD and/or below VSS are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between VDD and VSS is 18.0 V. Most parameters are specified up to 15 V which is the recommended maximum difference between VDD and VSS.

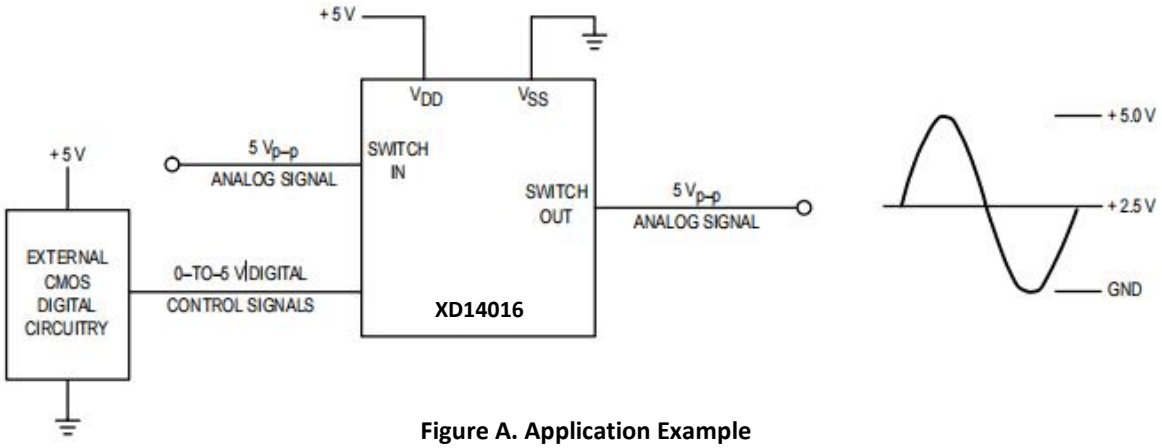


Figure A. Application Example

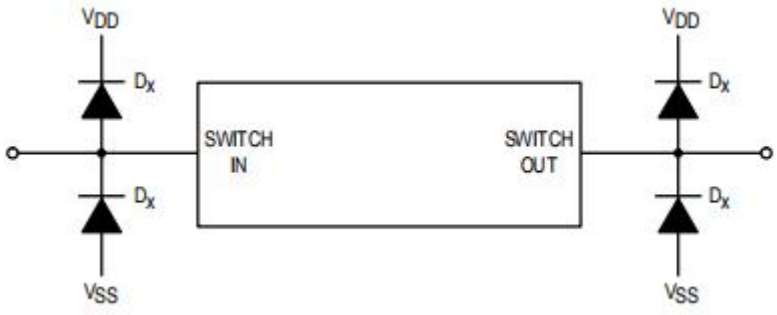


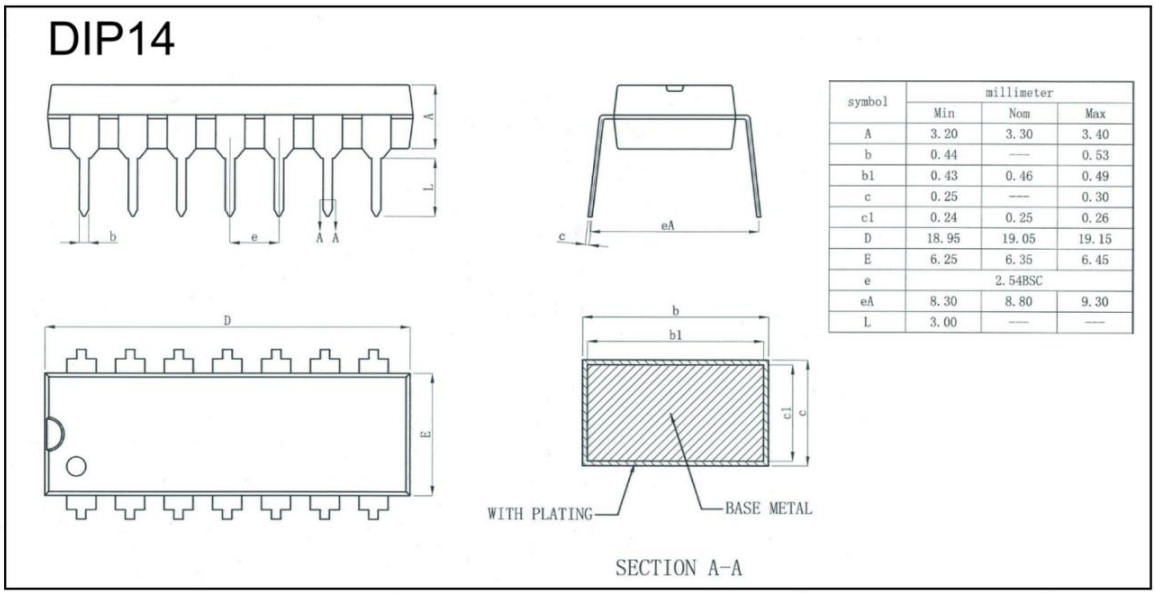
Figure B. External Germanium or Schottky Clipping Diodes

10. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD14016	XD14016	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

11. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	----	0.53
b1	0.43	0.46	0.49
c	0.25	----	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	----	----