High Common-Mode Voltage Difference Amplifier

Features

- ESD rating: 2.5 kV HBM
- Common-Mode Voltage Range: ±270 V
- Minimum CMRR: 90 dB
- DC Specifications:
  - Maximum Offset Voltage: 750 µV
  - Maximum Offset Voltage Drift: 15 µV/°C
  - Maximum Gain Error: 0.01%
  - Maximum Gain Error Drift: 3 ppm/°C
  - Maximum Gain Nonlinearity: 0.001% FSR
- AC Performance:
  - Bandwidth: 450 kHz
  - Typical Slew Rate: 1.8 V/µs
- Wide Supply Range: ±2.25 V to ±18 V
  - Maximum Quiescent Current: 1 mA
  - Rail-to-Rail Output
- Input Protection:
  - Common-Mode: ±500 V
  - Differential: ±500 V

Applications

- High-Voltage Current Sensing
- Battery Cell Voltage Monitoring
- Power-Supply Current Monitoring
- Motor Controls
- Replacement for Isolation Circuits

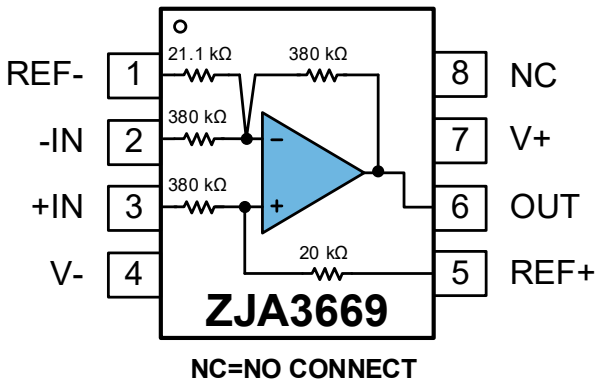
General Description

The ZJA3669 is a precision unity-gain difference amplifier with a very high input common-mode voltage range. It is a single, monolithic device that consists of a precision op amp and an integrated thin film resistor network. The ZJA3669 can accurately measure small differential voltages in the presence of common-mode signals up to ±270 V. The ZJA3669 inputs are protected from momentary common-mode or differential overloads of up to 500 V.

In many applications, where galvanic isolation in not required, the ZJA3669 can replace isolation amplifiers. This ability can eliminate costly isolated input side power supplies and the associated ripple, noise, and quiescent current. The excellent 0.0005% nonlinearity and 450 kHz bandwidth of the ZJA3669 are superior to those of conventional isolation amplifiers.

The ZJA3669 performance is specified over a wide temperature range of -40 °C to +125 °C. Its supply voltage is from ±2.25 V to ±18 V. The ZJA3669 is available in 8-lead SOIC package.

Functional Block Diagram



NC=NO CONNECT

Typical Performance Characteristics

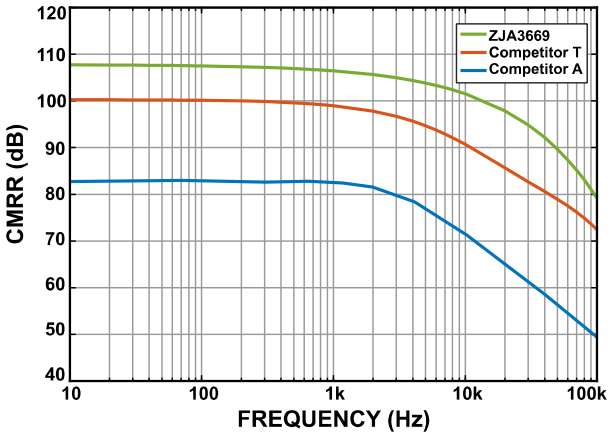


Table of Contents

Version (Release C) [1]

Revision History

Mar. 2025 — Release C

Updated Outline Dimensions and Related Parts

Dec. 2024 — Release B

Added Error Budget Analysis Example 2

Nov. 2024

Updated Typical Performance Characteristics, Specifications and Ordering Guide

Oct. 2024 — Release A

Jan. 2024 — Initial

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Pin Configurations and Function Descriptions

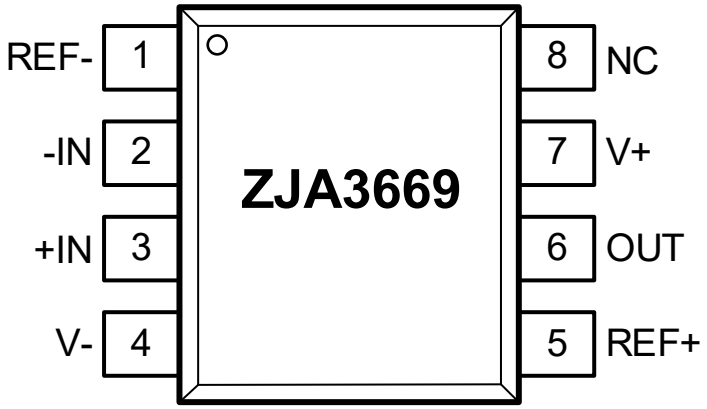


Figure 1. ZJA3669 Pin Configuration (8-lead SOIC)

Mnemonic	Pin No.	I/O [1]	Description
REF-	1	AI	Reference input
-IN	2	AI	Inverting input
+IN	3	AI	Non-inverting input
V- [2]	4	P	Negative power supply
REF+	5	AI	Reference input
OUT	6	AO	Output
V+	7	P	Positive power supply
NC	8	- -	No internal connection

[1] AI: Analog Input; P: Power; AO: Analog Output.
[2] In this document, (V+) - (V-) is referred to as V_S.

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Input Voltage	±300 V
Common-mode and Differential, 10s	±500 V
Maximum Voltage on REF+ and REF-	(V-) - 0.3 to (V+) + 0.3 V
Input Current on Any Input Pin	10 mA
Output Short-Circuit Duration [2]	Indefinite
Storage Temperature Range	-65 °C to 150 °C
Maximum Reflow Temperature [3]	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) [4]	
Human Body Model (HBM) [5]	2.5 kV
Charged Device Model (CDM) [6]	2 kV

Thermal Resistance [7]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	158	43	°C/W

[1] These ratings apply at 25°C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Limited by Over Temperature Protection (OTP).

[3] IPC/JEDEC J-STD-020 Compliant

[4] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[5] ANSI/ESDA/JEDEC JS-001 Compliant

[6] ANSI/ESDA/JEDEC JS-002 Complaint

[7] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at V_S = ±15 V, T_A = 25 °C, R_L = 2 kΩ connected to ground and V_{CM} = REF- =REF+ = GND, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
GAIN							
Initial	G	V_{OUT} = ±10 V			1		V/V
Gain Error	GE	V_{OUT} = ±10 V			0.002	0.01	%FSR
Gain vs Temperature	ΔG/ΔT	V_{OUT} = ±10 V	●		1	3	ppm/°C
Nonlinearity	GN	V_{OUT} = -10 V to +10 V			0.0005	0.001	%FSR
OFFSET VOLTAGE							
Initial Offset Voltage	V_{OS}				200	750	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		●		3	15	µV/°C
vs Supply	PSRR	V_S = ±2.25 V to ±18 V		90	120		dB
INPUT CHARACTERISTICS							
Impedance	R_{IN}	Differential			800		kΩ
		Common-mode			200		kΩ
Voltage Range	IVR	Differential		-14.7		14.7	V
		Common-mode		-270		270	V
Common-mode Rejection Ratio	CMRR	At dc, V_{CM} = ±250 V		90	100		dB
			●	84			dB
		At ac, 500 Hz, V_{CM} = 500 V_{P-P}		90			dB
		At ac, 1 kHz, V_{CM} = 500 V_{P-P}			90		dB
OUTPUT CHARACTERISTICS							
Voltage Range				-14.7		14.7	V
			●	-14.5		-14.5	V
Short-Circuit Current	I_{SC}	Source			50		mA
		Sink			90		mA
Capacitive Load Drive		No sustained oscillations			10		nF
OUTPUT NOISE VOLTAGE							
0.01 Hz to 10 Hz					20		μV_{P-P}
1 kHz					550		$nV/\sqrt{Hz}$
DYNAMIC PERFORMANCE							
Small-signal Bandwidth	BW				450		kHz
Slew Rate	SR	V_{OUT} = ±10 V step			1.8		V/µs
Full-power Bandwidth		V_{OUT} = 20 V_{P-P}			28		kHz
Settling Time	t_S	0.01%, V_{OUT} = 10 V step			18		µs
POWER SUPPLY							
Voltage Range				±2.25		±18	V
Quiescent Current	I_{SY}	V_S = ±18 V, V_{OUT} = 0 V			0.9	1	mA
			●			1.2	mA
TEMPERATURE RANGE							
Specified Temperature Range				-40		125	°C

Typical Performance Characteristics

Unless otherwise stated, V_S = ±15 V, T_A = 25 °C, R_L = 2 kΩ.

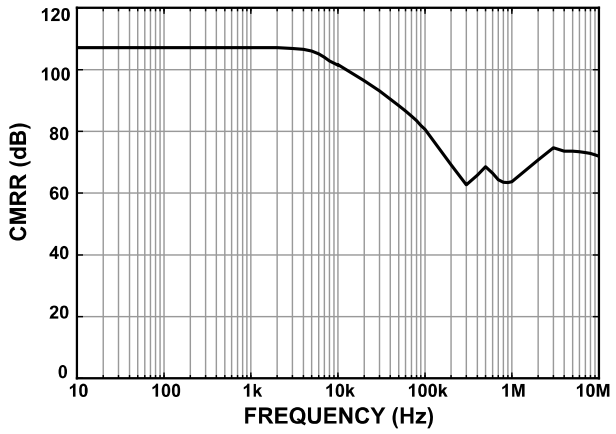


Figure 2. CMRR vs Frequency

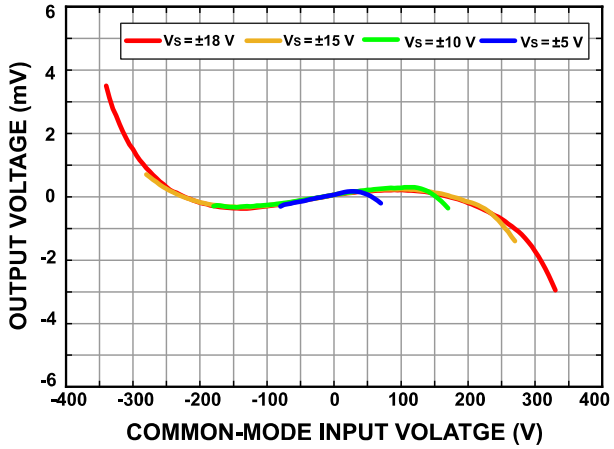


Figure 3. Common-mode Rejection

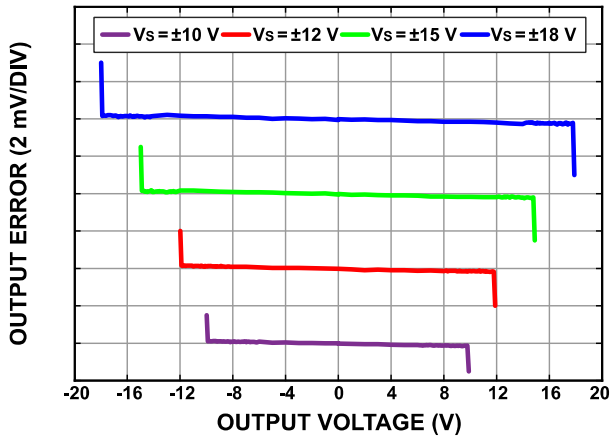


Figure 4. Output Error vs Output Voltage (R_L = 10 kΩ)

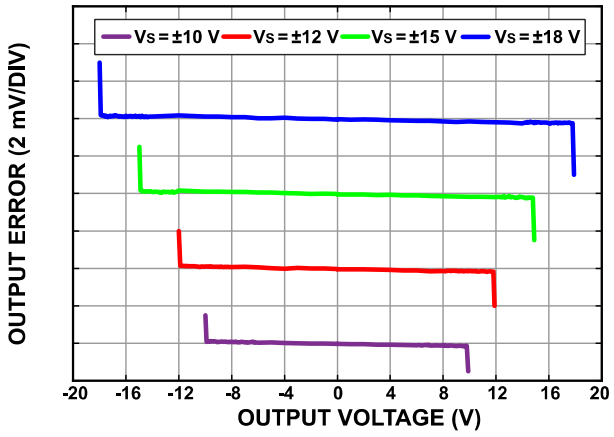


Figure 5. Output Error vs Output Voltage (R_L = 2 kΩ)

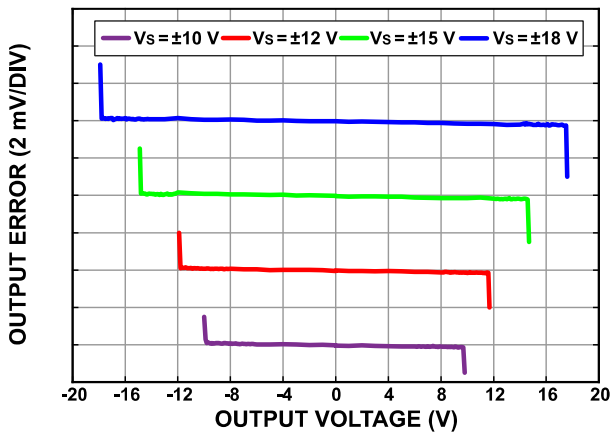


Figure 6. Output Error vs Output Voltage (R_L = 1 kΩ)

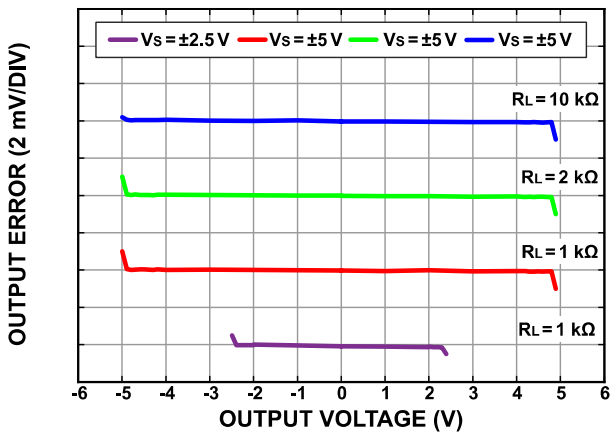


Figure 7. Output Error vs Output Voltage

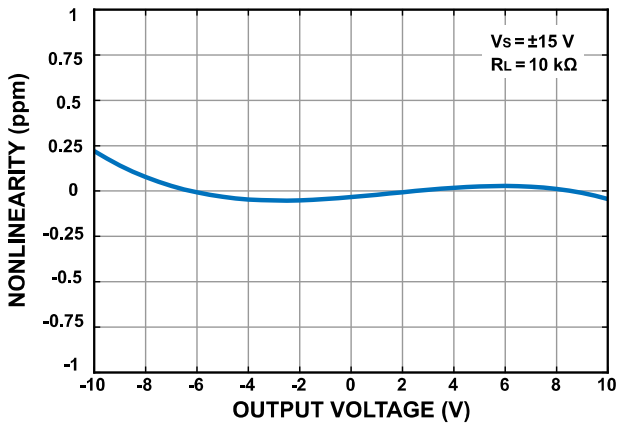


Figure 8. Gain Nonlinearity (R_L = 10 kΩ)

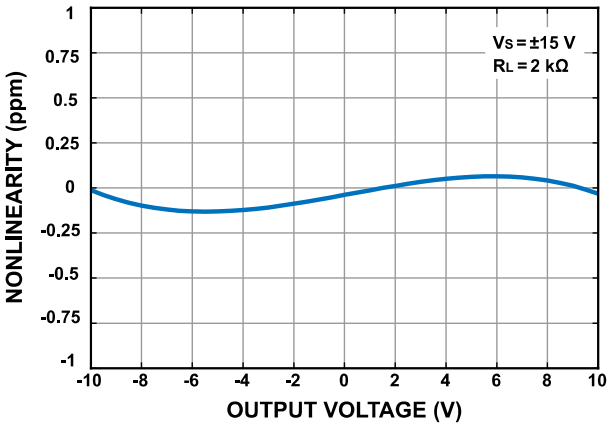


Figure 9. Gain Nonlinearity (R_L = 2 kΩ)

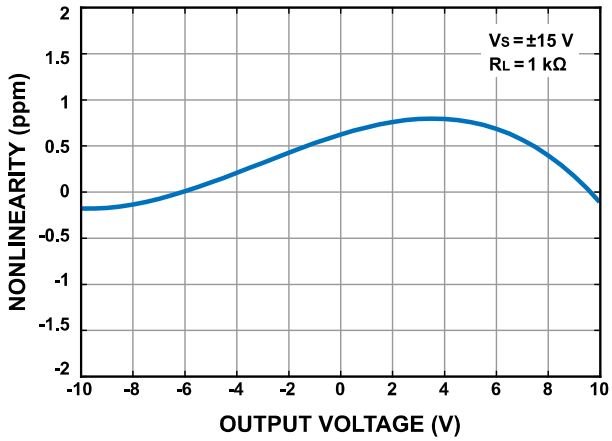


Figure 10. Gain Nonlinearity (R_L = 1 kΩ)

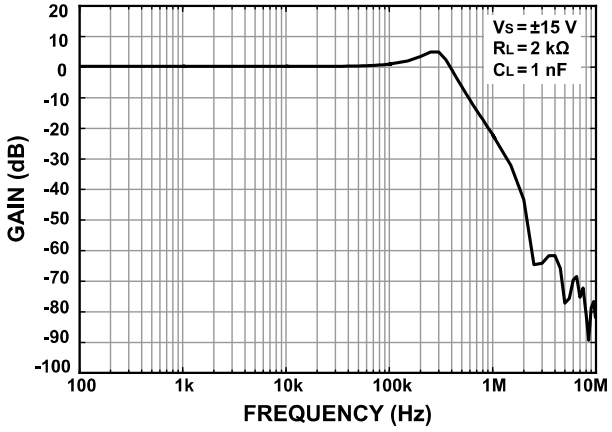


Figure 11. Gain vs Frequency

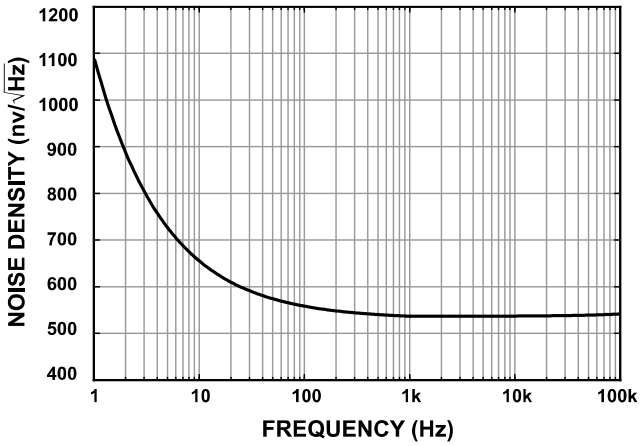


Figure 12. Noise Density vs Frequency

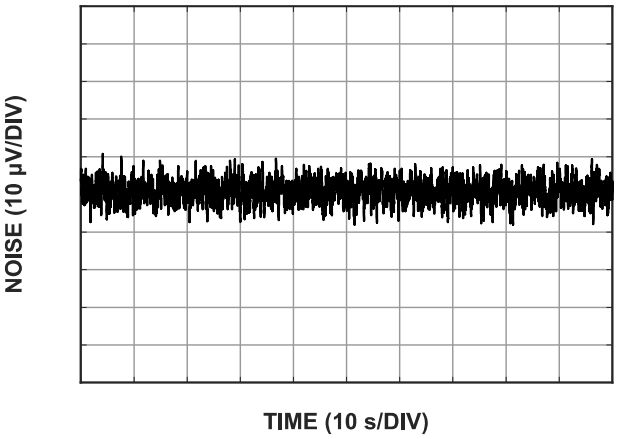


Figure 13. 0.01 Hz to 10 Hz Noise

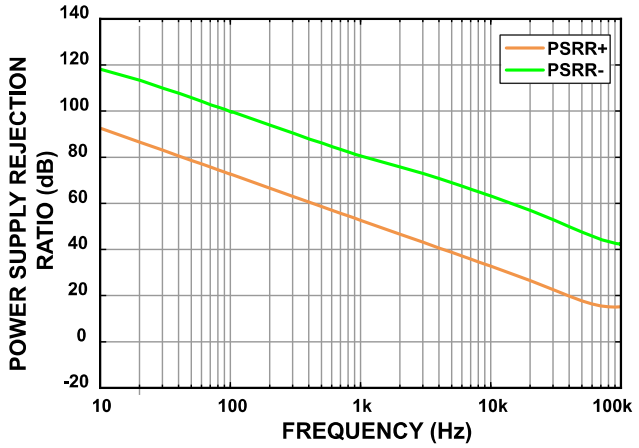


Figure 14. PSRR vs Frequency

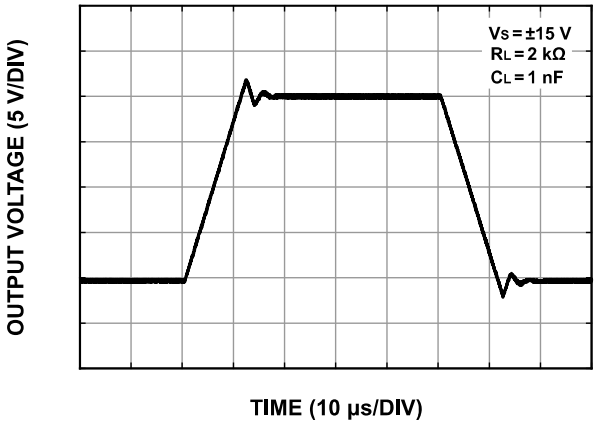


Figure 15. Large Signal Step Response

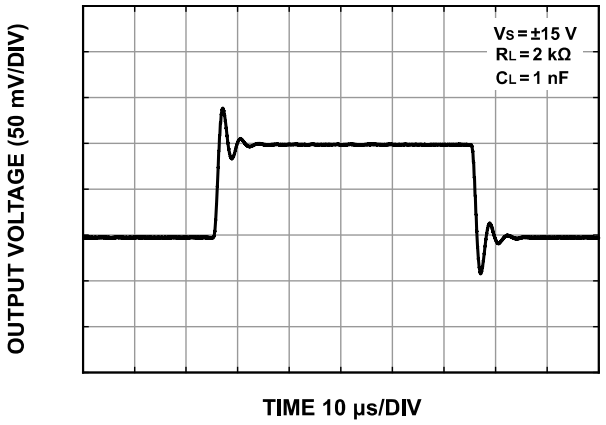


Figure 16. Small Signal Step Response

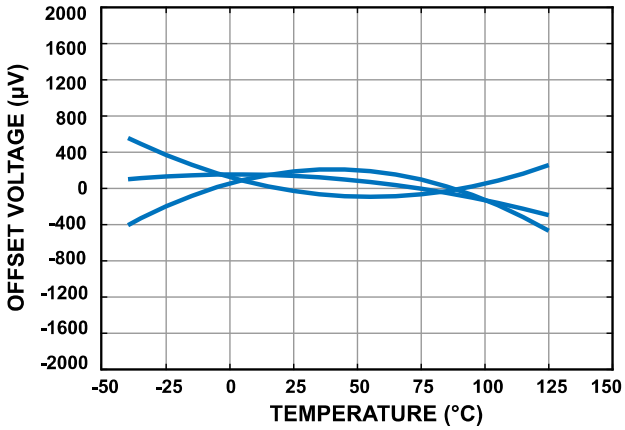


Figure 17. Offset Voltage vs Temperature

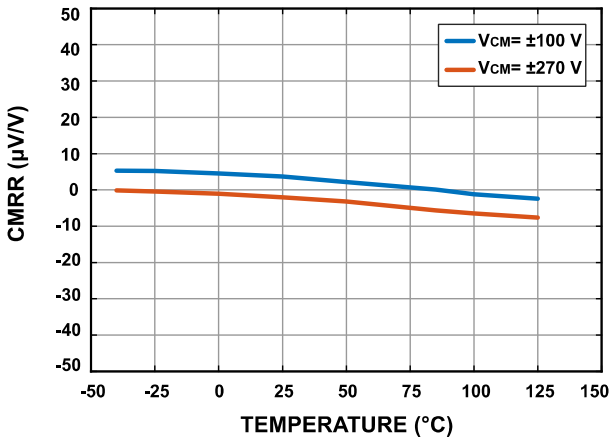


Figure 18. CMRR vs Temperature

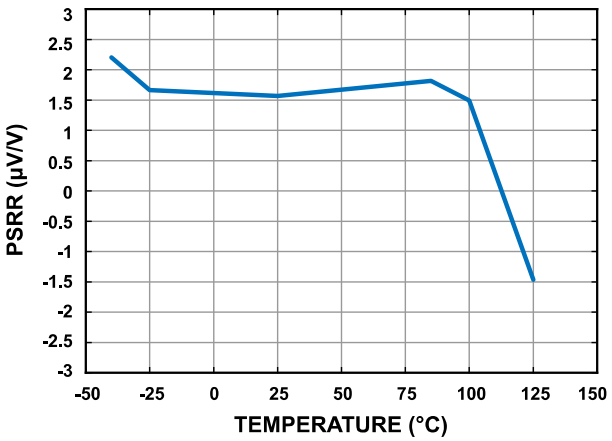


Figure 19. PSRR vs Temperature

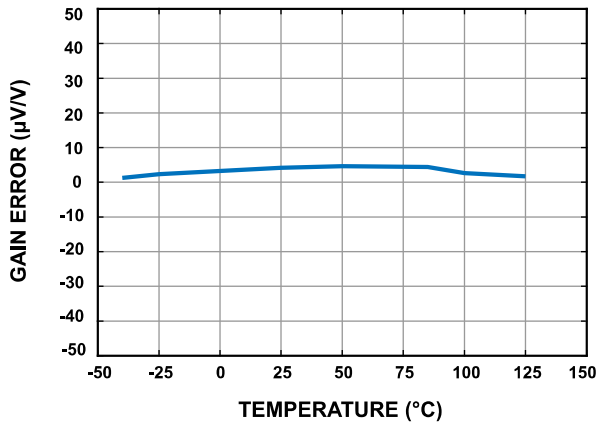


Figure 20. Gain Error vs Temperature

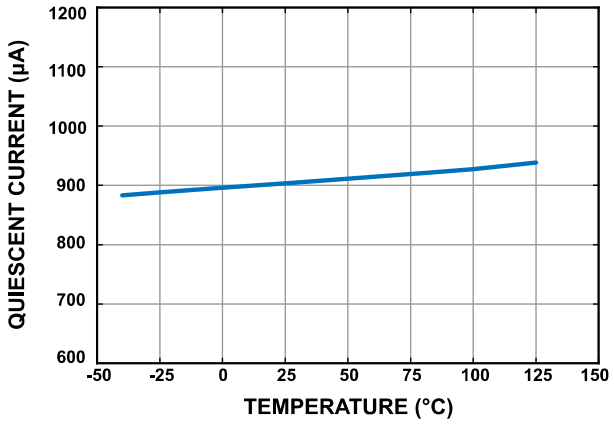


Figure 21. Quiescent Current vs Temperature

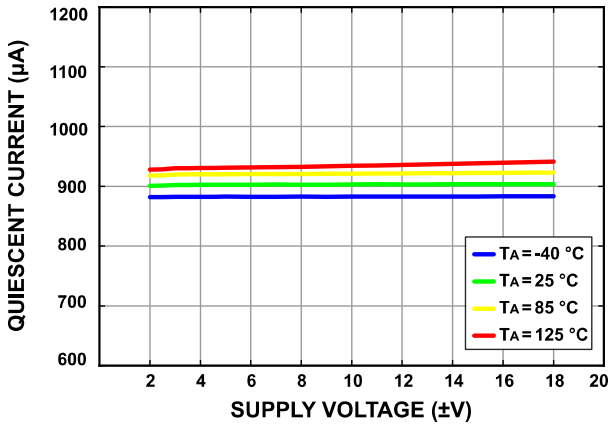


Figure 22. Quiescent Current vs Supply Voltage

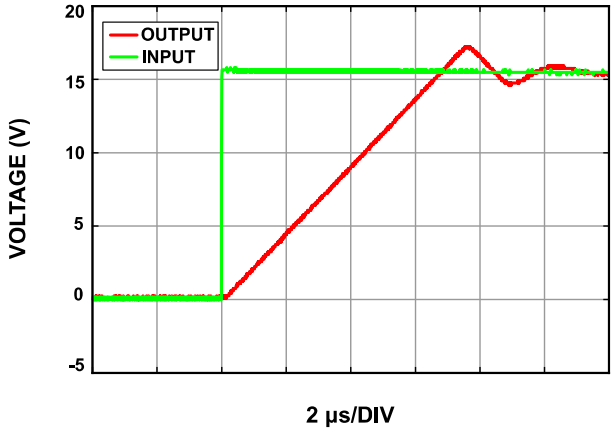


Figure 23. Positive Overload Recovery

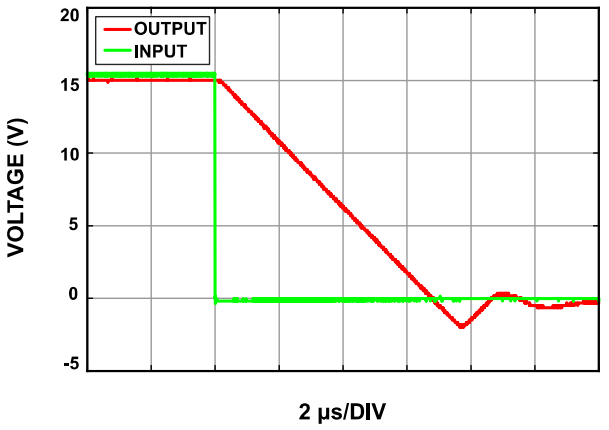


Figure 24. Negative Overload Recovery

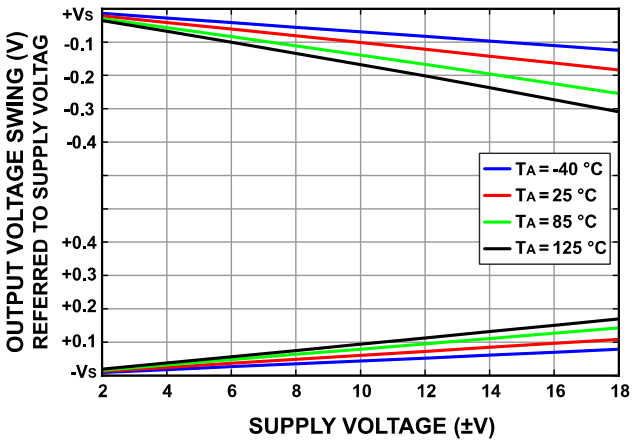


Figure 25. Output Voltage Swing vs. Supply Voltage (R_L=2 kΩ)

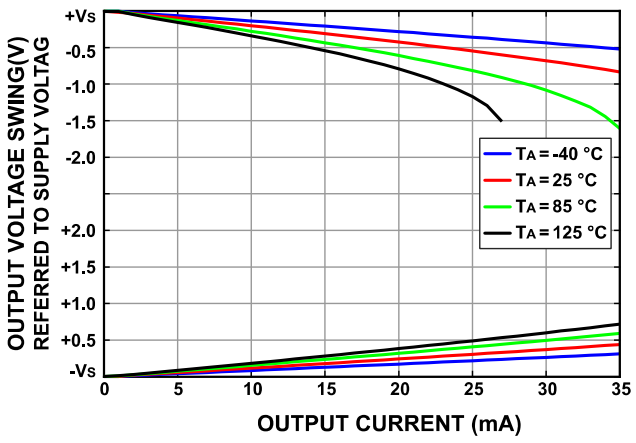


Figure 26. Output Voltage Swing vs. Output Current

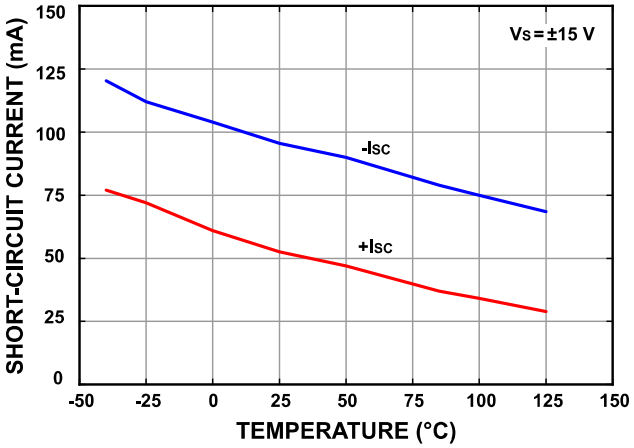


Figure 27. Short-Circuit Current vs. Temperature

Theory Of Operation

The ZJA3669 is a unity gain, differential-to-single-ended amplifier (difference amp) that can reject extremely high common-mode signals (in excess of 270 V with ±15 V supplies). It consists of an operational amplifier (op amp) and a resistor network.

To achieve high common-mode voltage range, an internal resistor divider (Pin 3 or Pin 5) attenuates the non-inverting signal by a factor of 20. Other internal resistors (Pin 1, Pin 2, and the feedback resistor) restore the gain to provide a differential gain of unity. The complete transfer function equals

$$V_{OUT} = V(+IN) - V(-IN)$$

Some applications, however, apply voltages to the reference terminals (REF+ and REF-). The complete transfer function is given:

$$V_{OUT} = V(+IN) - V(-IN) + 19 \times V(REF+) - 18 \times V(REF-)$$

ZJW's proprietary trimming ZHIJINGTRIM® provides resistor matching so that common-mode signals are rejected while differential input signals are amplified.

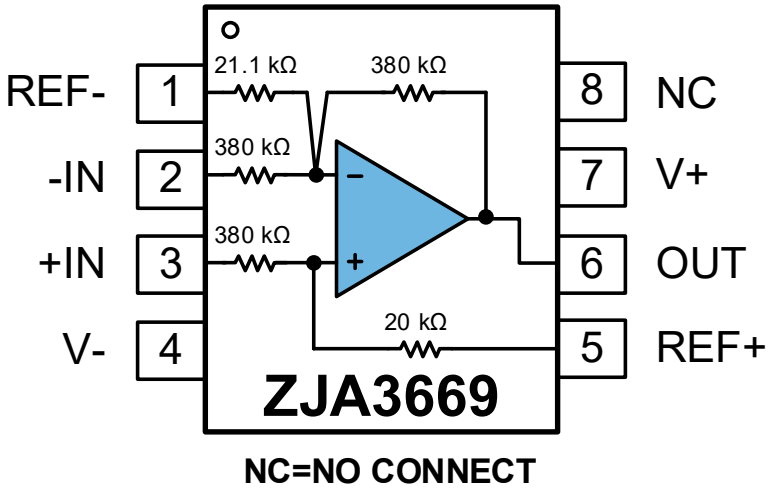


Figure 28. Functional Block Diagram

Applications Information

Basic Connections

Figure 29 shows the basic connections for operating the ZJA3669 with a dual supply. A supply voltage of between ±2.25 V and ±18 V is applied between Pin 7 and Pin 4. Both supplies should be decoupled close to the pins using 0.1 µF capacitors. Electrolytic capacitors of 10 µF, also located close to the supply pins, may be required if low frequency noise is present on the power supply. While multiple amplifiers can be decoupled by a single set of 10 µF capacitors, each amplifier should have its own set of 0.1 µF capacitors so that the decoupling point can be located right at the IC's power pins.

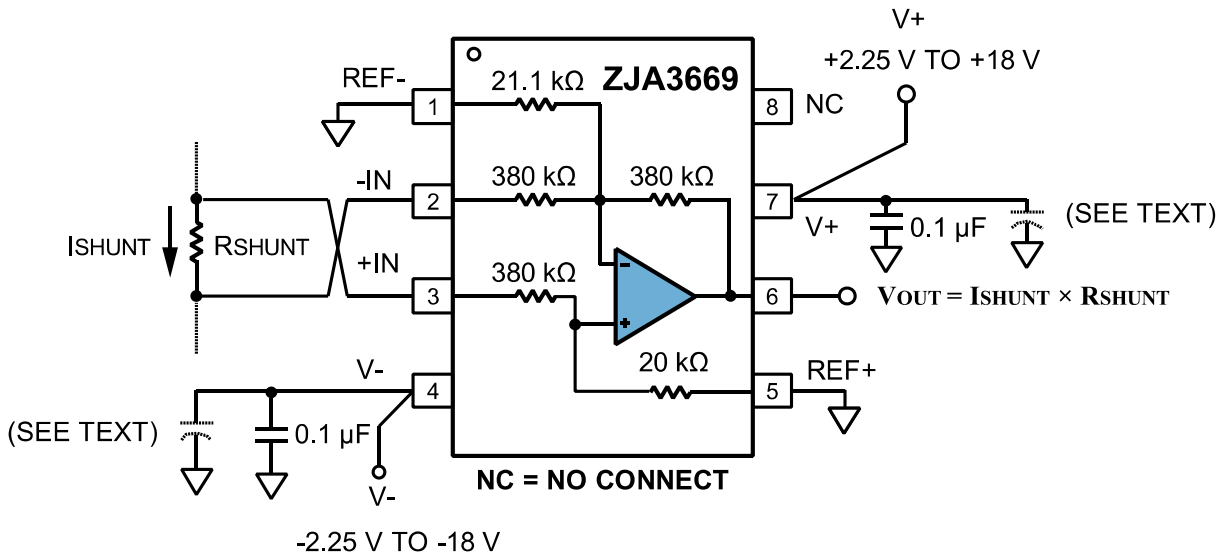


Figure 29. Basic Connections with a Dual Supply

The differential input signal, which typically results from a load current flowing through a small shunt resistor, is applied to Pin 2 and Pin 3 with the polarity shown to obtain a positive gain. The common-mode range on the differential input signal can range from -270 V to +270 V, and the maximum differential range is ±14.7 V. When configured as shown in Figure 29, the device operates as a simple gain of 1, differential-to-single-ended amplifier; the output voltage being the shunt resistance times the shunt current. The output is measured with respect to Pin 1 and Pin 5.

Pin 1 and Pin 5 (REF- and REF+) should be grounded for a gain of unity and should be connected to the same low impedance ground plane. Failure to do this results in degraded common-mode rejection. Pin 8 is a no connect pin and should be left open.

Single-Supply Operation

Figure 30 shows the connections for operating the ZJA3669 with a single supply. Because the output can swing to within about 0.3 V of either rail, it is necessary to apply an offset to the output. This can be conveniently done by connecting REF+ and REF- to a low impedance reference voltage (some ADCs provide this voltage as an output), which is capable of sinking current. Therefore, for a single supply of 10 V, V_{REF} may be set to 5 V for a bipolar input signal. This allows the output to swing ±4.7 V around the central 5 V reference voltage. Alternatively, for unipolar input signals, V_{REF} can be set to about 0.3 V, allowing the output to swing from 0.3 V (for a 0 V input) to within 0.3 V of the positive rail. The rail-to-rail output feature not only makes ZJA3669 makes full use of the circuit's dynamic range, but also easy to use.

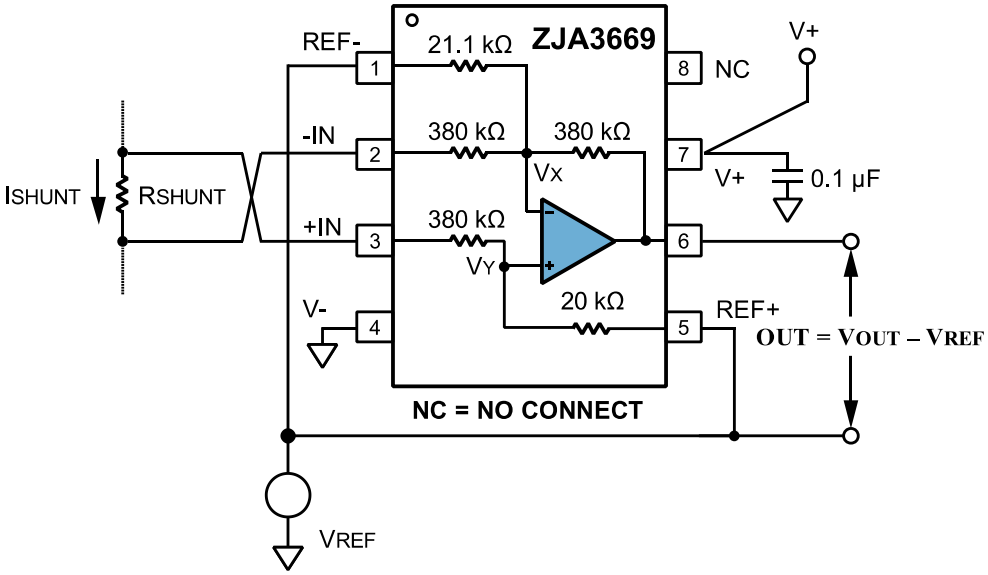


Figure 30. Operation with a Single Supply

Applying a reference voltage to REF+ and REF- and operating on a single supply reduces the input common-mode range of the ZJA3669. The new input common-mode range depends upon the voltage at the inverting and noninverting inputs of the internal operational amplifier, labeled V_X and V_Y in Figure 30. These nodes can swing to within 1 V of either rail.

Therefore, for a (single) supply voltage of 10 V, V_X and V_Y can range between 1.5 V and 8.5 V. If V_{REF} is set to 5 V, the permissible common-mode range is +75 V to -65 V by using the equations below of $V_{CM,\,min}$ and $V_{CM,\,max}$. The common-mode voltage ranges can be calculated by

$$V_X = V_Y = \frac{V_{+IN} + 19 \times V_{REF+}}{20}$$

$$V_{CM,min} = 20 \times V_{Y,min} - 19 \times V_{REF}$$

$$V_{CM,max} = 20 \times V_{Y,max} + 19 \times V_{REF}$$

System-Level Decoupling and Grounding

The use of ground planes is recommended to minimize the impedance of ground returns (and therefore the size of dc errors). Figure 31 shows how to work with grounding in a mixed-signal environment, that is, with digital and analog signals present. To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground returns. All ground pins from mixed-signal components, such as ADCs, should return through a low impedance analog ground plane. Digital ground lines of mixed-signal converters should also be connected to the analog ground plane. Typically, analog and digital grounds should be separated; however, it is also a requirement to minimize the voltage difference between digital and analog grounds on a converter, to keep them as small as possible (typically within 0.3 V). The increased noise, caused by the converter's digital return currents flowing through the analog ground plane, is typically negligible. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. Note that Figure 31 suggests a "star" ground system for the analog circuitry, with all ground lines being connected, in this case, to the ADC's analog ground.

However, when ground planes are used, it is sufficient to connect ground pins to the nearest point on the low impedance ground plane.

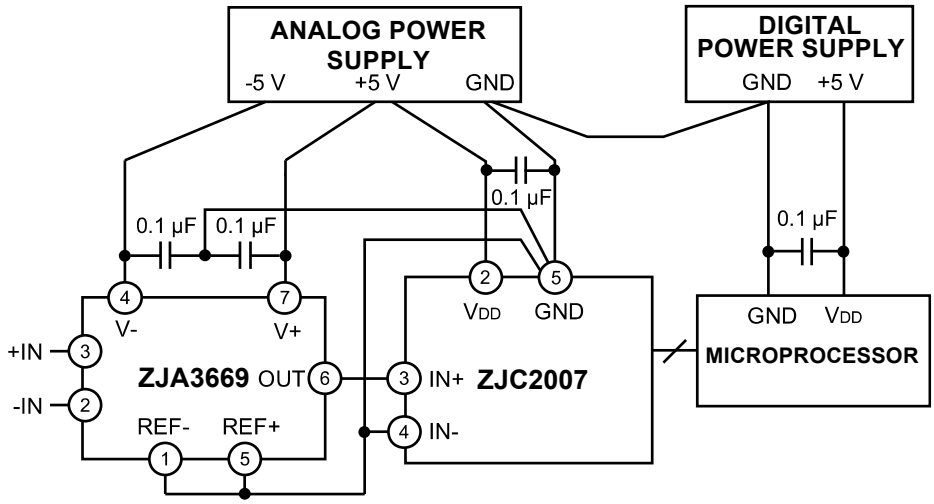


Figure 31. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

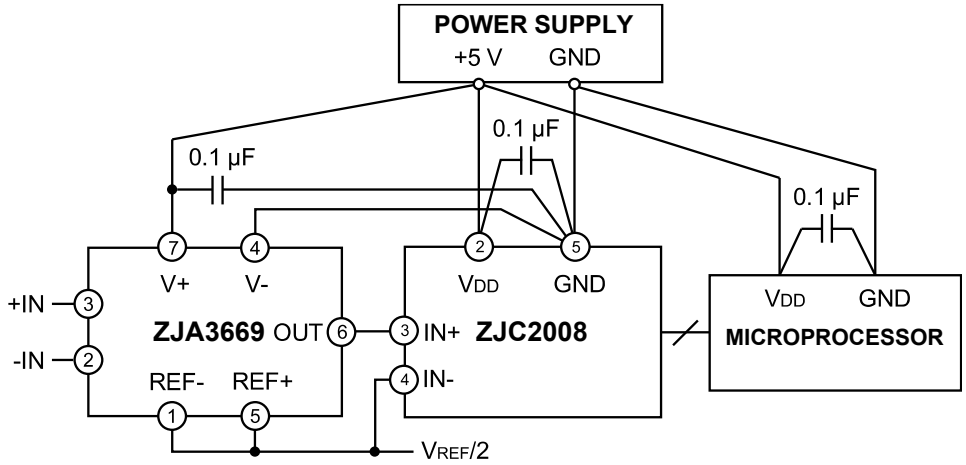


Figure 32. Optimal Ground Practice in a Single-Supply Environment

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 32 shows how to minimize interference between the digital and analog circuitry.

In this example, a separate voltage of V_{REF} / 2 is used to drive ADC's pin IN-, ZJA3669's pin REF+ and pin REF-. The external reference must be capable of sourcing and sinking a current equal to V_{CM} / 200 kΩ. As in the previous case, separate analog and digital ground planes should be used (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes should connect at the power supply's ground pin. Separate traces (or power planes) should run from the power supply to the supply pins of the digital and analog circuits. Ideally, each device should have its own power supply trace, but these can be shared by a number of devices, as long as a single trace is not used to route current to both digital and analog circuitry.

Using a Large Sense Resistor

Insertion of a large value shunt resistance across the input pins, pin 2 and pin 3, will imbalance the input resistor network, introducing a common-mode error. The magnitude of the error will depend on the common-mode voltage and the magnitude of R_{SHUNT}.

Table 1 shows some sample error voltages generated by a common-mode voltage of 200 V DC with shunt resistors from 20 Ω to 2000 Ω. Assuming that the shunt resistor is selected to use the full ±10 V output swing of the ZJA3669, the error voltage becomes quite significant as R_{SHUNT} increases.

R_S (Ω)	Error V_{OUT} (V)	Error Indicated (mA)
20	0.01	0.5
1000	0.499	0.499
2000	0.995	0.498

Table 1. Error Resulting from Large Values of R_{SHUNT} (Uncompensated Circuit)

To measure low current or current near zero in a high common-mode environment, an external resistor equal to the shunt resistor value can be added to the low impedance side of the shunt resistor, as shown in Figure 33.

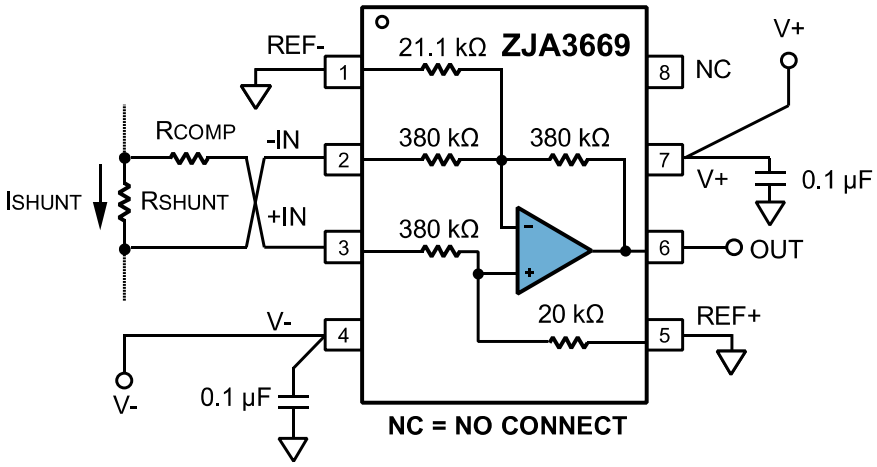


Figure 33. Compensating for Large Sense Resistors

The sense resistor imbalances the input resistor matching of the ZJA3669, thus degrading its CMR. Common-mode rejection (CMR) of the ZJA3669 depends on the input resistor network, which is trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedance driving the two inputs. A 75 Ω resistance in series with pins 2 or 3 decreases the common-mode rejection ratio (CMRR) from 100 dB (typical) to 74 dB. Resistance in series with the reference pins also degrades CMR. A 4 Ω resistance in series with pins 1 or 5 decreases CMRR from 100 dB to 74 dB.

Also, the input impedance of ZJA3669 loads R_{SHUNT}, causing gain error in the voltage-to-current conversion. Both errors can be corrected.

The CMR error can be corrected with the addition of a compensation resistor (R_{COMP}), equal to the value of R_{SHUNT}, as shown in Figure 33. If R_{SHUNT} is less than 5 Ω, degradation in the CMR is negligible and R_{COMP} can be omitted. If R_{SHUNT} is larger than approximately 250 Ω, trimming R_{COMP} may be required to achieve greater than 90 dB CMRR even if ZJA3669 CMRR is not taken into account. This error is caused by the ZJA3669 input impedance mismatch.

If R_{SHUNT} is more than approximately 75 Ω, the gain error is greater than the 0.02% specification of the ZJA3669. This gain error can be corrected by slightly increasing the value of R_{SHUNT}. The corrected value (R_{SHUNT}') can be calculated by

$$R'_{SHUNT} = R_{SHUNT} \times 380\ k\Omega / (380\ k\Omega - R_{SHUNT})$$

Example: For a 1 V/mA transfer function, the nominal, uncorrected value for R_{SHUNT} would be 1 kΩ. A slightly larger value (R_{SHUNT}' = 1002.6 Ω), compensates for the gain error as a result of loading.

Output Filtering

The wideband noise performance of the ZJA3669 is dominated by the internal resistor network. The thermal or Johnson noise of these resistors measures approximately 550 nV$\sqrt{Hz}$. The internal op amp contributes virtually no excess noise at frequencies above 100 Hz.

Many applications may be satisfied with less than the full 450 kHz bandwidth of the ZJA3669. In these cases, the noise can be reduced with a low-pass filter on the output. A simple 2-pole, low-pass Butterworth filter can be implemented using the ZJA3001-1 after the ZJA3669 to limit noise at the output, as shown in Figure 34. Table 2 gives recommended component values for various corner frequencies, along with the peak-to-peak output noise for each case.

$$C_1 = m*C_2$$

$$R_1 = n*R_2$$

$$f_c = \frac{1}{2\pi R_2 C_2 \sqrt{mn}}$$

$$Q = \frac{\sqrt{mn}}{n+1}$$

For 2-pole Butterworth filter, Q = 0.7071. Set m = 2.2 in order to be easier to find suitable capacitor values of C_1 and C_2. Use Q equation to get the n for resistors ratio and calculate R_2 by using cut-off frequency f_C and find the suitable values of R_1 and R_2 in the resistors with 1% tolerance.

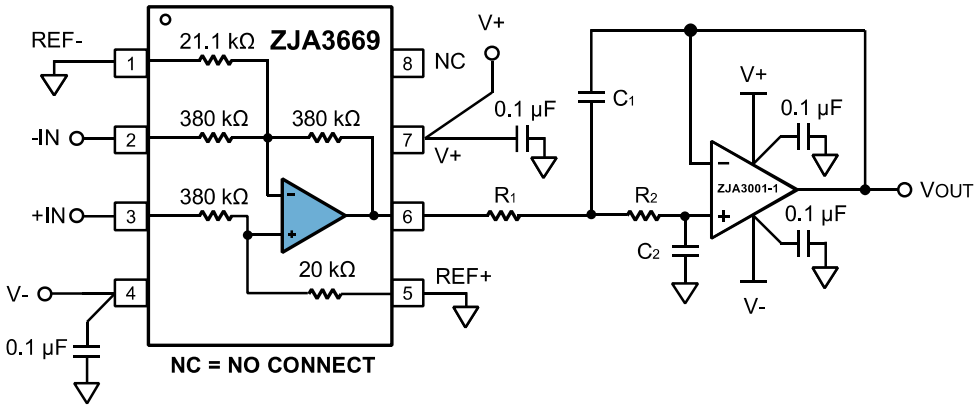


Figure 34. Filtering of Output Noise Using a 2-Pole Butterworth Filter

Corner Frequency	R_1	R_2	C_1	C_2	Output Noise (P-P)
No Filter					3.05 mV
50 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	2.2 nF ± 10%	1 nF ± 10%	1 mV
5 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	22 nF ± 10%	10 nF ± 10%	320 µV
500 Hz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	220 nF ± 10%	0.1 µF ± 10%	100 µV
50 Hz	2.7 kΩ ± 10%	1.5 kΩ ± 10%	2.2 µF ± 20%	1 µF ± 20%	32 µV

Table 2. Recommended Values for 2-Pole Butterworth Filter

A Gain of 19 Differential Amplifier

While low level signals can be connected directly to the -IN and +IN inputs of the ZJA3669, differential input signals can also be connected, as shown in Figure 35, to give a precise gain of 19. However, large common-mode voltages are no longer permissible.

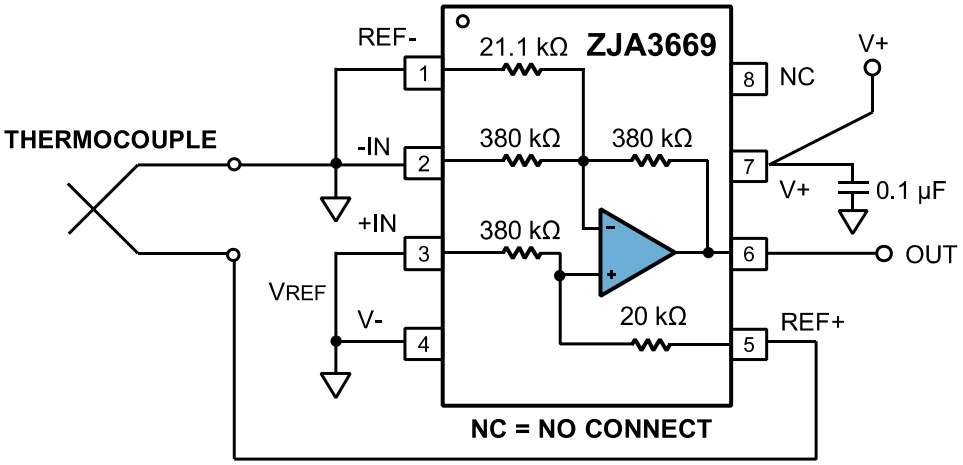


Figure 35. A Gain of 19 Thermocouple Amplifier

Error Budget Analysis Example 1

In the dc application that follows, the 10 A output current from a device with a high common-mode voltage (such as a power supply or current-mode amplifier) is sensed across a 1 Ω shunt resistor (see Figure 36). The common-mode voltage is 200 V, and the resistor terminals are connected through a long pair of lead wires located in a high noise environment, for example, 50 Hz/60 Hz, 440 V AC power lines.

The calculations in Table 3 assume an induced noise level of 1 V at 50 Hz on the leads, in addition to a full-scale dc differential voltage of 10 V. The error budget table quantifies the contribution of each error source. This example demonstrates that the dominate source of error, even over temperature, comes from the CMRR specification of the devices. The common-mode error is 38% of the total error for the competitor T device (“Comp T” in the table), while 49% of the total error for the competitor A’s higher-grade device (“Comp A” in the table). The ZJA3669 exhibits superior accuracy both at room temperature and across the tested temperature range.

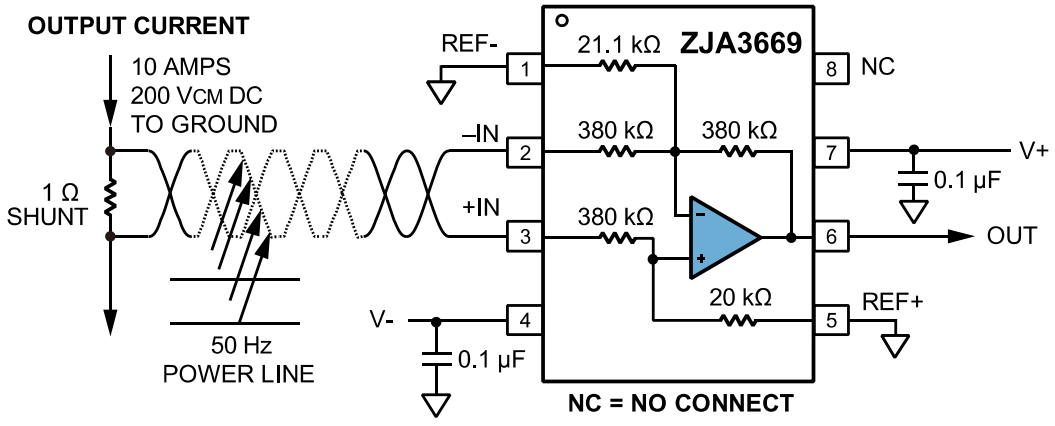


Figure 36. Error Budget Analysis Example 1: VIN = 10 V Full-Scale, V_{CM} = 200 V AC, R_{SHUNT} = 1 Ω, 1 V_{P-P}, 50 Hz Power-Line Interference

Error Source	ZJA3669	Comp T	Comp A	Error, ppm of FS		
				ZJA3669	Comp T	Comp A
ACCURACY, T_A = 25 °C						
Initial Gain Error	**0.01% FS max (0.0001×10)/10 V×10⁶**	**0.02% FS max (0.0002×10)/10 V×10⁶**	**0.03% FS max (0.0003×10)/10 V×10⁶**	100	200	300
Offset Voltage	**0.75 mV max (0.00075 V/10 V)×10⁶**	**1.1 mV max (0.0011 V/10 V)×10⁶**	**0.5 mV max (0.0005 V/10 V)×10⁶**	75	110	50
DC CMR	**90 dB min (31.6×10⁻⁶×200 V)/10 V×10⁶**	**90 dB min (31.6×10⁻⁶×200 V)/10 V×10⁶**	**86 dB min (50.1×10⁻⁶×200 V)/10 V×10⁶**	632	632	1002
			Total Accuracy Error	807	942	1352
TEMPERATURE DRIFT, T_A = 25 °C to 85 °C						
Gain	**3 ppm/°C×60 °C**	**10 ppm/°C×60 °C**	**10 ppm/°C×60 °C**	180	600	600
Offset Voltage	**(15 µV/°C×60 °C) ×10⁶/10 V**	**(15 µV/°C×60 °C) ×10⁶/10 V**	**(10 µV/°C×60 °C) ×10⁶/10 V**	90	90	60
			Total Drift Error	270	690	660
RESOLUTION						
Noise, Typical, 0.01 Hz to 10 Hz, μV_{P-P}	**20 µV/10 V×10⁶**	**20 µV/10 V×10⁶**	**15 µV/10 V×10⁶**	2	2	1.5
CMR, 50 Hz	**90 dB min (31.6×10⁻⁶×1 V)/10 V×10⁶**	**90 dB min (31.6×10⁻⁶×1 V)/10 V×10⁶**	**86 dB min (50.1×10⁻⁶×1 V)/10 V×10⁶**	3.2	3.2	5.0
Nonlinearity	**10 ppm max (10⁻⁵×10 V)/10 V×10⁶**	**10 ppm max (10⁻⁵×10 V)/10 V×10⁶**	**10 ppm max (10⁻⁵×10 V)/10 V×10⁶**	10	10	10
			Total Resolution Error	15.2	15.2	16.5
			Total Error	1092	1647	2029

Table 3. ZJA3669 vs. Competitors Error Budget Analysis Example (V_{CM} = 200 V DC)

Error Budget Analysis Example 2

This application is similar to the previous example except that the sensed load current is from an amplifier with an ac common-mode component of ±100 V (frequency = 500 Hz) present on the shunt (see Figure 37). All other conditions are the same as before. Note that the same kind of power-line interference can happen as detailed in Example 1. However, the ac common-mode component of 200 V_{P-P} coming from the shunt is much larger than the interference of 1 V_{P-P}; therefore, this interference component can be neglected. The ZJA3669's excellent CMRR across frequency and minimal gain drift over temperature make it suitable for precision applications operating under high-frequency interference across a wide temperature range, such as those found in industrial or automotive environments.

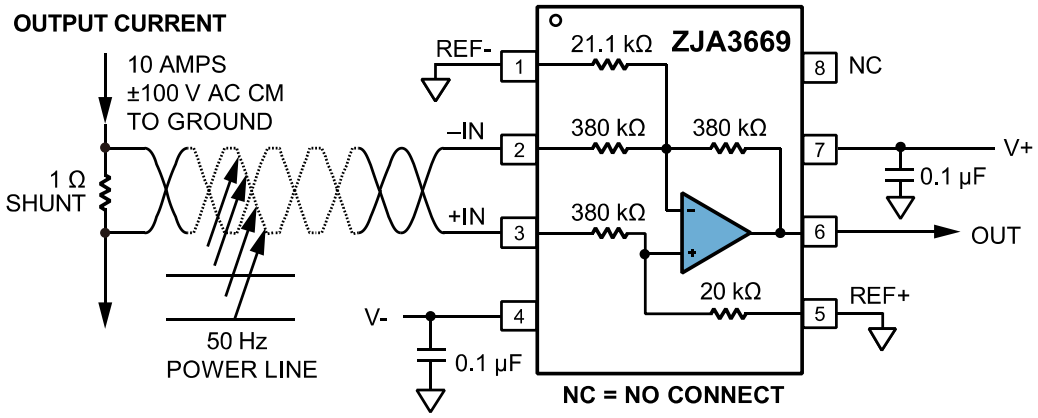


Figure 37. Error Budget Analysis Example 2: VIN = 10 V Full-Scale, V_{CM} = ±100 V at 500 Hz, R_{SHUNT} = 1 Ω

Error Source	ZJA3669	Comp T	Comp A	Error, ppm of FS		
				ZJA3669	Comp T	Comp A
ACCURACY, T_A = 25 °C						
Initial Gain Error	**0.01% FS max (0.0001×10)/10 V×10⁶**	**0.02% FS max (0.0002×10)/10 V×10⁶**	**0.03% FS max (0.0003×10)/10 V×10⁶**	100	200	300
Offset Voltage	**0.75 mV max (0.00075 V/10 V)×10⁶**	**1.1 mV max (0.0011 V/10 V)×10⁶**	**0.5 mV max (0.0005 V/10 V)×10⁶**	75	110	50
			Total Accuracy Error	175	310	350
TEMPERATURE DRIFT, T_A = 25 °C to 85 °C						
Gain	**3 ppm/°C×60 °C**	**10 ppm/°C×60 °C**	**10 ppm/°C×60 °C**	180	600	600
Offset Voltage	**(15 µV/°C×60 °C) ×10⁶/10 V**	**(15 µV/°C×60 °C) ×10⁶/10 V**	**(10 µV/°C×60 °C) ×10⁶/10 V**	90	90	60
			Total Drift Error	270	690	660
RESOLUTION						
Noise, Typical, 0.01 Hz to 10 Hz, μV_{P-P}	**20 µV/10 V×10⁶**	**20 µV/10 V×10⁶**	**15 µV/10 V×10⁶**	2	2	1.5
CMR, 50 Hz	**90 dB min (31.6×10⁻⁶×1 V)/10 V×10⁶**	**90 dB min (31.6×10⁻⁶×1 V)/10 V×10⁶**	**86 dB min (50.1×10⁻⁶×1 V)/10 V×10⁶**	3.2	3.2	5.0
Nonlinearity	**10 ppm max (10⁻⁵×10 V)/10 V×10⁶**	**10 ppm max (10⁻⁵×10 V)/10 V×10⁶**	**10 ppm max (10⁻⁵×10 V)/10 V×10⁶**	10	10	10
AC CMR @ 500 Hz	**90 dB min (31.6×10⁻⁶×200 V)/10 V×10⁶**	**90 dB min (31.6×10⁻⁶×200 V)/10 V×10⁶**	**86 dB min (50.1×10⁻⁶×200 V)/10 V×10⁶**	632	632	1002
			Total Resolution Error	647	647	1019
			Total Error	1092	1647	2029

Table 4. ZJA3669 vs. Competitors Error Budget Example 2 (V_{CM} = ±100 V @ 500 Hz)

Thermal Shutdown

Due to its high operating voltage (up to 40 V) and short-circuit current (up to 50/90 mA), the ZJA3669 can dissipate up to 2 W to 3 W of power during use. As thermal resistance for various package formats typically exceeds 100 °C/W, self-heating and the risk of permanent damage from high temperatures are concerns in real-world applications. To address this, ZJA3669 incorporates an automatic over-temperature protection (OTP) function. When the chip temperature reaches 150 °C, OTP triggers, putting the chip into shutdown mode. Both input and output terminals enter a high-impedance state, significantly reducing power consumption and facilitating temperature drop. Once the chip cools down to 130 °C, OTP disengages, and the chip resumes normal operation.

Battery Cell Voltage Monitor

The ZJA3669 can be used to measure the voltages of single cells in a stacked battery pack for its high common-mode voltage range and precision performances. Figure 38 shows an example for such an application.

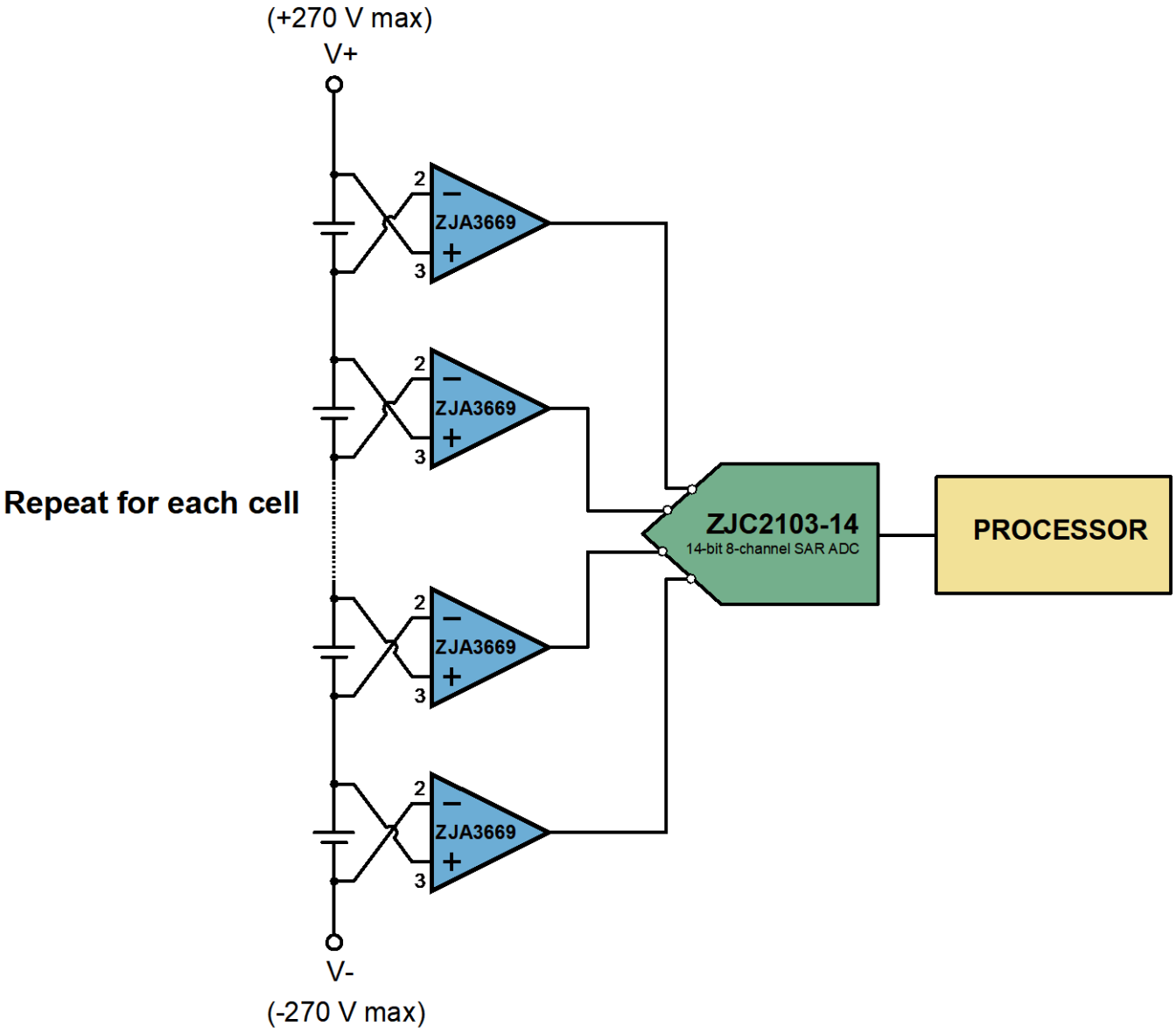


Figure 38. Battery Cells Voltage Monitor

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1 µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

As a result of the high common-mode input voltage rating of the ZJA3669, evaluation of the device often involves high-voltage operation. As a difference amplifier, it may also be used in current-sensing applications. In addition to voltage and current limitations, proper electrostatic discharge precautions are recommended.

High Voltage

The common-mode input voltage rating of the ZJA3669 is ±270 V. When using the device under such circumstances, all proper safety practices must be followed. Do not apply more than ±270 V common-mode.

High Current

For current-sensing applications, ensure that the power rating of the sense resistor is sufficient for the application and all proper safety practices must be followed.

Outline Dimensions

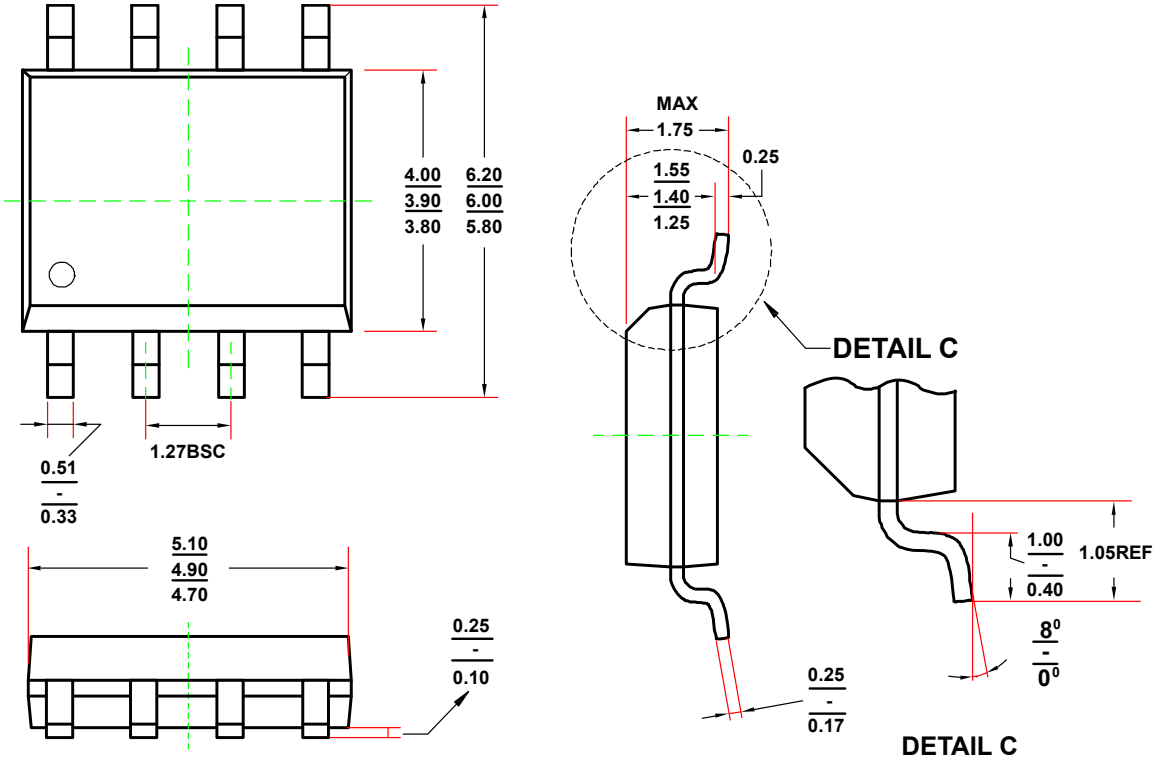
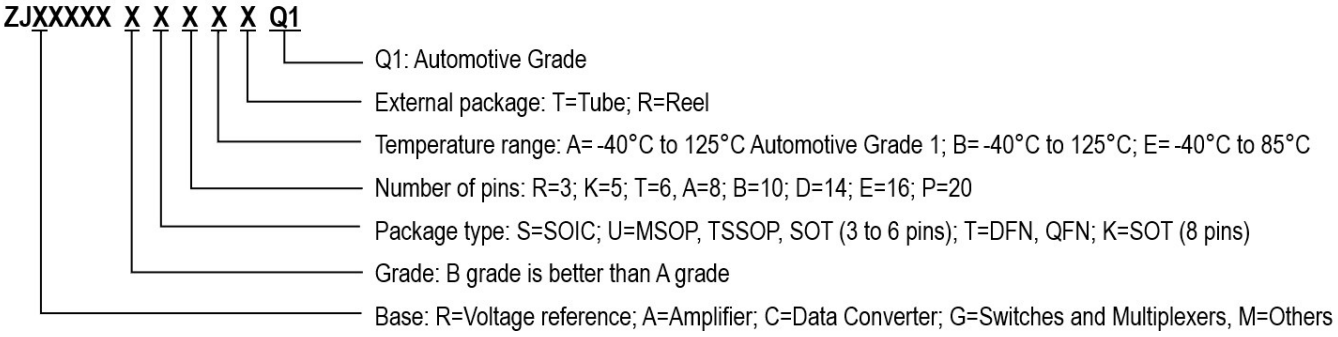


Figure 39. 8-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Package	Temperature Range (°C)	External Package
ZJA3669	ZJA3669ASABT	SOIC-8	-40 to 125	Tube
	ZJA3669ASABR			13” reel

Product Order Model



Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN 16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV