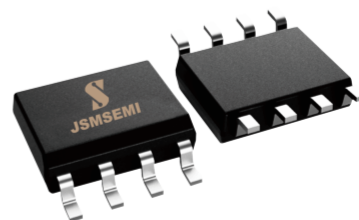


1 Description

The JSM2006G is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 650 V.

2 Features

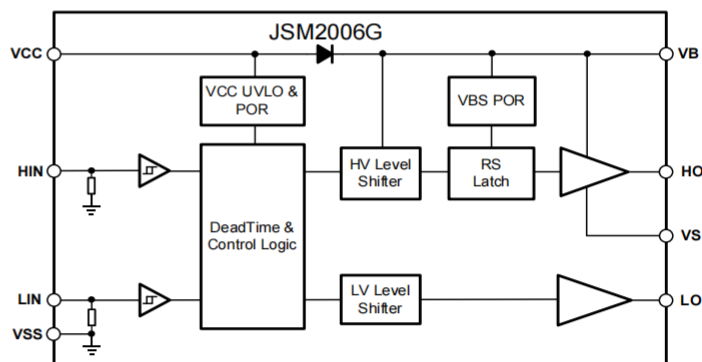
- Floating channel designed for bootstrap operation
- Fully operational to +650 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ± 50 V/ns
- Allowable negative Vs capability: -9V
- Undervoltage lockout for both channels
 - VCC UVLO threshold 8.7V/7.7V
 - VBS UVLO threshold 8.2V/7.3V
- Propagation delay
 - Ton/Toff = 250ns/150ns
 - Matching delay time 50ns
- Cross-conduction prevention logic
 - Deadtime 130ns
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 0.6A/1A
- RoSH compatible



3 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Functional Block Diagram



4 Function Pin Description

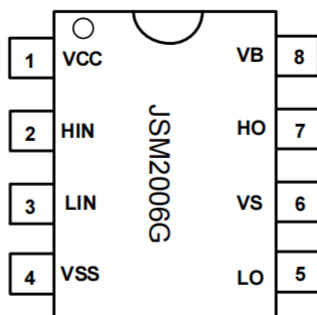


Table4-1 Lead Definitions

Number	Symbol	Description
1	V _{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	LIN	Logic input for low side gate driver output (LO), in phase
4	V _{SS}	Low side return
5	LO	Low side gate drive output
6	V _S	High side floating supply return
7	HO	High side gate drive output
8	V _B	High side floating supply

5 Product Specifications

5.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	-0.3	650	V
V _S	High side floating supply return	V _B - 25	V _B + 0.3	
V _{HO}	High side gate drive output	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and main power supply	-0.3	25	
V _{LO}	Low side gate drive output	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input of HIN & LIN	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

5.2 ESD Rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	2000	—	V
	Machine Model	1000	—	V

5.3 Rated Power

Symbol	Definition	MIN.	MAX.	Units
P _D	Package Power Dissipation @ TA ≤ 25°C	—	625	mW

5.4 Thermal Information

Symbol	Definition	MIN.	MAX.	Units
R _{thJA}	Thermal Resistance, Junction to Ambient	—	200	°C/W
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

5.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	V _S + 10	V _S + 20	V
V _S	High side floating supply return	-9	600	
V _{HO}	High side gate drive output	V _S	V _B	
V _{CC}	Low side and main power supply	10	20	
V _{LO}	Low side gate drive output	0	V _{CC}	
V _{IN}	Logic input of HIN & LIN	0	V _{CC}	
T _A	Ambient temperature	-40	125	°C

Note1: Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design.

5.6 Electrical Characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC} = V_B = 15\text{V}$, $C_L = 1\text{nF}$, unless otherwise specified

5.6.1 Dynamical Electrical Characteristics

t_{ON}	Turn-on propagation delay	—	250	300	ns	$V_S = 0\text{V}$
t_{OFF}	Turn-off propagation delay	—	150	200	ns	$V_S = 600\text{V}$
t_R	Turn-on rise time	—	70	130	ns	
t_F	Turn-off fall time	—	35	70	ns	
DT	Deadtime	—	—	50	ns	
MT	Matching delay(t_{ON}, t_{OFF})	—	—	50	ns	
MT	Matching delay(t_{ON}, t_{OFF})	—	—	60	ns	

5.6.2 Static Electrical Characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC} = V_B = 15\text{V}$, $C_L = 1\text{nF}$, unless otherwise specified.

V_{CCUV+}	VCC supply UVLO threshold	7.7	8.7	9.7	V	
V_{CCUV-}		6.7	7.7	8.7	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	1	—	V	
V_{BSUV+}	VBS supply UVLO threshold	7.2	8.2	9.2	V	
V_{BSUV-}		6.3	7.3	8.3	V	
$V_{BSUVHYS}$	hysteresis of V_{BS} UVLO	—	0.9	—	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	$V_B = V_S = 600\text{V}$
I_{QBS}	Quiescent VB supply current	—	35	100	μA	$V_{IN} = 0\text{V}$
I_{QCC}	Quiescent VCC supply current	—	60	150	μA	$V_{IN} = 0\text{V}$
V_{IH}	Logic "1" (HIN&LIN) input voltage	2.5	—	—	V	$V_{CC} = 10\text{V to } 20\text{V}$
V_{IL}	Logic "0" (HIN&LIN) input voltage	—	—	0.8	V	$V_{CC} = 10\text{V to } 20\text{V}$
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	0.2	V	$I_O = 0\text{A}$
V_{OL}	Low level output voltage, V_O	—	—	0.2	V	$I_O = 0\text{A}$
I_{IN+}	Logic "1" Input bias current	—	25	60	μA	$HIN = 5\text{V}, LIN = 5\text{V}$
I_{IN-}	Logic "0" Input bias current	—	—	5	μA	$HIN = 0\text{V}, LIN = 0\text{V}$
I_{O+}	Output high short circuit pulsed current	0.27	0.6	—	A	$V_O = 0\text{V}$ $PW \leq 10\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	0.4	1	—	A	$V_O = 15\text{V}$ $PW \leq 10\mu\text{s}$

6 Function Description

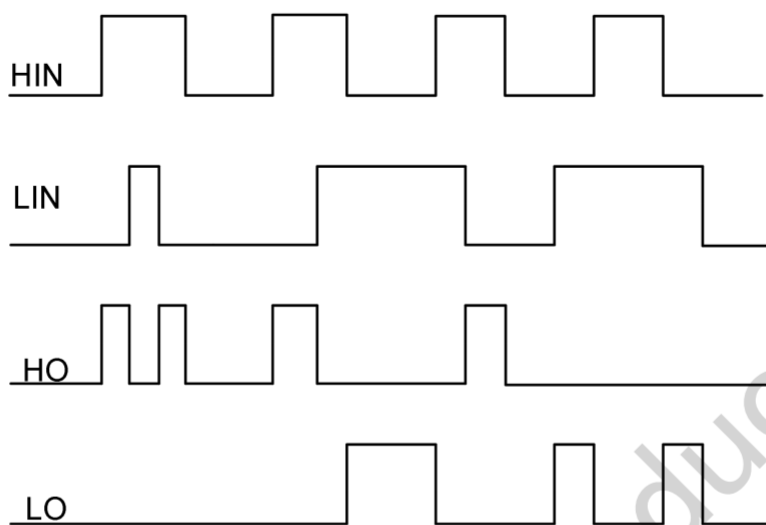


Figure 6-1 JSM2006G Input and output timing waveform

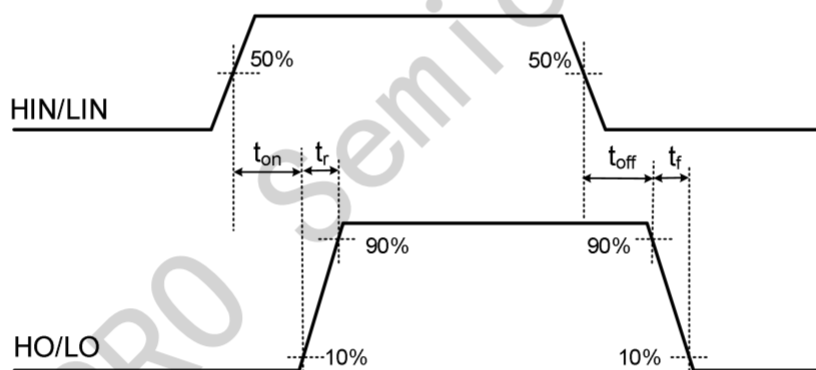


Figure 6-2 Propagation Time Waveform Definition

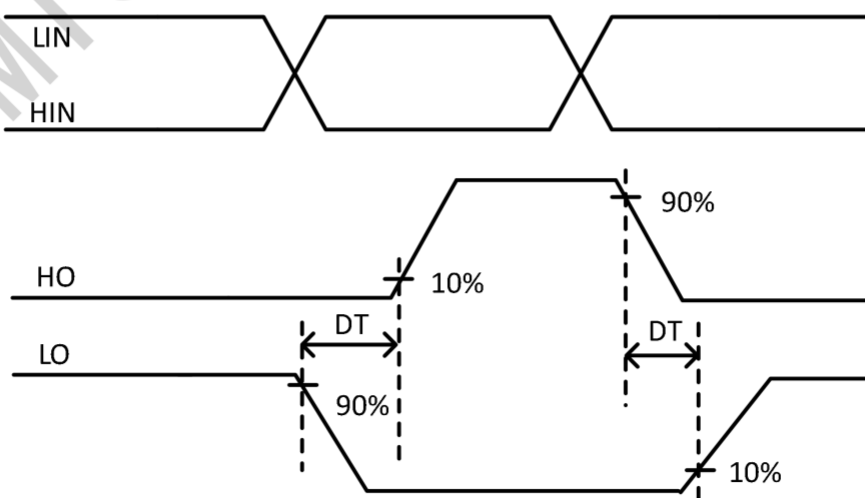


Figure 6-3 Cross Conduction Prevention Delay Time Waveform Definition

7 JSM2006G Description

7.1 Function Block Diagram

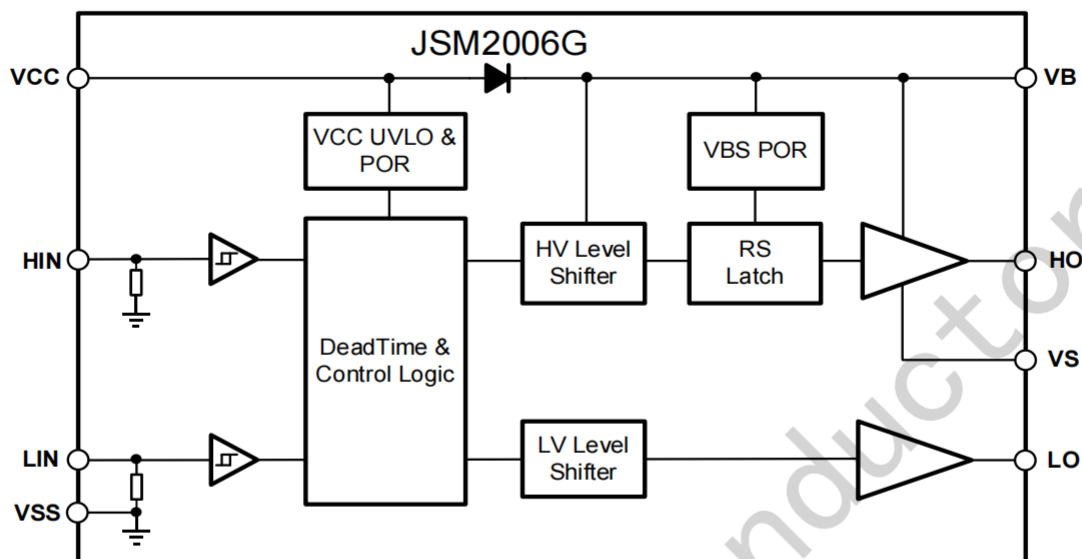


Figure7-1 Function Block Diagram of JSM2006G

7.2 Application Diagram

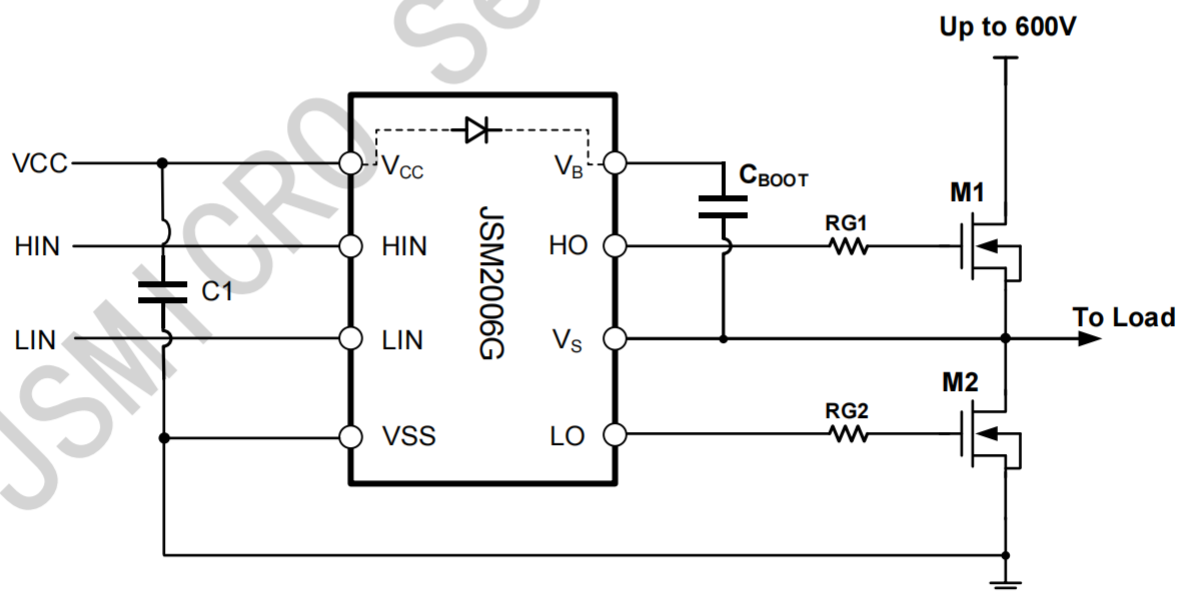
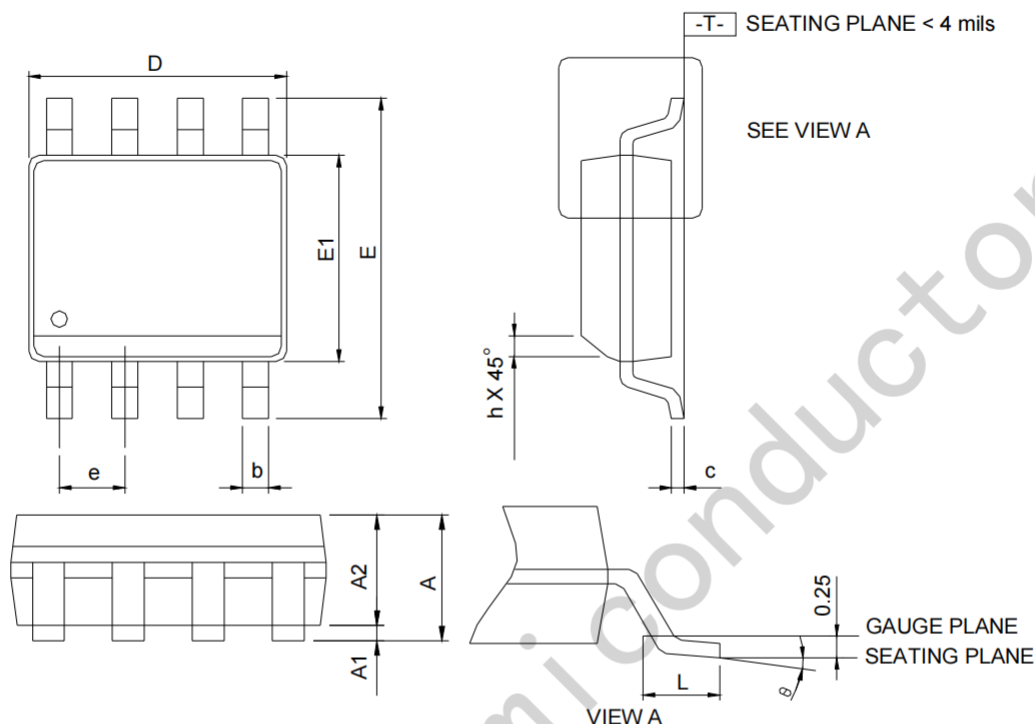


Figure7-2 Typical application circuit of JSM2006G

8 Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
- Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

