Features

- Senses Bus Voltages From 0V to 36V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power
- High Accuracy
- Configurable Averaging Options
- 16 Programmable Addresses
- Operates from 2.7-V to 5.5-V Power Supply
- 10-Pin, MSOP Package

Applications

- Power management
- Servers
- Telecom Equipment
- Computing
- Test Equipment

Description

The TPA626 is a current and power monitor, with I^2C or SMBUS-compatible interface. The device monitors both a shunt voltage drop and bus supply voltage.

The TPA626 common mode input voltage can vary from 0V to 36V.

The TPA626 features up to 16 programmable addresses on the I^2C-compatible interface.

Function block or application schematic

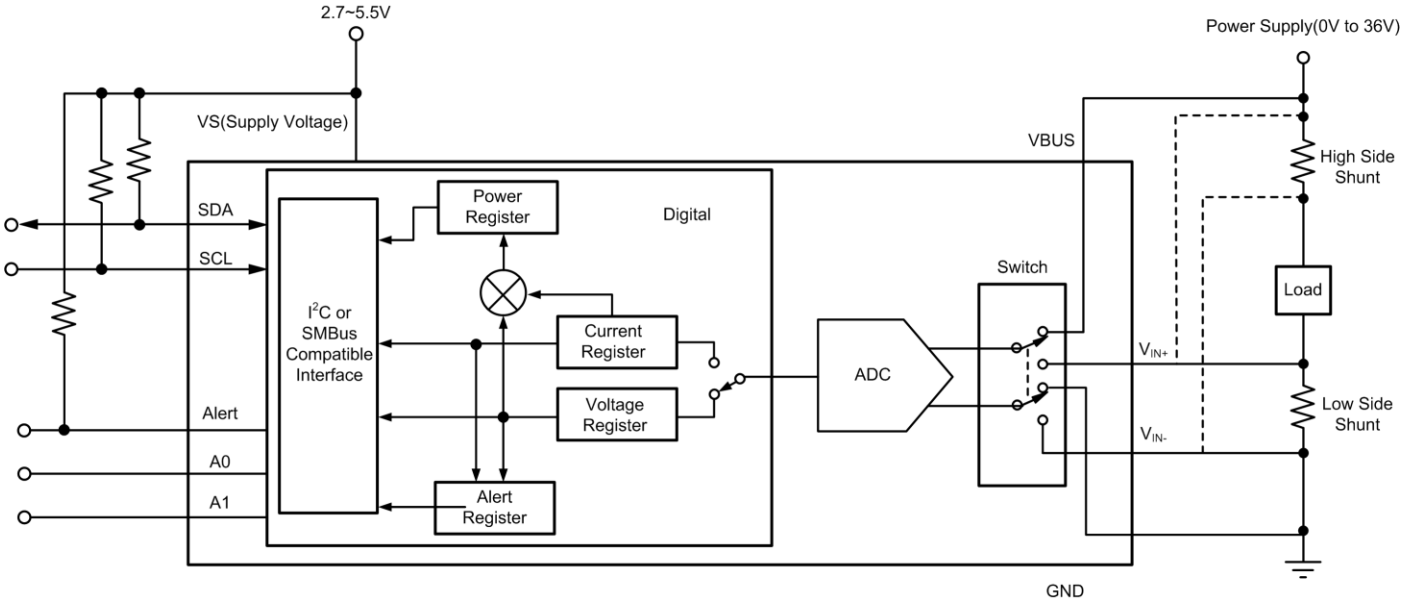
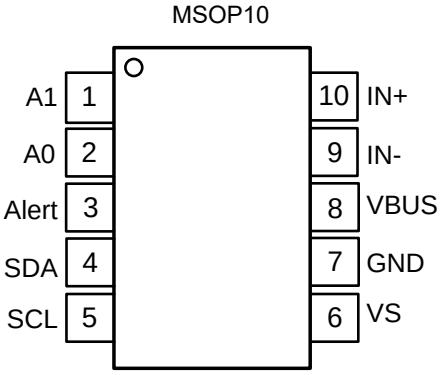


Figure 1.

Table of Contents

Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	2	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
A1	1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
Alert	3	Digital output	Multi-functional alert, open-drain output.
GND	7	Analog	Ground.
IN+	10	Analog input	Connect to supply side of shunt resistor.
IN–	9	Analog input	Connect to load side of shunt resistor.
SCL	5	Digital input	Serial bus clock line, open-drain input.
SDA	4	Digital I/O	Serial bus data line, open-drain input/output.
VBUS	8	Analog input	Bus voltage input.
VS	6	Analog	Power supply, 2.7 V to 5.5 V.

Order Information

Model Name	Order Number	Package	MSL Level	Transport Media, Quantity	Marking Information
TPA626	TPA626-VR-S	MSOP10	1	Tape and Reel, 3000	TPA626

Absolute Maximum Ratings

Cover operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VS}	Supply voltage		6	V
Analog Inputs, IN+, IN–	Differential (V_{IN+} – V_{IN-})(2)	–40	40	V
	Common-Mode (V_{IN+} + V_{IN-}) / 2	–0.3	40	
V_{VBUS}		–0.3	40	V
V_{SDA}		GND – 0.3	6	V
V_{SCL}		GND – 0.3	V_{VS} + 0.3	V
I_{IN}	Input current into any pin		5	mA
I_{OUT}	Open-drain digital output current		10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) IN+ and IN– may have a differential voltage between –40 V and 40 V. However, the voltage at these pins must not exceed the range –0.3 V to 40 V.

ESD, Electrostatic Discharge Protection

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

Recommended Operating Conditions

		Min	Typ	Max	Unit
V_{CM}	Common mode input voltage		12		V
V_{VS}	Operating supply voltage		3.3		V
T_A	Operating free-air temperature	-40		125	

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	171	42.9	°C/W

Electrical Characteristics

T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Shunt voltage input range		–81.9175		81.92	mV
	Bus voltage input range(1)		0		36	V
CMRR	Common-mode rejection	0 V ≤ V_{IN+} ≤ 36 V	120	140		dB
V_{OS}	Shunt offset voltage, RTI(2)			±2.5	±30	µV
	Shunt offset voltage, RTI(2) vs temperature	–40°C ≤ T_A ≤ 125°C		0.15		µV/°C
PSRR	Shunt offset voltage, RTI(2) vs power supply	2.7 V ≤ VS ≤ 5.5 V		5		µV/V
V_{OS}	Bus offset voltage, RTI(2)			±10	±20	mV
	Bus offset voltage, RTI(2) vs temperature	–40°C ≤ T_A ≤ 125°C		60		µV/°C
PSRR	Bus offset voltage, RTI(2) vs power supply			1		mV/V
I_B	Input bias current				10	µA
	VBUS input impedance			830		kΩ
	Input leakage (3)	(IN+ pin) + (IN– pin), Power-down mode		1		µA
DC ACCURACY						
	ADC native resolution			16		Bits
	1 LSB step size	Shunt voltage		2.5		µV
		Bus voltage		1.25		mV
	Shunt voltage gain error			0.02%	0.4%	
	Shunt voltage gain error vs temperature	–40°C ≤ T_A ≤ 125°C		50		ppm/°C
	Shunt voltage linearity				0.5%	
	Bus voltage gain error			0.02%	0.4%	
	Bus voltage gain error vs temperature	–40°C ≤ T_A ≤ 125°C		50		ppm/°C
	Bus voltage linearity				0.5%	
t_{CT}	ADC conversion time	CT bit = 000		66		µs
		CT bit = 001		134		
		CT bit = 010		269		

		CT bit = 011	542		
		CT bit = 100	1085		µs
		CT bit = 101	2170		
		CT bit = 110	4341		
		CT bit = 111	8682		
SMBus					
SMBus timeout(4)			28		ms

(1) While the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V.
(2) RTI = Referred-to-input.
(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(4) SMBus timeout in the TPA626 resets the interface any time SCL is low for more than 28 ms.
(5) Test Levels: (A) Tested at final test. Over temperature limits are set by characterization and simulation. (B) Set by characterization and simulation. (C) Typical value only for information, provided by design simulation.

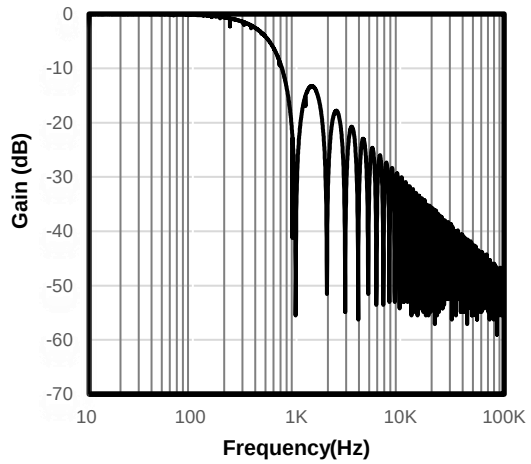
Electrical Characteristics

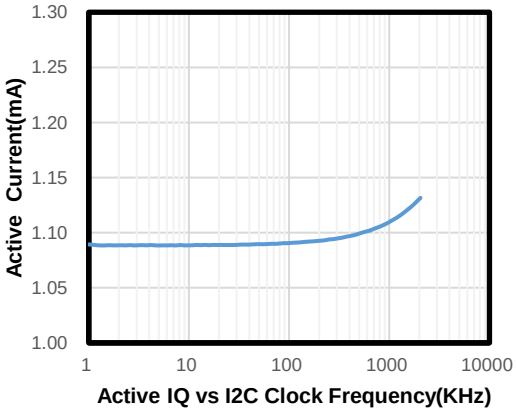
T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted

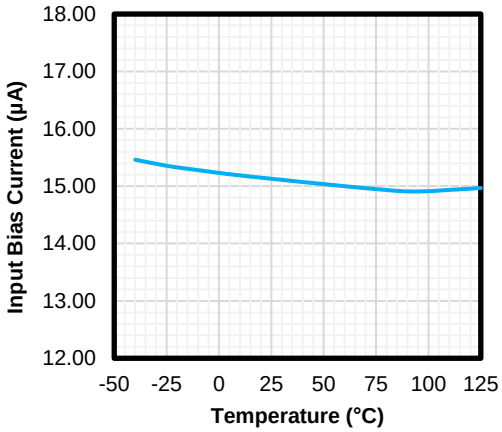
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Input capacitance			3		pF
	Leakage input current	0 V ≤ V_{SCL} ≤ V_{VS} , 0 V ≤ V_{SDA} ≤ V_{VS}, 0 V ≤ V_{Alert} ≤ V_{VS} , 0 V ≤ V_{A0} ≤ V_{VS} , 0 V ≤ V_{A1} ≤ V_{VS}		0.1		µA
V_{IH}	High-level input voltage		0.7×V_{VS}			V
V_{IL}	Low-level input voltage				0.3×V_{VS}	V
V_{OL}	Low-level output voltage, SDA, Alert		0		0.4	V
	Hysteresis			150		mV
POWER SUPPLY						
	Operating supply range		2.7		5.5	V
I_Q	Quiescent current			1100		µA
	Quiescent current, power-down (shutdown) mode			8		µA
V_{POR}	Power-on reset threshold			2.2		V

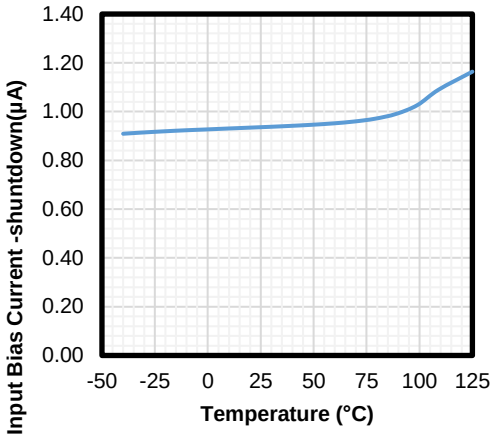
Typical Performance Characteristics

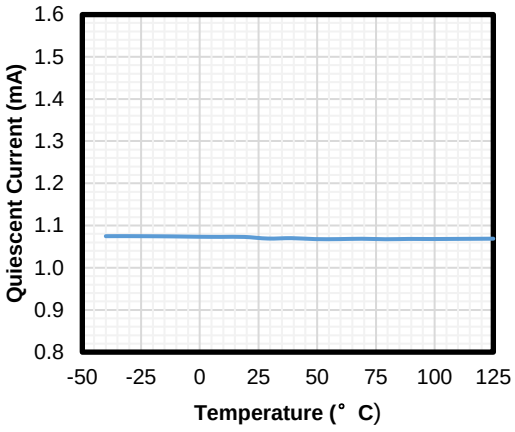
At T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted.

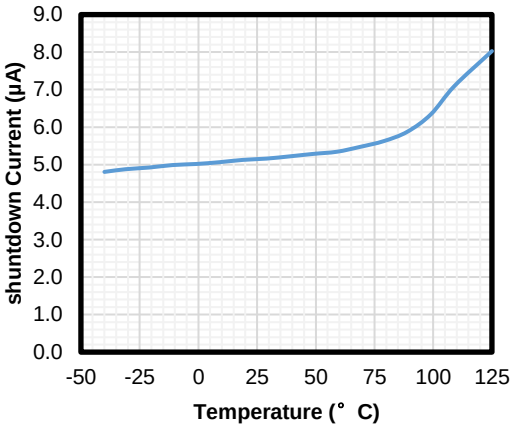




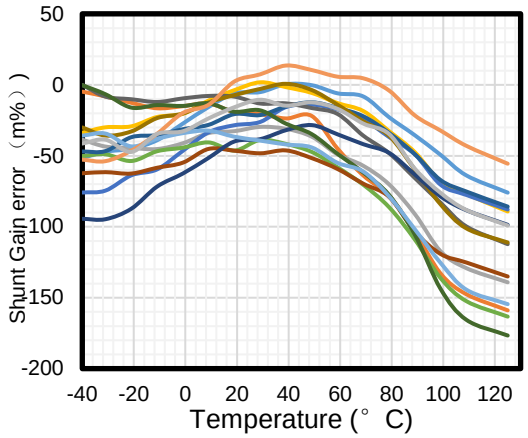


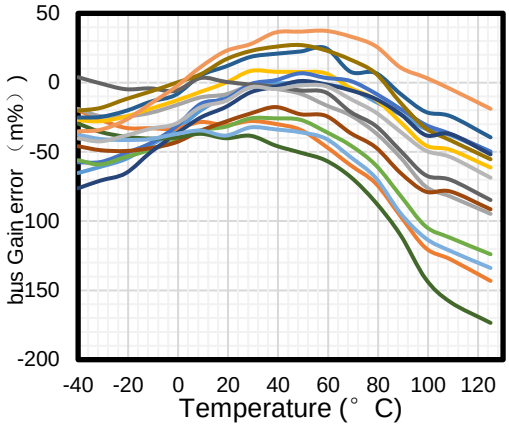


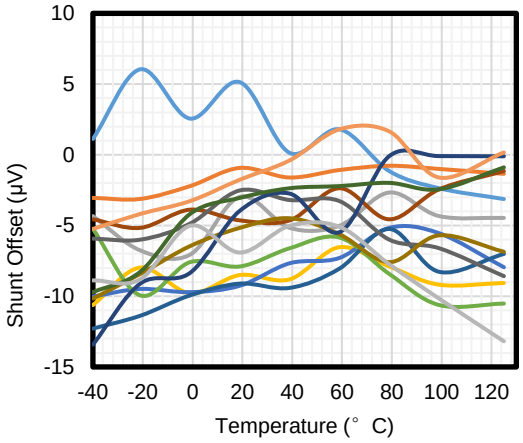


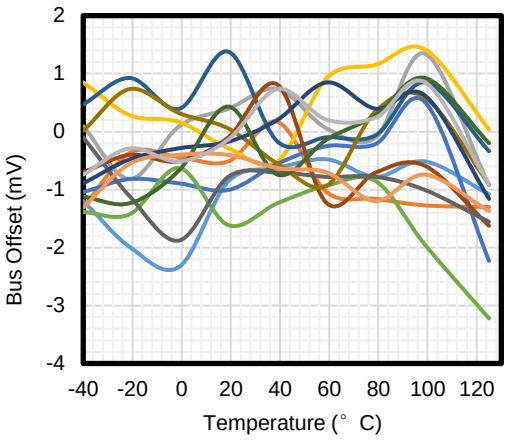


At T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted.









Detailed description

The TPA626 is a digital current sense amplifier with an I2C- and SMBus-compatible interface. It performs two measurements on the power-supply bus: The differential shunt voltage created by load current flowing through a shunt resistor is measured at the IN+ and IN– pins. And the power supply bus voltage is measured at the VBUS pin.

There are no special requirements for power supply sequencing, since power supply and input voltages are independent of each other.

Programming

Table 1 lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 1 Calculating Current and Power

STEP	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Step 1	Configuration Register	00h	4127h	—	—	—
Step 2	Shunt Register	01h	1F40h	8000	2.5 µV	20 mV
Step 3	Bus Voltage Register	02h	2570h	9584	1.25 mV	11.98 V
Step 4	Calibration Register	05h	A00h	2560	—	—
Step 5	Current Register	04h	2710	10000	1 mA	10 A
Step 6	Power Register	03h	12B8h	4792	25 mW	119.82 W

I2C address

The device has two address pins, A0 and A1. The device samples the state of pins A0 and A1 on every bus communication. Following table lists the pin logic levels for each of the 16 possible addresses.

Table 2 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110

SCL	SCL	1001111

Register map

Table 3 Register Set Summary

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE(1)
HEX			BINARY	HEX	
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	01000001 00100111	4127	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	00000000 00000000	0000	R
02h	Bus Voltage Register	Bus voltage measurement data.	00000000 00000000	0000	R
03h	Power Register(2)	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
04h	Current Register(2)	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R

Table 4

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE(1)
HEX			BINARY	HEX	
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	00000000 00000000	0000	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	00000000 00000000	0000	R/W
FEh	Manufacturer ID Register	Contains unique manufacturer identification number.	0101010001001001	5549	R
FFh	Die ID Register	Contains unique die identification number.	0010001001100000	2260	R

Table 5 Configuration Register (00h) (Read/Write) Descriptions

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSHCT2	VSHCT1	VSHCT0	MODE3	MODE2	MODE1
POR VALUE	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

Table 6 AVG Bit Settings[11:9] Combinations

AVG 2 D11	AVG1 D10	AVG0 D9	NUMBER OF AVERAGES(1)
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

(1) Shaded values are default.

Table 7 VBUSCT Bit Settings [8:6] Combinations

VBUSCT2 D8	VBUSCT1 D7	VBUSCT0 D6	CONVERSION TIME (μS)
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170
1	1	0	4341
1	1	1	8682

Table 8 VSHCT Bit Settings [5:3] Combinations

VSHCT2 D5	VSHCT1 D4	VSHCT0 D3	CONVERSION TIME(1)
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170
1	1	0	4341
1	1	1	8682

Table 9 Mode Settings [2:0] Combinations

MODE 3 D2	MODE2 D1	MODE1 D0	MODE(1)
0	0	0	Power-Down (or Shutdown)
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	Power-Down (or Shutdown)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

Table 10 Shunt Voltage Register (01h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 11 Bus Voltage Register (02h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 12 Power Register (03h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 13 Current Register (04h) (Read-Only) Register Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14 Calibration Register (05h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15 Mask/Enable Register (06h) (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: Shunt Voltage Over-Voltage
Bit 15
Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.

SUL: Shunt Voltage Under-Voltage
Bit 14
Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.

BOL: Bus Voltage Over-Voltage
Bit 13
Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.

BUL: Bus Voltage Under-Voltage
Bit 12
Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.

POL: Power Over-Limit
Bit 11
Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.

CNVR: Conversion Ready
Bit 10

Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.

AFF: Alert Function Flag
Bit 4
While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert.
When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.

CVRF: Conversion Ready Flag
Bit 3
Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions:
1.) Writing to the Configuration Register (except for Power-Down selection)
2.) Reading the Mask/Enable Register

OVF: Math Overflow Flag
Bit 2
This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.

APOL: Alert Polarity bit; sets the Alert pin polarity.
Bit 1
1 = Inverted (active-high open collector)
0 = Normal (active-low open collector) (default)

LEN: Alert Latch Enable; configures the latching feature of the Alert pin and Alert Flag bits.
Bit 0
1 = Latch enabled
0 = Transparent (default)
When the Alert Latch Enable bit is set to transparent mode, the Alert pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

Table 16 Alert Limit Register (07h) (Read/Write) Description

ddBIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17 Manufacturer ID Register (FEh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
POR VALUE	0	1	0	1	0	1	0	1	0	1	0	0	1	0	0	1

Table 18 Die ID Register (FFh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	RID3	RID2	RID1	RID0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

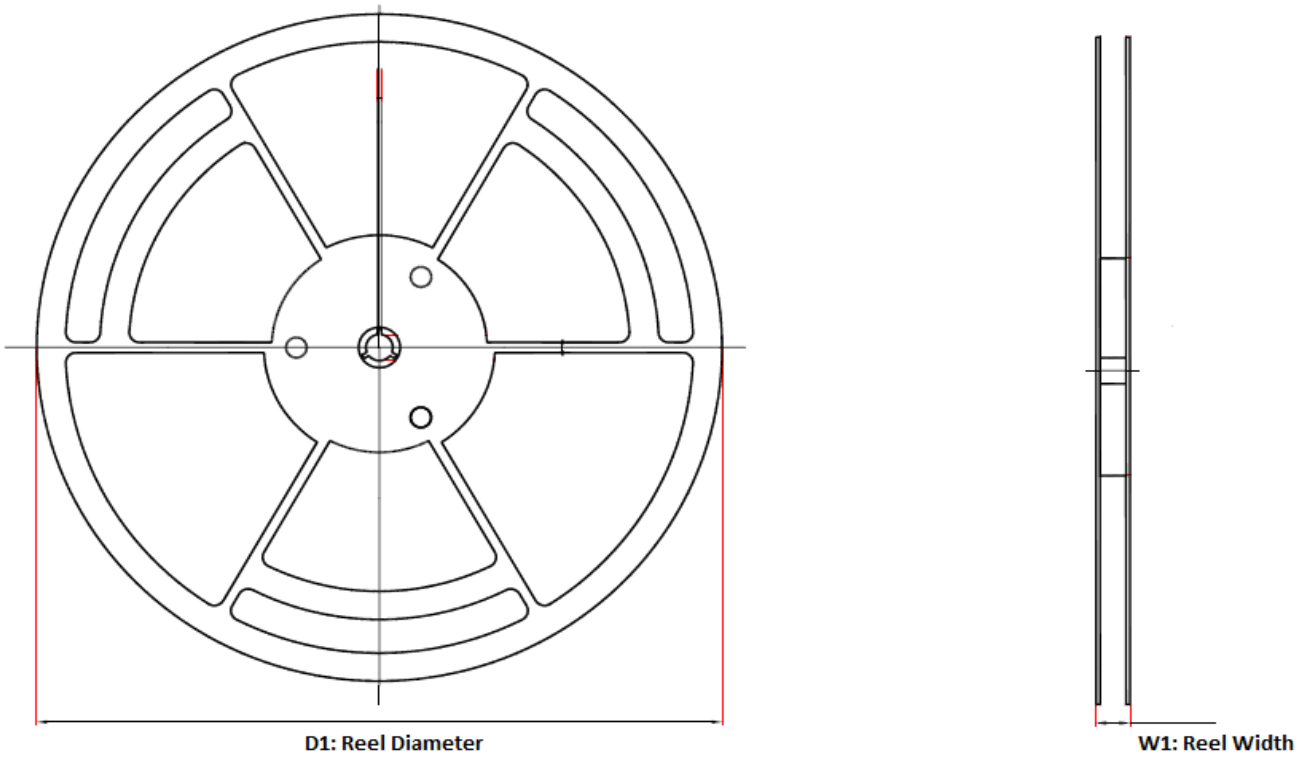
Detailed description

The device could not accept stop command immediately after a start operation. If customer wants to reset I2C communication, 9 clocks could be sent to TPA626 after a start operation, to make sure the device quite to default mode, and then wait for a new I2C start operation.

SMBUS alert function is supported respond to the SMBus Alert Response address (0001 100) when an alert occurs. But be aware when master is accessing the address if the device doesn't has alert, the device will still acknowledge to address but without following response.

I^2C Data hold time should be at least 10nS for a proper start function is recognized.

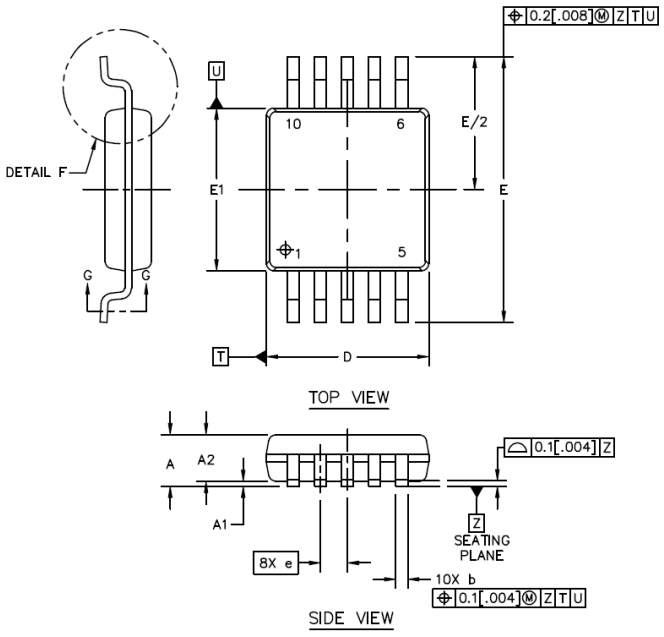
Tape And Reel Information



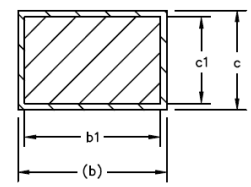
Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
	MSOP10	330.0	17.6	5.20	3.30	1.50	8.0	12.0	Q1

Package Outline Dimensions

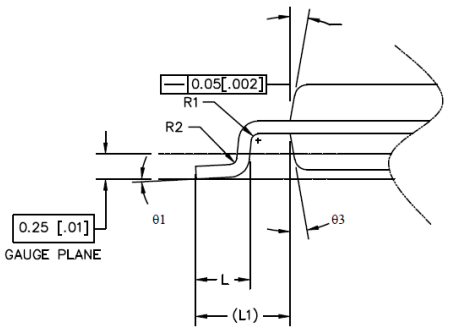
MSOP10



		SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS		A	0.86		1.04	.034		.041
STAND OFF		A1	0.05		0.13	.002		.005
MOLD THICKNESS		A2	0.81		0.91	.032		.036
LEAD WIDTH(PLATING)		b	0.17		0.27	.007		.011
LEAD WIDTH		b1	0.17		0.23	.007		.009
L/F THICKNESS(PLATING)		c	0.13		0.2	.005		.008
L/F THICKNESS		c1	0.08		0.18	.003		.007
BODY SIZE	X	D	2.9	3	3.1	.114	.118	.122
	Y	E1	2.9	3	3.1	.114	.118	.122
		E	4.8	4.9	5	.189	.193	.197
LEAD PITCH		e	0.5 BSC			.02 BSC		
		L	0.445	0.546	0.648	.018	.021	.026
FOOTPRINT		L1	0.95 REF			.037 REF		
		θ1	0°		6°	0°		6°
		θ2	5°		15°	5°		15°
		θ3	5°		15°	5°		15°
		R1	0.07		---	.003		---
		R2	0.07		---	.003		---



SECTION G–G
SCALE: 150/1



DETAIL F
ROTATED 90° CCW
SCALE: 22/1

Revision History

Date	Version	Note
2019/9/6	A.01	First version
2019/11/23	A.02	Add Ib bias current max limit. Add shunt and bus linearity parameters. Correct register bit number typo in Table 8
2020/09/04	A.03	Add notice for no requirements of power up sequence.
2020/09/11	A.04	Update register explanations.
2021/5/25	A.05	Update diagram
2021/12/8	A.06	Update recommended operating conditions
2022/12	A.07	Update application information

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