Low Power, Precision Instrumentation Amplifier

Features

- Gain Set with One External Resistor (Gain range 1 to 10,000)
- High CMRR: 93 dB min (G = 10)
- Low Input Offset Voltage: 125 μV max
- Low Input Offset Drift: 0.1 μV/°C
- Low Input Bias Current: 2 nA max
- Low Noise: 6.5 nV/$\sqrt{\text{Hz}}$
- 0.2 μV_{P-P} Input Noise (0.1 Hz to 10 Hz, G = 100)
- Bandwidth: 100 kHz (G = 100)
- Supply Current: 1.3 mA
- Supply Voltage: ±2.3 V to ±18 V
- Specified Temperature Range: -40 °C to +85 °C

Applications

- Precision Data Acquisition
- Instrumentation
- Sensor Signal Conditioning
- Industrial Control

ZJA3600 Product Family

Part Number	Gain Setting	
	G = 1 + 49.4 kΩ/R_G	G = 1 + 50 kΩ/R_G
Classic Pinout	ZJA3600	ZJA3618
	ZJA3610 (G ≥ 10)	ZJA3608 (G ≥ 10)
Optimized Pinout	ZJA3601	ZJA3619
	ZJA3611 (G ≥ 10)	ZJA3609 (G ≥ 10)

General Description

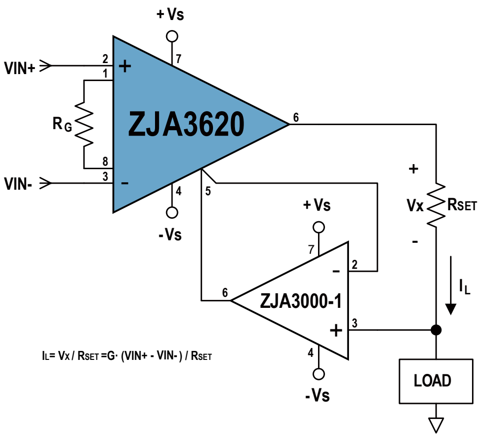
The ZJA3620 is a precision, low-noise instrumentation amplifier that can be used to set the gain range from 1 to 10,000 with a single external resistor.

The ZJA3620 is based on classic three-op-amp structure to provide high common-mode rejection ratio (CMRR) over 93 dB at a gain of 10. This allows it to accurately amplify useful signals in the presence of large external interference, which is a common situation in precision data acquisition, bridge sensor interface, thermocouples, and medical signal acquisition (such as ECG, EEG, etc.).

The ZJA3620 has excellent dc and ac performances. It has low offset voltage of 125 μV max, offset drift of 0.1 μV/°C, and the bias current is 2 nA max, to lower the system calibration cost. The ZJA3620 works well as a preamplifier due to its low input voltage noise of 6.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz, 0.2 μV_{P-P} in the 0.1 Hz to 10 Hz band at the gain of 100. Also, the ZJA3620 is well suited for multiplexed applications with its settling time of 13 μs to 0.01%, slew rate of 1.2 V/μs and bandwidth of 400 kHz at the gain of 10.

The ZJA3620 perform is specified temperature range of -40 °C to +85 °C. Its supply voltage is from ±2.3 V to ±18 V. The ZJA3620 is available in 8-lead SOIC package.

Application Examples



Typical Performance Characteristics

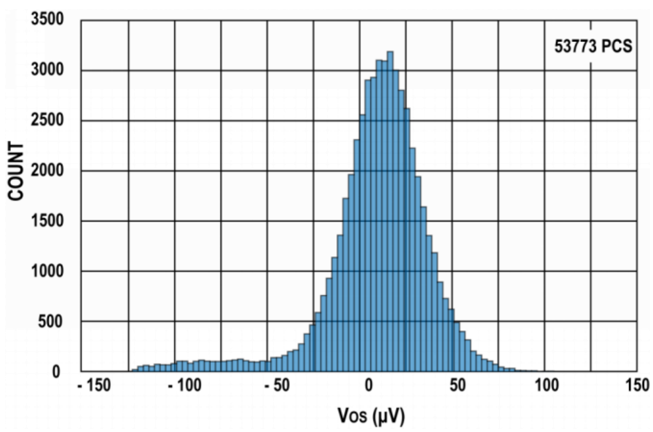


Table of contents

Version (Release A) [1]

Revision History

Nov 2024——Release A

English version

Updated Outline Dimensions, Ordering Guide, Orderable Device Explanation, Related Parts

June 2023

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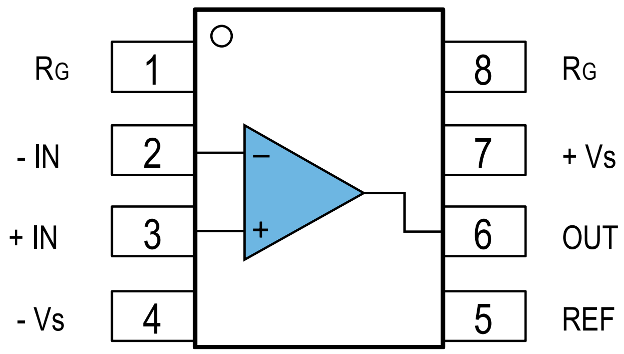
Pin Configurations and Function Descriptions



ZJA3620 Pin Configuration (8-lead SOIC)

Mnemonic	Pin No.	I/O [1]	Description
R_G	1	AI	Gain setting pin. Place a gain resistor between pin 1 and pin 8
-IN	2	AI	Inverting input
+IN	3	AI	Non-inverting input
$-V_S$	4	P	Negative power supply
REF	5	AI	Reference input. This pin must be driven by a low impedance source
OUT	6	AO	Output
$+V_S$	7	P	Positive power supply
R_G	8	AI	Gain setting pin. Place a gain resistor between pin 1 and pin 8

[1] AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±Vs
Differential Input Voltage (G = 1 to10)	25 V
Operating Temperature Range	-40 °C to 85 °C
Storage Temperature Range	-65 °C to 150 °C
Maximum Reflow Temperature [2]	150 °C
Lead Temperature, Soldering (10 sec)	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	1.5 kV

Thermal Resistance [5]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	130	43	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] IPC/JEDEC J-STD-020 Compliant

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant

[5] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range (- 40 °C to 85 °C), otherwise specifications are at V_S = ±15 V, R_L= 2 kΩ, T_A = 25 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
GAIN		G = 1 + (49.4 kΩ / R_G)					
Gain Range				1		10,000	
Gain Error	GE	V_{OUT} = ±10 V					
G = 1				-0.10		0.10	%
G = 10				-0.30		0.30	%
G = 100				-0.30		0.30	%
G = 1,000				-0.70		0.70	%
Gain Nonlinearity		G = 1-100, V_{OUT} = -10 V to +10 V					
		R_L = 10 kΩ			10	50	ppm
		R_L = 2 kΩ			10	95	ppm
Gain vs Temperature		G = 1	●			10	ppm/°C
		G > 1 [1]	●			50	ppm/°C
OFFSET VOLTAGE	V_{OS}	Total Error RTI $\left(V_{OS,RTI}\right) = V_{OSI} + \frac{V_{OSO}}{G}$					
Input Offset Voltage	V_{OSI}	V_S = ±4.5 V to ±16.5 V		-125		125	μV
Average TC	TCV_{OSI}	V_S = ±4.5 V to ±16.5 V	●		0.1		μV/°C
Output Offset Voltage	V_{OSO}	V_S = ±4.5 V to ±16.5 V		-1000	200	1000	μV
Average TC	TCV_{OSO}	V_S = ±4.5 V to ±16.5 V	●		2.5		μV/°C
POWER SUPPLY REJECTION RATIO	PSR	V_S = ±2.3 V to ±18 V					
G = 1				80	100		dB
G = 10				95	120		dB
G = 100				110	140		dB
G = 1,000				110	140		dB
INPUT BIAS CURRENT		V_S = ±16.5 V					
Input Bias Current	I_B				0.5	2	nA
Average TC			●		3		pA/°C
Input Offset Current	I_{OS}			-1		1	nA
INPUT CHARACTERISTICS							
Input Impedance	R_{IN} /C_{IN}	Differential Mode			10/2		GΩ/pF
		Common Mode			10/2		GΩ/pF
Input Operating Voltage Range [2]	IVR	G = 1, V_S = ±4.5 V		$-V_S$+1.9		$+V_S$-1.2	V
		G = 1, V_S = ±16.5 V		$-V_S$+1.9		$+V_S$-1.4	V

[1] The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
[2] One input is connected to ground.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common-Mode Rejection Ratio	CMRR	V_S = ±16.5 V				
G = 1			73	90		dB
G = 10			93	110		dB
G = 100			110	130		dB
G = 1,000			110	130		dB
OUTPUT CHARACTERISTICS						
Output Swing		V_S = ±2.3 V to ±4.5 V	$-V_S$+1.1		$+V_S$-1.2	V
		V_S = ±18 V	$-V_S$+1.2		$+V_S$-1.4	V
Short-Circuit Current	I_{SC}			±20		mA
DYNAMIC PERFORMANCE						
Small Signal Bandwidth, -3 dB		G = 1		700		kHz
		G = 10		400		kHz
		G = 100		100		kHz
		G = 1,000		12		kHz
Slew Rate	SR		0.75	1.2		V/μs
Settling Time (to 0.01%)	t_S	G = 1 to 100, 0 to 5 V step		13		μs
		G = 1,000, 0 to 5 V step		110		μs
NOISE PERFORMANCE						
Voltage Noise		f = 1 kHz				
Input Voltage Noise	e_{ni}			6.5	13	nV/√Hz
Output Voltage Noise	e_{no}			70	100	nV/√Hz
0.1 Hz to 10 Hz, Referred-To-Input (RTI)		G = 1		5		$\mu V_{P\text{-}P}$
		G = 10			0.8	$\mu V_{P\text{-}P}$
		G = 100		0.2	0.4	$\mu V_{P\text{-}P}$
Input Current Noise		f = 1 kHz		100		fA /√Hz
		0.1 Hz to 10 Hz		10		$pA_{P\text{-}P}$
REFERENCE INPUT						
R_{IN}				20		kΩ
I_{IN}		V_S = ±16.5 V		50	60	μA
Voltage Range			$-V_S$+1.6		$+V_S$-1.6	V
Reference Gain to Output			0.9999		1.0001	
POWER SUPPLY						
Operating Range			±2.3		±18	V
Quiescent Current	I_{SY}			1.3	1.7	mA
TEMPERATURE RANGE		Specified Temperature Range	-40		85	°C

Typical Performance Characteristics

Unless otherwise stated, V_S = ±15.0 V, I_{LOAD} = 0, C_L = 0.1 μF, T_A = 25 °C.

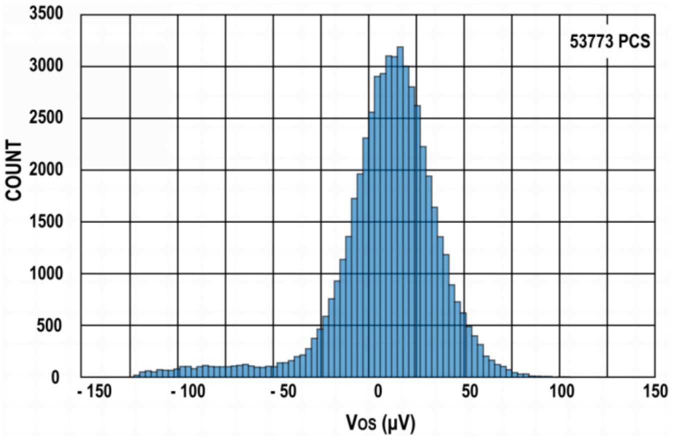


Figure 1. Typical Distribution of Input Offset Voltage

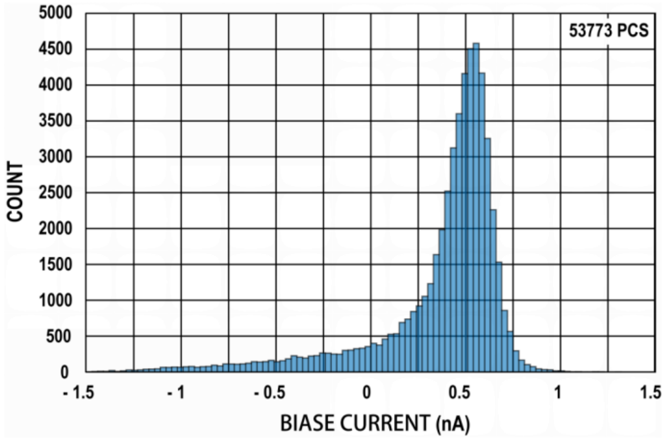


Figure 2. Typical Distribution of Input Bias Current

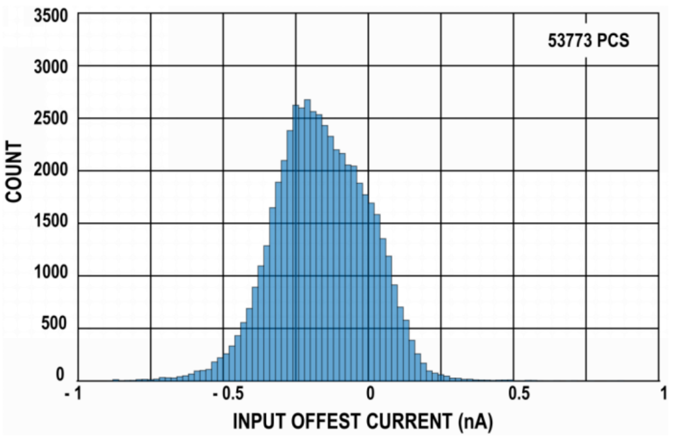


Figure 3. Typical Distribution of Input Offset Current

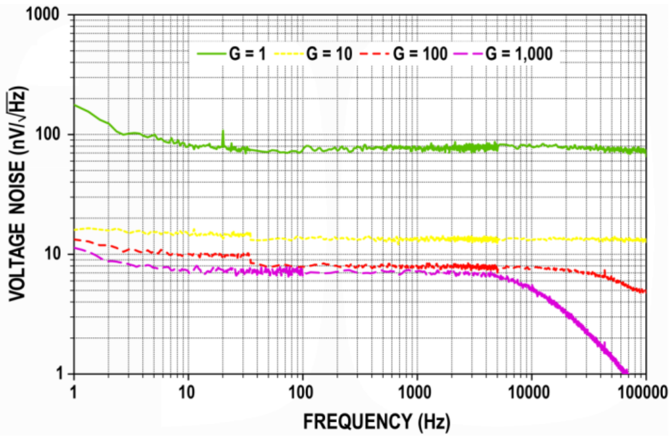


Figure 4. Voltage Noise Spectral Density vs. Frequency (G = 1 to 1000)

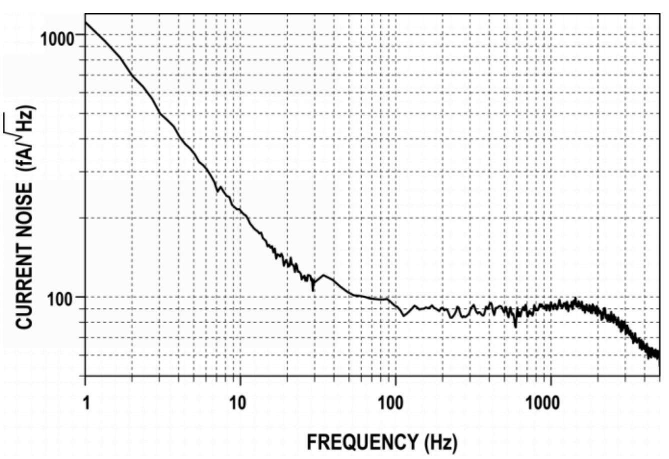


Figure 5. Current Noise Spectral Density vs. Frequency

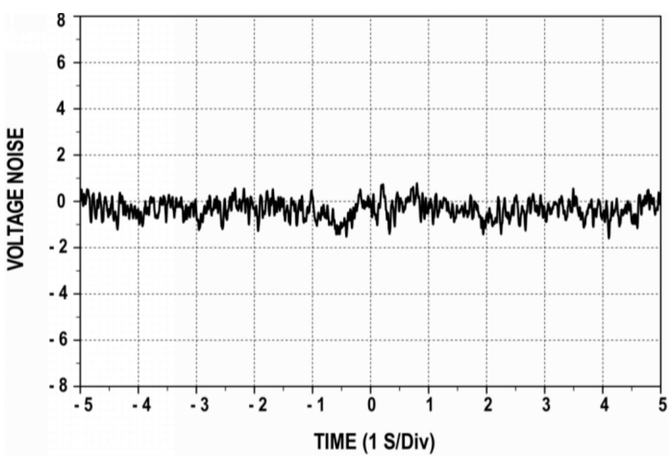


Figure 6. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

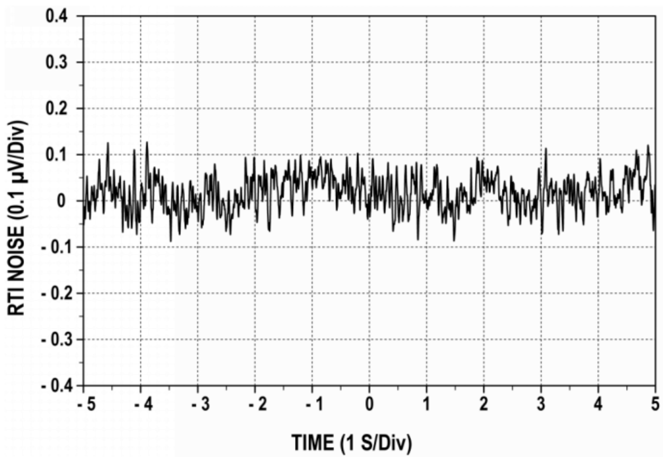


Figure 7. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

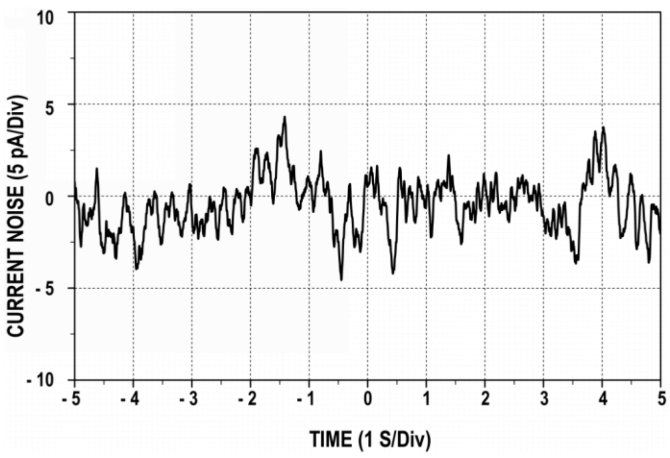


Figure 8. 0.1 Hz to 10 Hz Current Noise

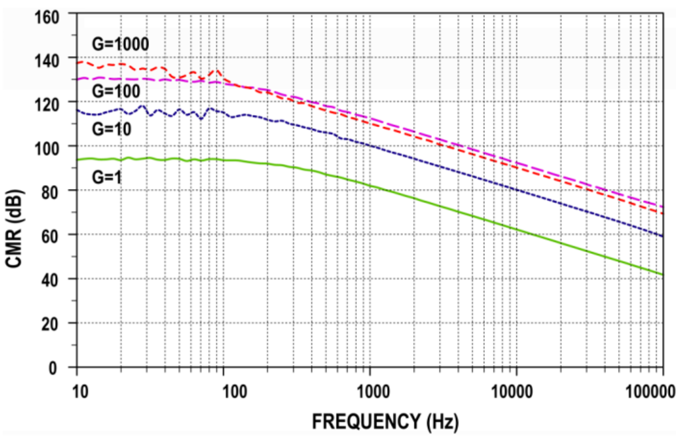


Figure 9. Typical CMR vs. Frequency, RTI

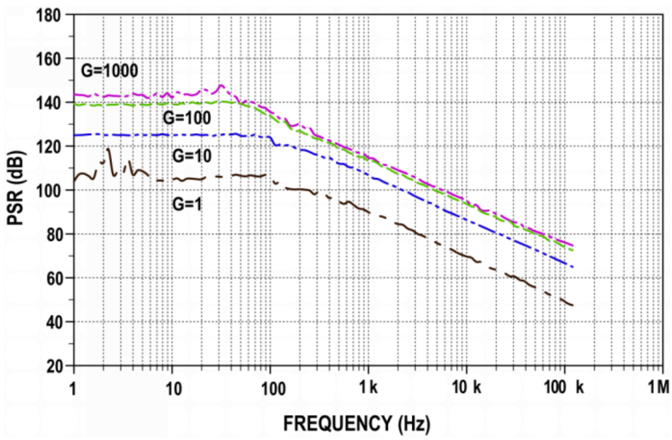


Figure 10. Positive PSR vs. Frequency, RTI (G = 1−1000)

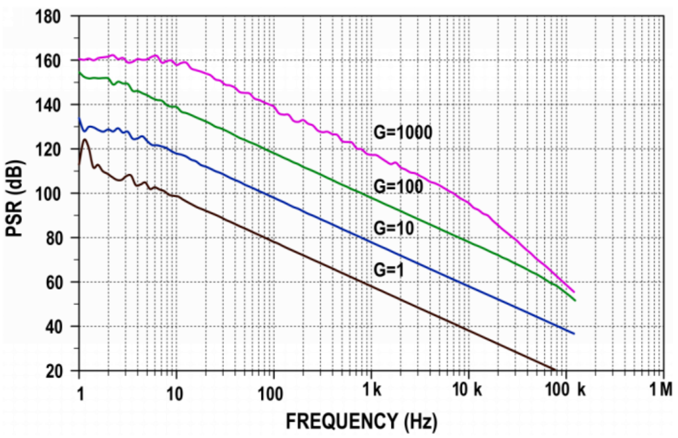


Figure 11. Negative PSR vs. Frequency, RTI (G = 1−1000)

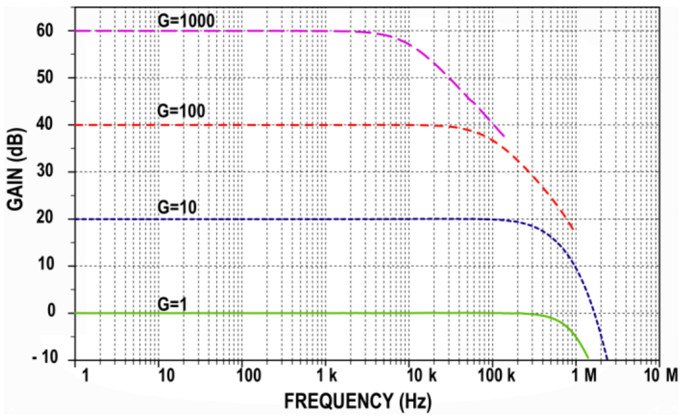


Figure 12. Gain vs. Frequency

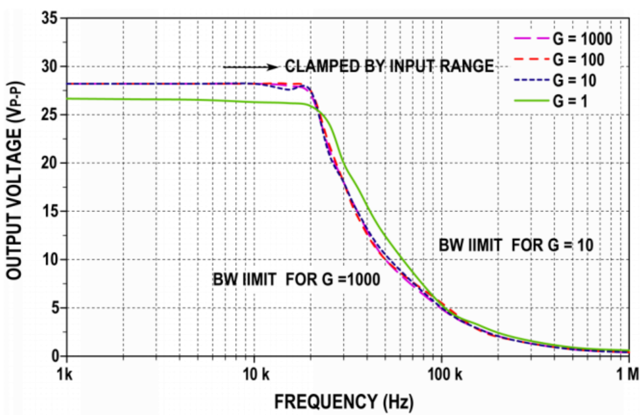


Figure 13. Large Signal Frequency Response

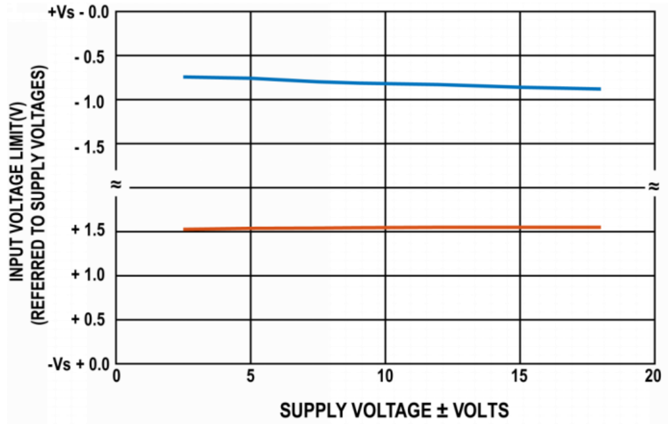


Figure 14. Input Voltage Range vs. Supply Voltage (G = 1)

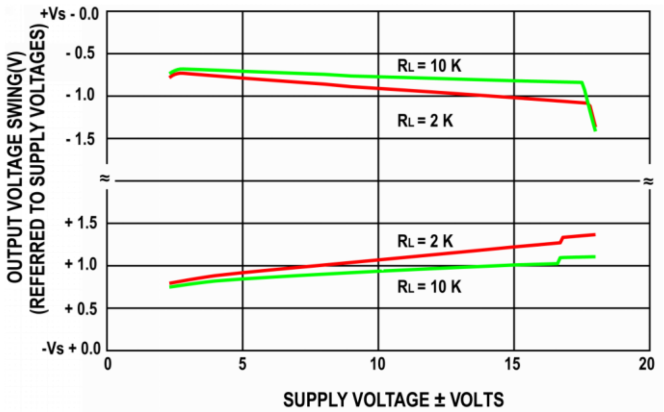


Figure 15. Output Voltage Swing vs. Supply Voltage (G = 10)

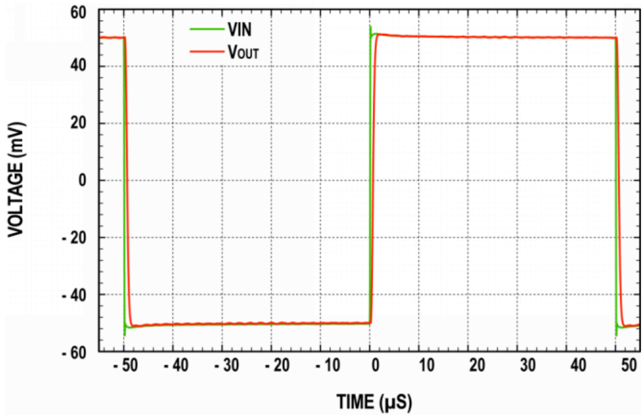


Figure 16. Small Signal Response (G = 1, R_L = 2 kΩ, C_L = 100 pF)

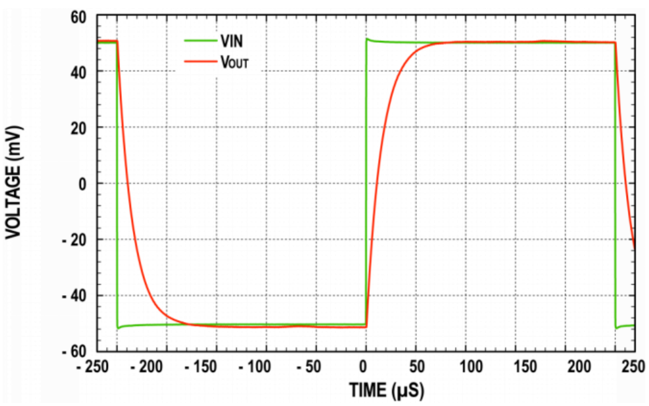


Figure 17. Small Signal Response (G = 1000, R_L = 2 kΩ, C_L = 100 pF)

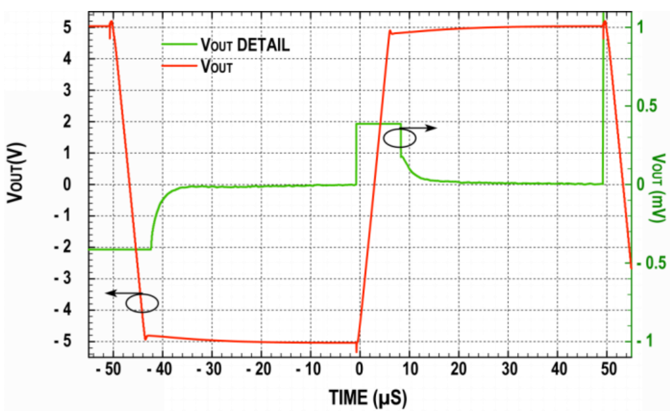


Figure 18. Large Signal Response and Settling Time, G = 1
(0.5 mV = 0.01%)

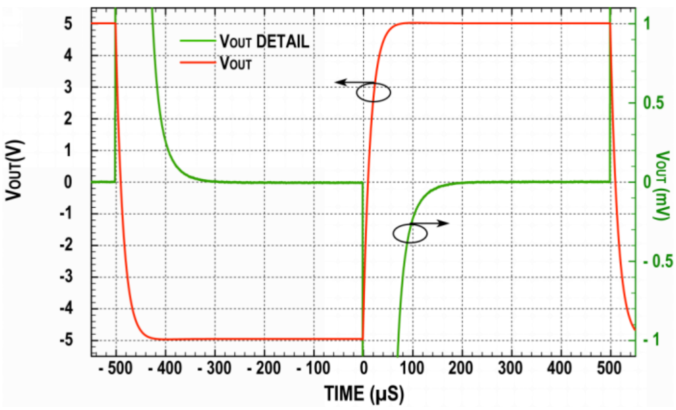


Figure 19. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

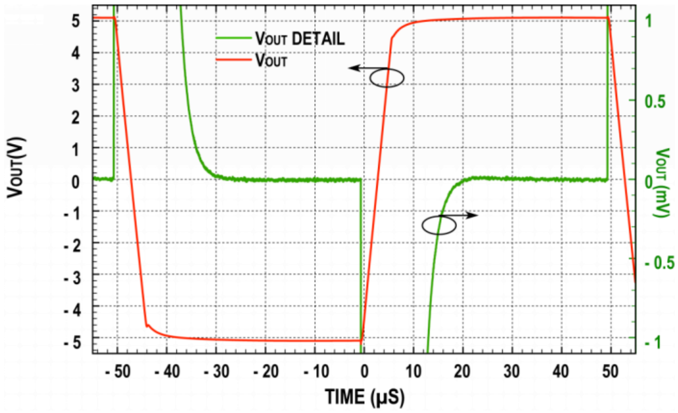


Figure 20. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

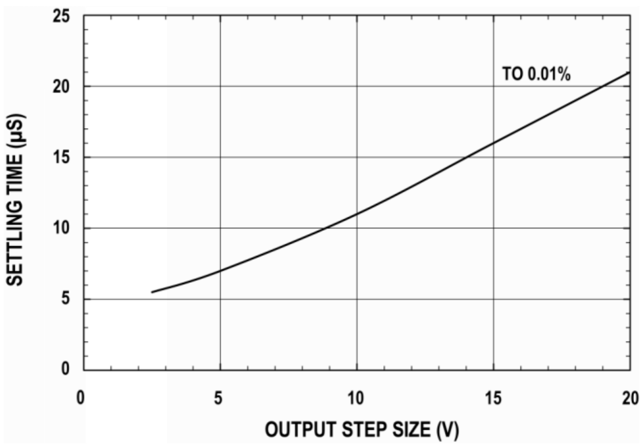


Figure 21. Settling Time vs. Step Size (G = 1)

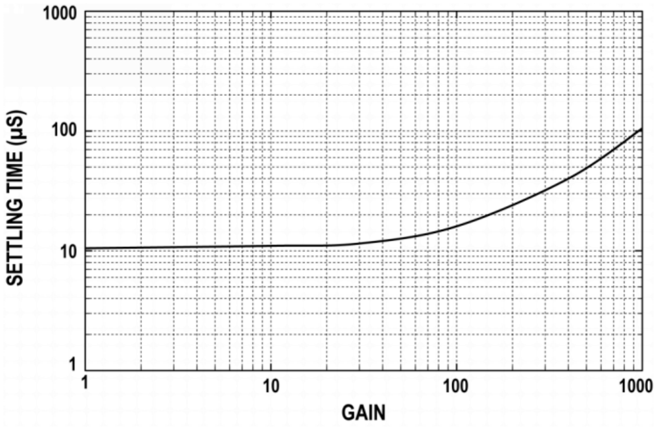


Figure 22. Settling Time to 0.01% vs. Gain, for a 10 V Step

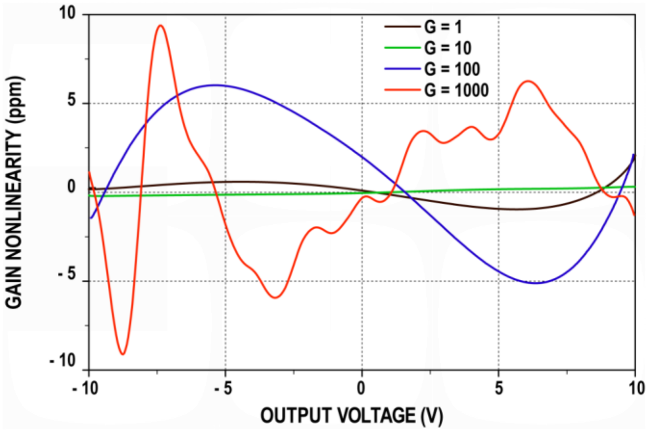


Figure 23. Gain Nonlinearity (R_L = 10 kΩ)

Theory of Operation

The ZJA3620 is manufactured in a high-performance bipolar process and its simplified schematic is shown below.

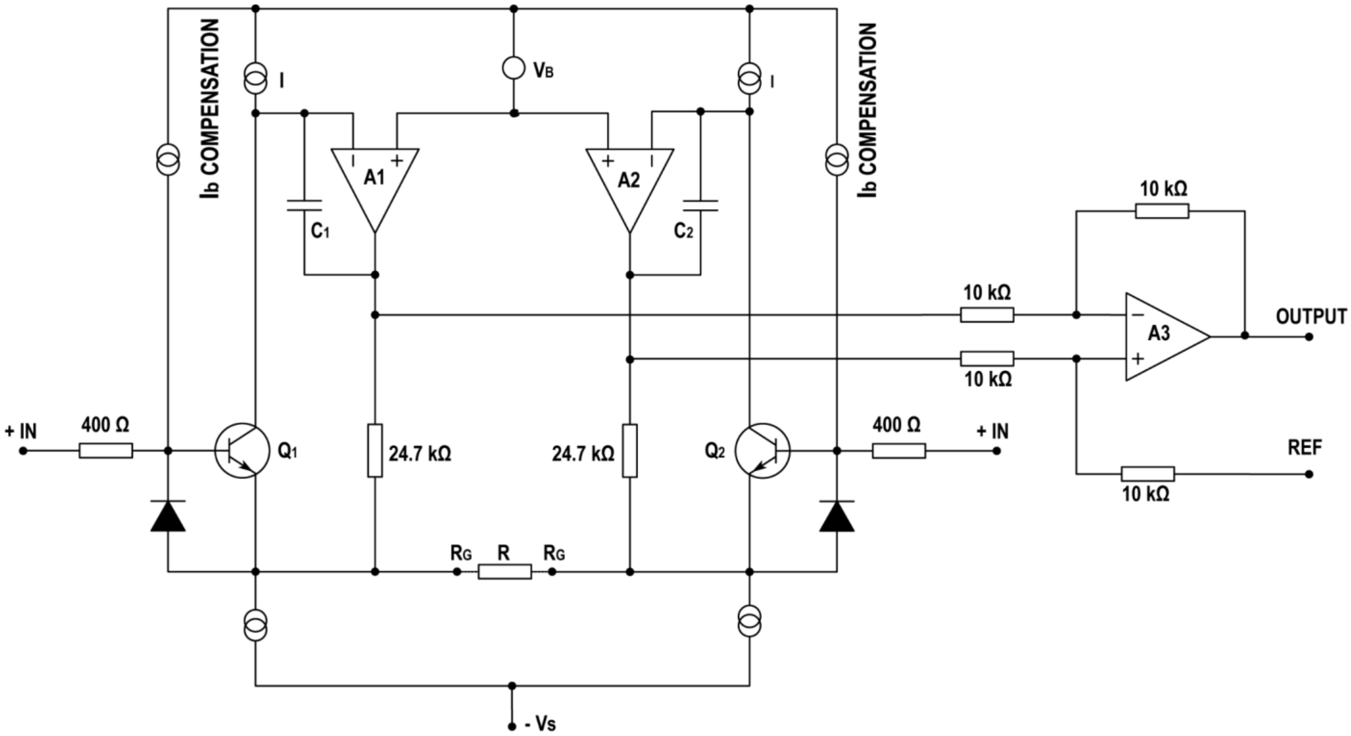


Figure 24. Simplified Schematic of ZJA3620

The ZJA3620 is a monolithic instrumentation amplifier based on the classic three op-amp approach. It allows the user to program gain accurately with only one resistor. Monolithic construction and laser wafer trimming allow tight matching and tracking of circuit components, thus ensuring high-level performance.

Input transistors Q_1 and Q_2 provide a single differential-pair bipolar input for high precision and offer 2 nA maximum input bias current using Superßeta technology. A1 and A2 are the input stage amplifiers with high input impedance, low noise, and low temperature drift. The internal gain resistors, R_1 and R_2, are trimmed to an absolute value of 24.7 kΩ, allowing accurate gain programming with a single external resistor R_G. The accuracy of R_1 and R_2 is key to user's gain accuracy and drift.

The input voltage noise is reduced to 6.5 nV/$\sqrt{\text{Hz}}$.

The unity-gain subtractor, A3, removes any common-mode signal, yielding a single-ended output referenced to the REF pin potential. The four 10 kΩ resistors are laser-trimmed for high CMRR.

The gain equation is the same as industry-standard parts.

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

Application Information

Gain Selection

Placing a resistor across the R_G terminals set the gain of ZJA3620, which can be calculated by referring to Table 1 or by using the gain equation.

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

1% Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

0.1% Standard Table Value of R_G (Ω)	Calculated Gain
49.3 k	2.002
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.01 k	49.91
499	100.0
249	199.4
98.8	501.0
49.3	1003

Table 1. Commonly-Used Gains and Resistor Values

The ZJA3620 defaults to G = 1 when no gain resistor is used. Gain accuracy is determined by the absolute tolerance of R_G. The TC of the external gain resistor increases the gain drift of the instrumentation amplifier. To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance. Gain error and gain drift are kept to a minimum when the gain resistor is not used.

Offset Voltage

The offset voltage of the ZJA3620 is attributed to two sources, input offset voltage V_{OSI} and output offset voltage V_{OSO}. The V_{OSO} is divided by G when referred to the input. In practice, the V_{OSI} dominates at high gains, and the V_{OSO} dominates at low gains. V_{OSI} includes the offset voltage generated by input amplifiers A1 and A2; V_{OSO} is the offset voltage of amplifier A3. The total V_{OS} for a given gain is calculated as

$$\text{Total Error RTI } (V_{OS,RTI}) = V_{OSI} + \frac{V_{OSO}}{G}$$

$$\text{Total Error RTO } (V_{OS,RTO}) = G * V_{OSI} + V_{OSO}$$

Reference Terminal

The reference terminal REF defines the zero-output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It can interface with pseudo-differential input ADCs easily, for example, ZJC2002 (pseudo-differential unipolar) and ZJC2003 (pseudo-differential bipolar).

The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 2 V. And as shown in Figure 24, it connects to one terminal of the trimmed 10 kΩ resistor. For best performance, source impedance to the REF terminal should be kept low, because parasitic resistance can adversely affect CMRR and gain accuracy. If the REF terminal is not connected to a clean and low-impedance system ground, it is generally recommended to add a precision op-amp buffer, such as ZJA3000-1, between the REF terminal and the signal source to obtain the best performance. This is how the typical applications in Figure 31 and Figure 32 are handled.

Input Protection

Instrumentation amplifiers like ZJA3620 is normally put in the very front of the system, thus its input protection is critical. The ZJA3620 features 400 Ω of series resistance at its inputs and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA (VIN/400 Ω). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an BAV99) will reduce the required resistance, yielding lower noise. Make sure short routing distance between the diodes and the input pins.

Input Bias Current Return Path

The input bias current of the ZJA3620 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 25 and Figure 26.

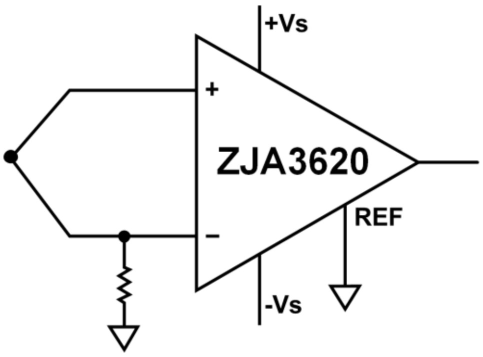


Figure 25. ZJA3620 Interfaces with Thermocouple

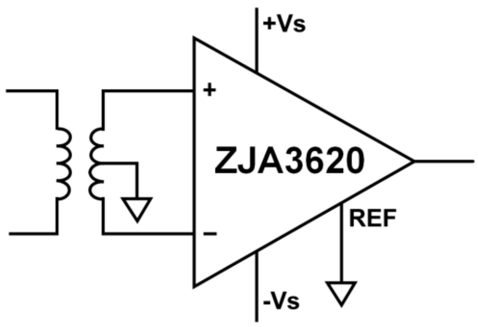


Figure 26. ZJA3620 Interfaces with Transformer

When using ZJA3620 for AC coupling, it is important to provide a return path to the input AC coupling capacitors. Otherwise, the input offset voltage will accumulate due to parasitic leakage and input currents, potentially causing the output to lock to a fixed voltage near the power rail. Figure 27 shows the correct connection for AC coupling, which utilizes a high-pass filter with a cutoff frequency determined by RC. And due to the differential inputs, the matching of R and C is crucial.

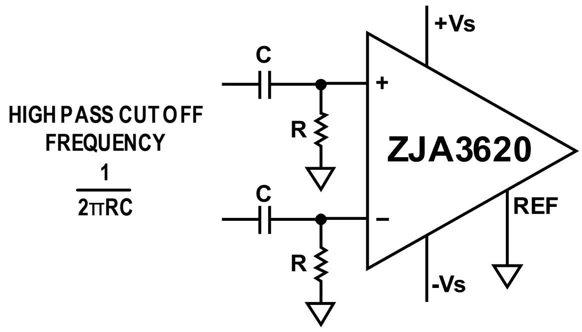


Figure 27. ZJA3620 in AC Coupling Connection

Power Supply Regulation and Bypassing

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. Bypass capacitors should be used to decouple the amplifier.

A low ESR 0.1 μF capacitor should be placed close to each supply pin. High-quality surface-mount ceramic capacitors (such as X5R or X7R) are recommended. As shown in Figure 28, a 10 μF tantalum capacitor can be used, and in most cases, it can be shared by other precision integrated circuits. Refer to the Layout Example section for specific layout examples.

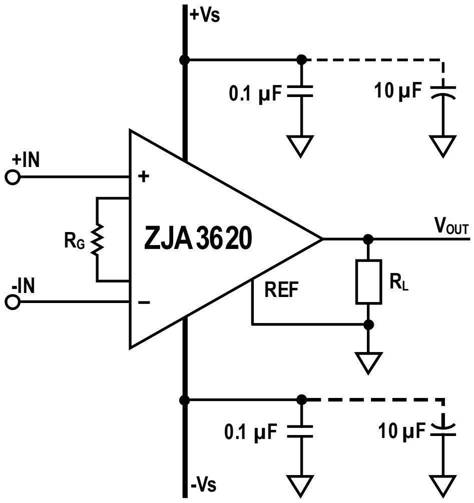


Figure 28. Supply Decoupling, REF and Output Referred to Local Ground

Although the ZJA3620 is a very reliable chip with certain protection functions, it is generally recommended to power on the ZJA3620 before applying the input signals.

Grounding

Star grounding is recommended for the ZJA3620 circuit, as shown in Figure 28. Maintain low impedance for the REF pin because the output voltage of the ZJA3620 is developed with respect to the potential on the REF. Place the decoupling capacitors as close to the power pins as possible to minimize the loop area.

In a multilayer PCB, use a large area ground plane if possible. Place analog signals on the layer above the ground plane.

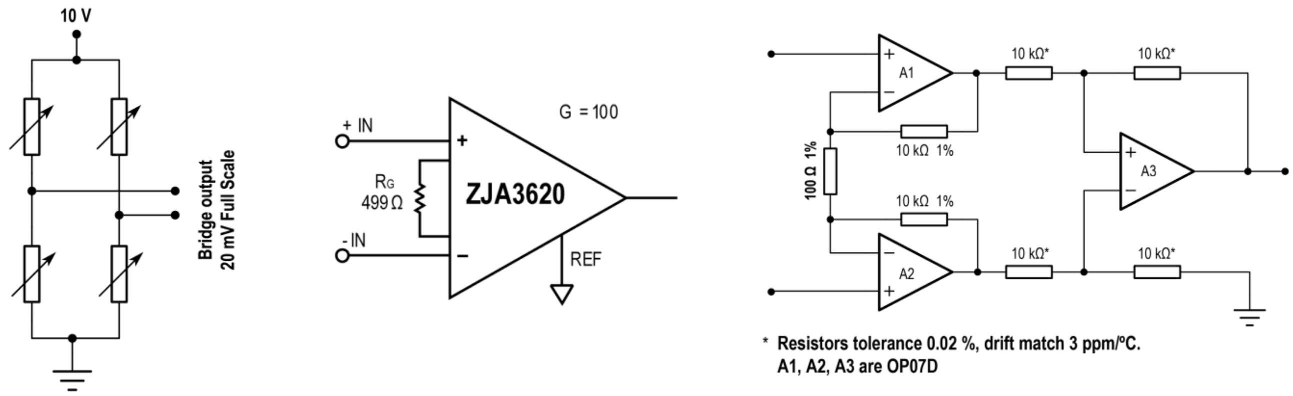
In mixed-signal environments, low level analog signals need to be isolated from the noisy digital environment. Modern precision SAR ADCs have separate analog and digital ground, and they are all connected to the analog ground. When used with this type of ADC, the ZJA3620 uses the analog ground as the reference.

The ZJA3620 has a low bias current. To reduce leakage current, it is recommended to remove the ground plane below the signal traces of the two inputs.

Make vs. Buy: A Typical Bridge Application Error Budget

The ZJA3620 offers improved performance over “homebrew” three op amp IA designs, along with smaller size, fewer components, and lower supply current. In the typical application, shown in Figure 29, a gain of 100 is required to amplify a bridge output of 20 mV full-scale over the industrial temperature range of -40 °C to +85 °C. Table 2 shows how to calculate the effect various error sources have on circuit accuracy. Regardless of the system in which it is being used, the ZJA3620 provides greater accuracy at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, leaving only the resolution errors of gain, nonlinearity, and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07D specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three-op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.



A Bridge sensor B ZJA3620 Monolithic Solution, G = 100 C "Homebrew" Solution, G = 100

Figure 29. Make vs. Buy ZJA3620

Error Source	ZJA3620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale	
			ZJA3620	Homebrew
Absolute accuracy at 25 °C				
Input Offset Voltage	125 µV / 20 mV	(150 µV*$\sqrt{2}$) / 20 mV	6,250	10,607
Output Offset Voltage	1,500 µV / 100 / 20 mV	(150 µV*2) / 100 / 20 mV	750	150
Input Bias Current	2 nA * 350 Ω / 20 mV	6 nA * 350 Ω / 20 mV	35	105
CMRR	108 dB (3.98 ppm) * 5 V / 20 mV	0.02% Match * 5 V / 20 mV / 100	995	500
Gain Error	0.375%	1%	3,750	10,000
Total Absolute Error at 25 °C			11,780	21,362
Drift to 85 °C				
Gain Drift	50 ppm/°C * 60 °C	100 ppm/°C Track * 60 °C	3,000	6,000
V_{OSI} Drift	1 µV/°C * 60 °C / 20 mV	2.5 µV/°C *$\sqrt{2}$ * 60 °C / 20 mV	3,000	10,607
V_{OSO} Drift	15 µV / °C * 60 °C / 100 / 20 mV	2.5 µV/°C * 2 * 6 0 °C / 100 / 20 mV	450	150
Total Drift Error			6,450	16,757
Resolution				
Gain nonlinearity	40 ppm	40 ppm	40	40
Noise (0.1-10 Hz)	0.2 µV_{P-P} / 20 mV	(0.38 µV_{P-P} *$\sqrt{2}$) / 20 mV	10	27
Total Resolution Error			50	67
Grand Total Error			18,280	38,186
Total Unadjusted Error			6,500	16,824

Table 2. Mak vs Buy ZJA3620 Error Budget

ZJA3620 Comparison to Zero-drift Instrumentation Amplifiers

The ZJA3620 is a continuous-signal processing instrumentation amplifier, unlike chopping/auto-zero-based zero-drift amplifiers reliant on non-continuous switch-based technology. These amplifiers contain a sampling capacitor at the input, causing the input bias current to exhibit periodic glitches invisible in datasheets due to averaging. Eliminating these glitches requires an output filter, significantly limiting their usable bandwidth and often restricting them to DC and near-DC signals. Adding a filter also adds complexity to system design. Additionally, tolerance of their internal sampling capacitors leads to variations in glitch amplitude across different ICs. More critically, their linearity (THD & THD+N) is often not great. While they may boast better low-frequency noise, this comes at the cost of transferring noise to the switching frequency, resulting in a noisy spectrum with large spike components. Consequently, their overall noise performance is often inferior to high-performance continuous sampling amplifiers like the ZJA3620.

Furthermore, the usable bandwidth of zero-drift amplifiers is typically only 1/10 or 1/100 of what their datasheets suggest, severely limiting their usability. Their settling time and overload recovery time are also often much longer, making them unsuitable for multi-channel switching or applications with dynamic performance requirements.

Applications and Implementation

Bridge Circuit Interface

Bridge circuits are widely used in various sensing systems. Figure 30 shows how the ZJA3620 interfaces with a bridge circuit, enabling its integration into a data acquisition system (DAS). Bridge circuits have different designs depending on the parameters being measured (excitation voltage Vexc, resistance Rb, and sensitivity, etc.), resulting in different electrical characteristics. The excitation voltage and resistance have the greatest impact on the interface circuit. As a general-purpose differential-to-single-ended input device, the instrumentation amplifier is very suitable for the interface of bridge circuit sensors. The excitation voltage determines the input common-mode voltage of the instrumentation amplifier as Vexc/2. It is necessary to pay attention to the supply voltage of the instrumentation amplifier to ensure that Vexc/2 is within the allowable input range. The wide supply voltage of ZJA3620 provides flexibility in use, and its excellent common-mode rejection ratio (CMRR) and guaranteed temperature characteristics ensure the accuracy of the circuit over the entire temperature range, simplifying system design. The resistance Rb has a significant impact on the instrumentation amplifier, and it is generally required that the instrumentation amplifier has high input impedance and low voltage noise. If Rb is higher than 100 kΩ, users need to carefully check the bias current and current noise of the instrumentation amplifier. The ZJA3620's bias current is within 2 nA and current noise is 100 fA $/\sqrt{Hz}$ at room temperature, making it ideal to interface with high-output impedance bridge circuits and ensuring system SNR (signal-to-noise ratio) and resolution.

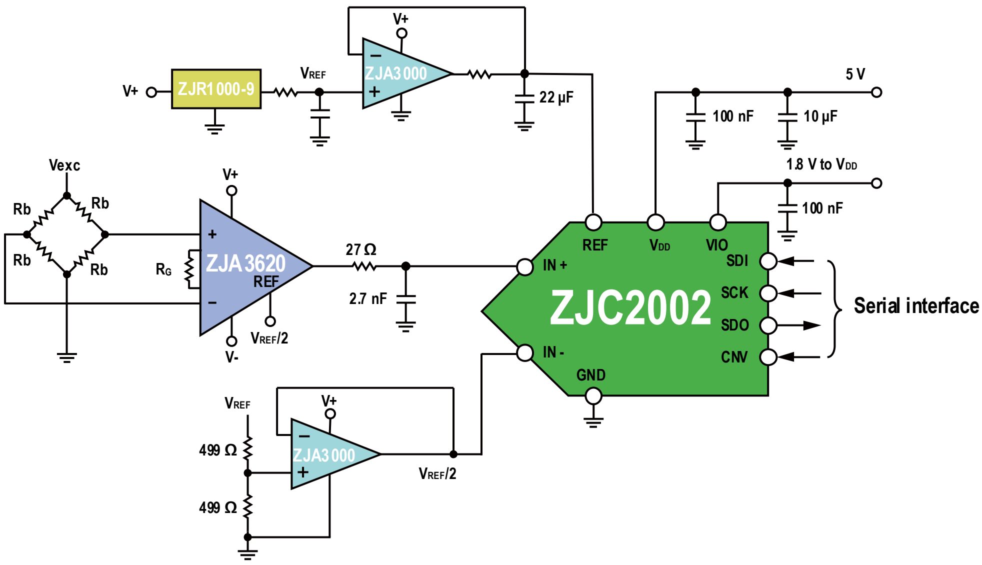


Figure 30. ZJA3620 Interfaces with Bridge Circuit

Building Precision Current Source with ZJA3620

Figure 31 illustrates the construction of a precision current source using a single ZJA3620 instrumentation amplifier, one ZJA3000-1 precision operational amplifier, and two resistors. This design offers flexibility with a supply voltage range of ±2.4 V to ±18 V. The ZJA3620's characteristics simplify setting the circuit's current output. The actual current output is equal to the set value minus the input bias current of the ZJA3000, which is within 25 pA at room temperature, making it often negligible.

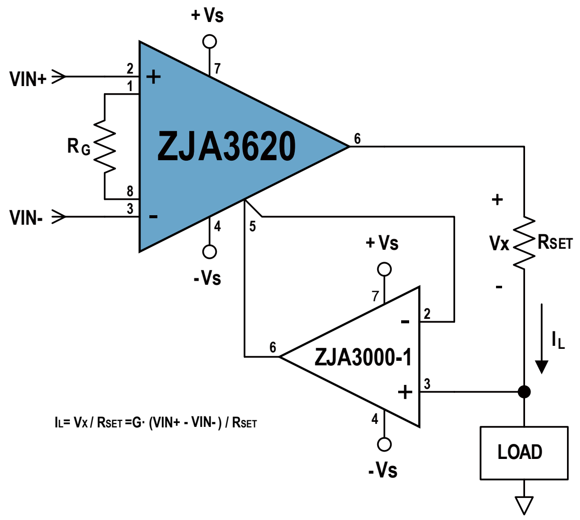


Figure 31. Building Precision Current Source with ZJA3620

Precision Current Sensing

The ZJA3620 is often used for precision current sensing due to its high accuracy, wide bandwidth, low input bias current, and ease of use. As shown in Figure 32, the shunt resistor Rs is typically low, possibly a few Ohms, or even in the mΩ range. The ZJA3620's high input impedance and input bias current of 2 nA or less allow it to detect currents as low as 10 nA; its low-frequency noise of 0.2 $\mu V_{P\text{-}P}$ allows it to detect µV-level signals. The ZJA3620 has a wide input range, allowing it to accurately measure input signals with a large dynamic range from µV to several volts. In general, current changes rapidly, so the ZJA3620's wide bandwidth is very suitable. This is particularly beneficial in applications like motor control or battery monitoring, where current can fluctuate rapidly. On the other hand, the voltage Vm can be a high voltage varying at a certain frequency. In this case, the ZJA3620's high CMRR is critical for accuracy.

For applications that require long-term operation and large environmental temperature changes, the ZJA3620's long-term stability and temperature drift characteristics are very valuable, making the design simpler and more reliable.

In some applications, the signal dynamic range is too big, and the accuracy or linearity of the instrumentation amplifier must be sacrificed by changing R_G to meet the needs of measuring the entire dynamic range. In this case, using digital potentiometers (digi-POTs) is not a good solution, because their temperature characteristics are often not very good. Engineers may consider the series and parallel connection of precision resistors, utilizing relays with good temperature characteristics to switch between ranges. Attention should be paid to wiring in such configurations.

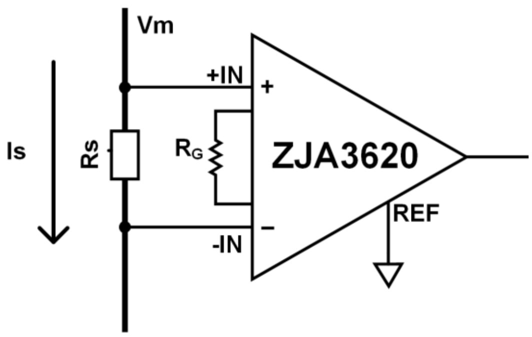


Figure 32. Using ZJA3620 for Precision Current Sensing

In precision current sensing, if a zero-drift instrumentation amplifier is used, the offset voltage caused by bias current glitch and high-frequency noise will limit the minimum detectable current, thereby limiting the detection accuracy. The available bandwidth of a zero-drift instrumentation amplifier is typically 1/10 to 1/100 of its data sheet bandwidth, which limits the available bandwidth of the current to be measured. This can often make it difficult to keep up with fast-changing currents, resulting in missed information or limiting the bandwidth of closed-loop systems. The longer settling time and lower slew rate of zero-drift instrumentation amplifiers will reduce the system's response speed. The poor linearity of zero-drift instrumentation amplifiers can make the design of control systems difficult or even impossible.

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible to minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

Layout Example

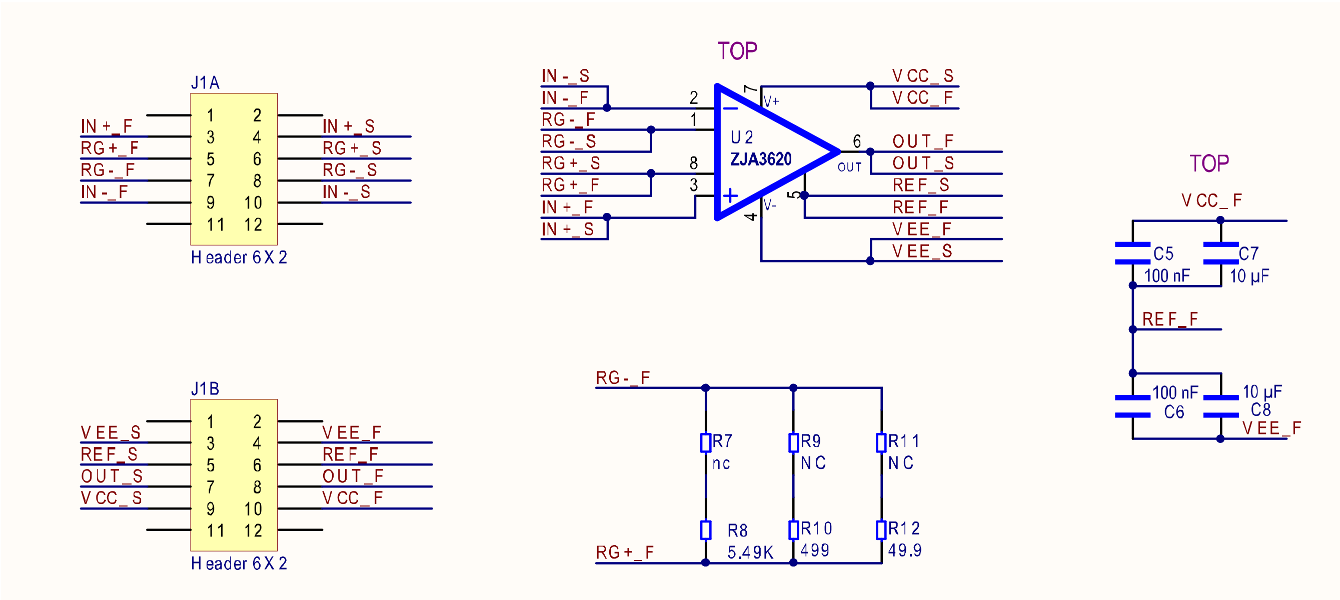


Figure 33. ZJA3620 Evaluation Board Schematic

During evaluation, a Kelvin connection, as shown in Figure 33, is typically not necessary. R7, R9, and R11 can be connected as needed, while R8, R10, and R12 can be selected based on the desired gain. In most cases, one of these paths is sufficient. For example, R7 could be set to 0 Ω, and R8 could be assigned the resistance value calculated for the desired gain.

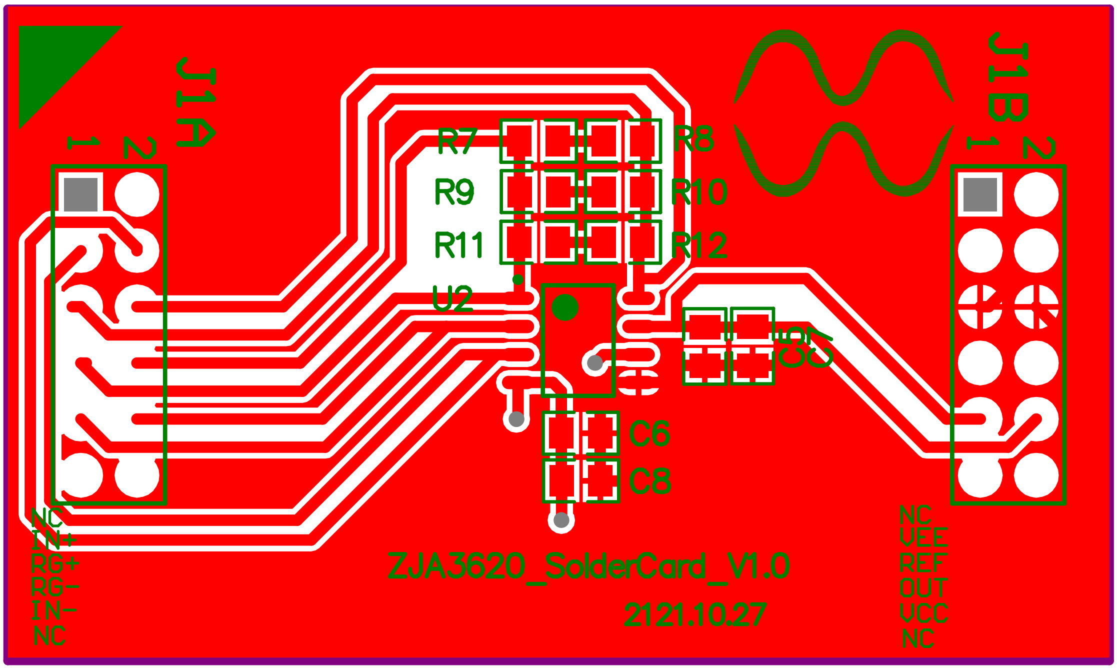


Figure 34. Layout of ZJA3620 Evaluation Board (Top Layer)

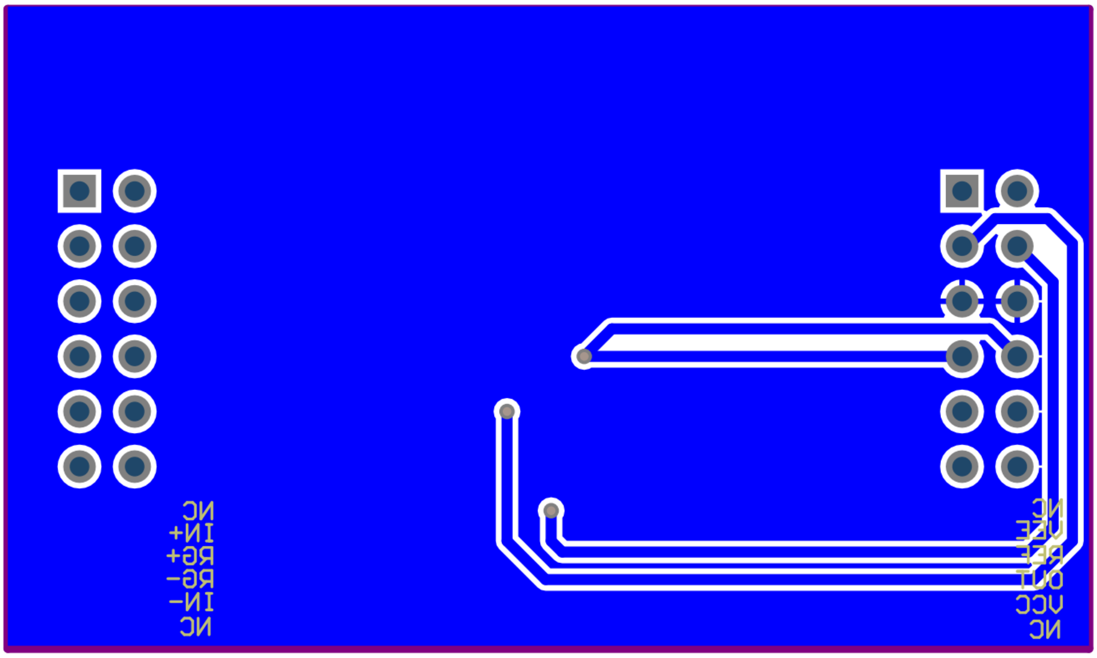


Figure 35. Layout of ZJA3620 Evaluation Board (Bottom Layer)

Outline Dimensions

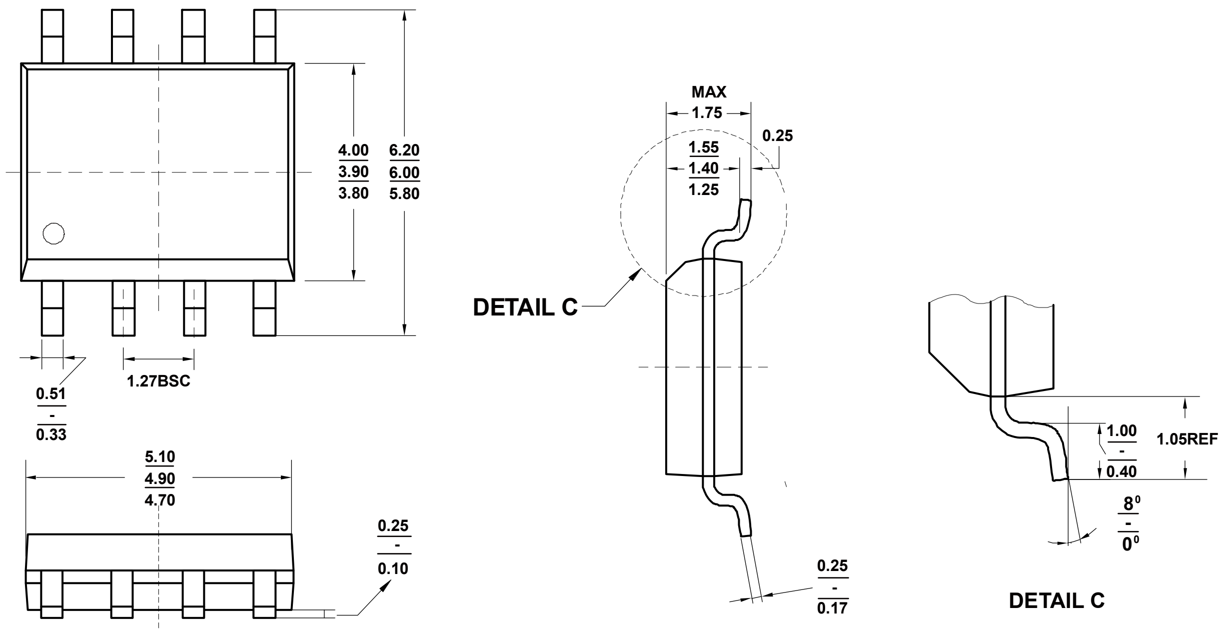


Figure 36. 8-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Status[1]	Temperature Range (°C)	Package	External Package
ZJA3620	ZJA3620ASAET	ACTIVE	-40 to 85	SOIC-8	Tube
	ZJA3620ASAER	ACTIVE	-40 to 85	SOIC-8	13” reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External package: T=Tube; R=Reel
- Temperature range: A=-40°C to 125°C Automotive Grade 1; B=-40°C to 125°C; E=-40°C to 85°C
- Number of pins: R=3; K=5; T=6, A=8; B=10; D=14; E=16; P=20
- Package type: S=SOIC; U=MSOP, TSSOP, SOT (3 to 6 pins); T=DFN, QFN; K=SOT (8 pins)
- Grade: B grade is better than A grade
- Base: R=Voltage reference; A=Amplifier; C=Data Converter; G=Switches and Multiplexers, M=Others

[1] The marketing status values are defined as follows:
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
ACTIVE: Product device recommended for new designs.
NRND: Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.
LIFEBUY: ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.
OBSOLETE: ZJW has discontinued the production of the device.

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91. 7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 μV max Vos, 0.5 μV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 μV max Vos, 0.5 μV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/μS, 50 μV max Vos, 1 μV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3217/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 μV max Vos, 1 μV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 μV max Vosi, ±2.4 V to ±18 V, -40°C to 125°C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 μV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 μV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 μA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/μS, 50 nS to 16-bit, 50 μV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 μV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 μV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 μA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω,14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV