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CAT5115

32-tap Digital Potentiometer (POT)

Description

The CAT5115 is a single digital POT designed as an electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5115 contains a 32-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_W. The wiper is always set to the mid point, tap 15 at power up. The tap position is not stored in memory. Wiper-control of the CAT5115 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device.

The digital POT can be used as a three-terminal resistive divider or as a two-terminal variable resistor. Digital POTs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

For a pin-compatible device that recalls a stored tap position on power-up refer to the CAT5114 data sheet.

Features

- 32-position Linear Taper Potentiometer
- Low Power CMOS Technology
- Single Supply Operation: 2.5 V – 6.0 V
- Increment Up/Down Serial Interface
- Resistance Values: 10 kΩ, 50 kΩ and 100 kΩ
- Available in PDIP, SOIC, TSSOP, MSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper-proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions

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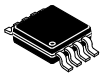
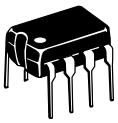
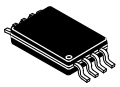
SOIC–8
V SUFFIX
CASE 751BD



MSOP–8
Z SUFFIX
CASE 846AD

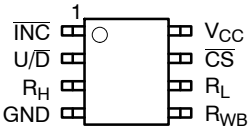


PDIP–8
L SUFFIX
CASE 646AA



TSSOP–8
Y SUFFIX
CASE 948AL

PIN CONFIGURATIONS



PDIP (L), SOIC (V), MSOP (Z)

TSSOP (Y)

(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Functional Diagram

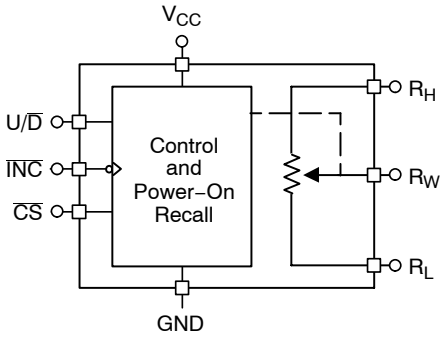


Figure 1. General

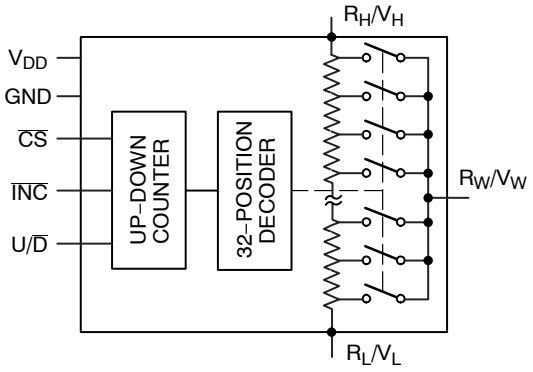


Figure 2. Detailed

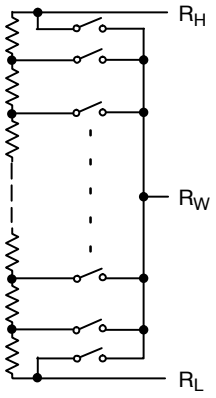


Figure 3. Electronic Potentiometer Implementation

Table 1. PIN DESCRIPTIONS

Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_W	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

Pin Function

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_W: Wiper Potentiometer Terminal

R_W is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. Voltage applied to the R_W terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5115 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

Device Operation

The CAT5115 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_W equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points, R_H and R_L. There are 31 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position.

With $\overline{CS}$ set LOW the CAT5115 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. When the CAT5115 is powered-down, the wiper position is reset. When power is restored, the counter is set to the mid point, tap 15.

Table 2. OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

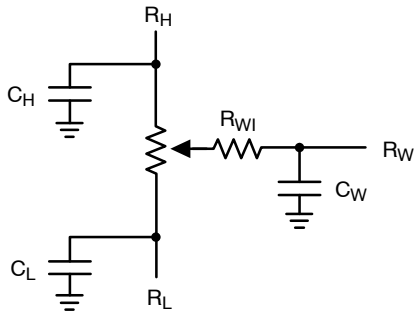


Figure 4. Potentiometer Equivalent Circuit

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V_{CC} to GND	−0.5 to +7	V
Inputs $\overline{CS}$ to GND	−0.5 to V_{CC} +0.5	V
$\overline{INC}$ to GND	−0.5 to V_{CC} +0.5	V
U/$\overline{D}$ to GND	−0.5 to V_{CC} +0.5	V
H to GND	−0.5 to V_{CC} +0.5	V
L to GND	−0.5 to V_{CC} +0.5	V
W to GND	−0.5 to V_{CC} +0.5	V
Operating Ambient Temperature Industrial ('I' suffix)	−40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	−65 to 150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP} (Note 1)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2000			V
I_{LTH} (Notes 1, 2)	Latch-up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL−STD−883, Test Method 1008	100			Years
N_{END}	Endurance	MIL−STD−883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} + 1 V.

Table 5. DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V to +6 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.5	–	6.0	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6 V, f = 1 MHz, I_W = 0	–	–	100	μA
		V_{CC} = 6 V, f = 250 kHz, I_W = 0	–	–	50	μA
I_{SB1} (Note 4)	Supply Current (Standby)	$\overline{CS}$ = V_{CC} – 0.3 V U/$\overline{D}$, $\overline{INC}$ = V_{CC} – 0.3 V or GND	–	0.01	1	μA
LOGIC INPUTS						
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	–	–	10	μA
I_{IL}	Input Leakage Current	V_{IN} = 0 V	–	–	–10	μA
V_{IH1}	TTL High Level Input Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V	2	–	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	–	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5 V ≤ V_{CC} ≤ 6 V	V_{CC} x 0.7	–	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		–0.3	–	V_{CC} x 0.2	V
POTENTIOMETER CHARACTERISTICS						
R_{POT}	Potentiometer Resistance	–10 Device		10		kΩ
		–50 Device		50		
		–00 Device		100		
	Pot. Resistance Tolerance				±20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			3.2		%
INL	Integral Linearity Error	I_W ≤ 2 μA		0.5	1	LSB
DNL	Differential Linearity Error	I_W ≤ 2 μA		0.25	0.5	LSB
R_{WI}	Wiper Resistance	V_{CC} = 5 V, I_W = 1 mA		70	200	Ω
		V_{CC} = 2.5 V, I_W = 1 mA		150	400	Ω
I_W	Wiper Current	(1)			1	mA
TC_{RPOT}	TC of Pot Resistance			±50	±300	ppm/°C
TC_{RATIO}	Ratiometric TC				20	ppm/°C
V_N	Noise	100 kHz / 1 kHz		8/24		nV/√Hz
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 kΩ		1.7		MHz

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V.
5. I_W = source or sink.
6. These parameters are periodically sampled and are not 100% tested.

Table 6. AC TEST CONDITIONS

V_{CC} Range	2.5 V ≤ V_{CC} ≤ 6.0 V
Input Pulse Levels	0.2 x V_{CC} to 0.7 x V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 x V_{CC}

Table 7. AC OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, V_H = V_{CC}, V_L = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100	–	–	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	–	–	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	–	–	ns
t_{IL}	$\overline{INC}$ LOW Period	250	–	–	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	–	–	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	–	–	μs
t_{CPH}	$\overline{CS}$ Deselect Time	100	–	–	ns
t_{IW}	$\overline{INC}$ to V_{OUT} Change	–	1	5	μs
t_{CYC}	$\overline{INC}$ Cycle Time	1	–	–	μs
t_R, t_F (Note 8)	$\overline{INC}$ Input Rise and Fall Time	–	–	500	μs
t_{PU} (Note 8)	Power-up to Wiper Stable	–	–	1	ms

7. Typical values are for T_A = 25°C and nominal supply voltage.
8. This parameter is periodically sampled and not 100% tested.
9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

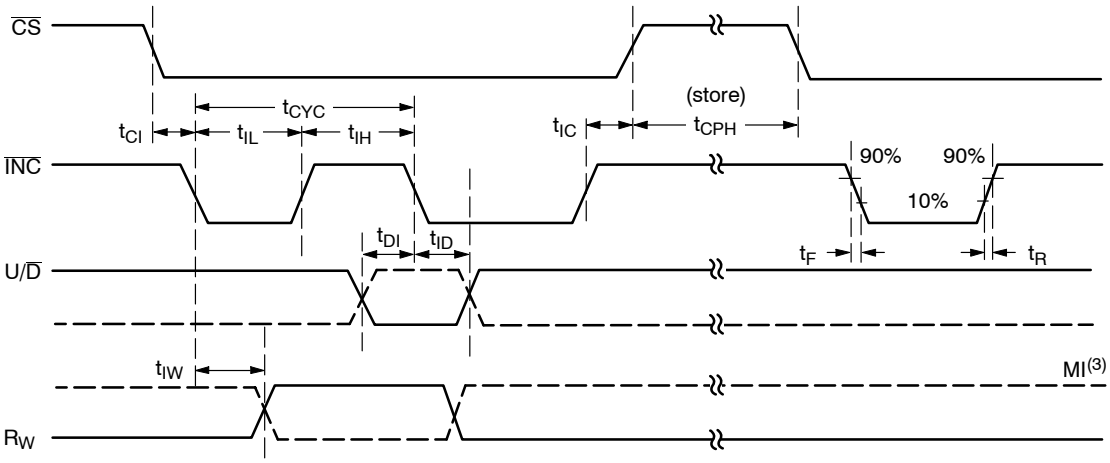


Figure 5. A.C. Timing

APPLICATIONS INFORMATION

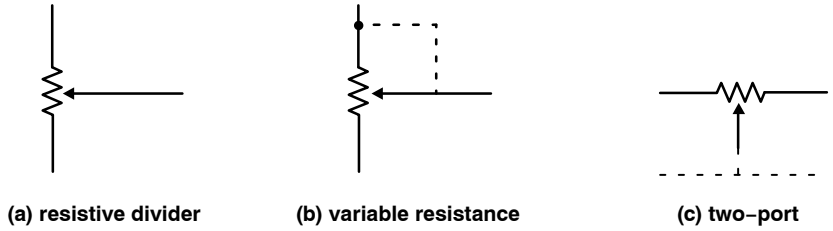


Figure 6. Potentiometer Configuration

Applications

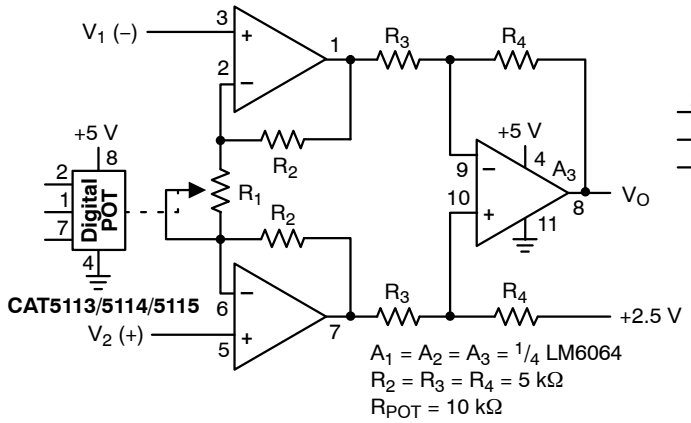


Figure 7. Programmable Instrumentation Amplifier

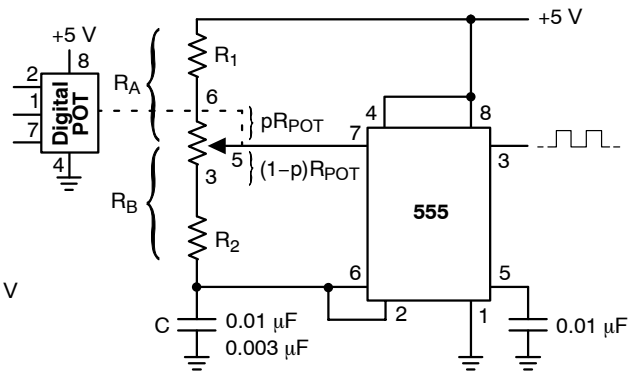


Figure 8. Programmable Sq. Wave Oscillator (555)

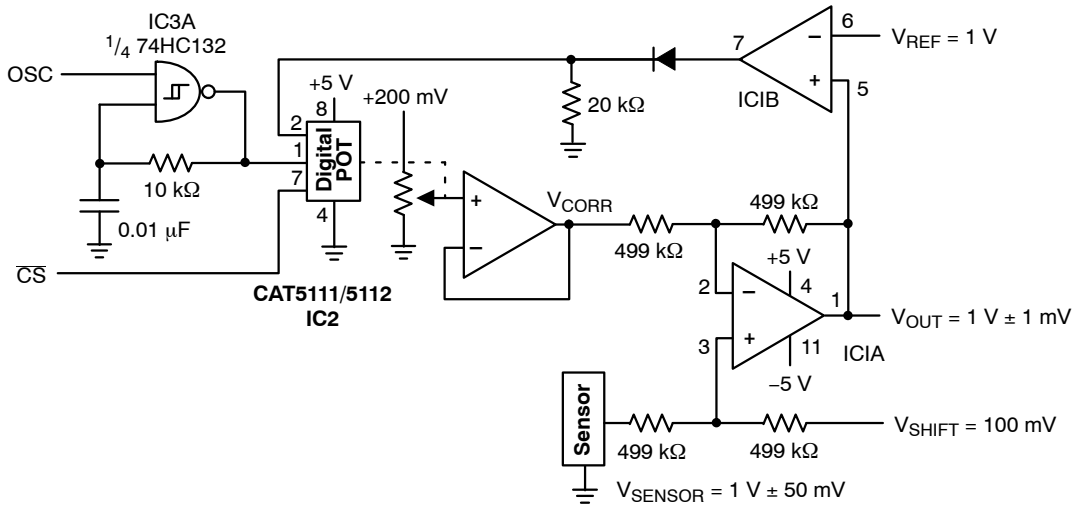


Figure 9. Sensor Auto Referencing Circuit

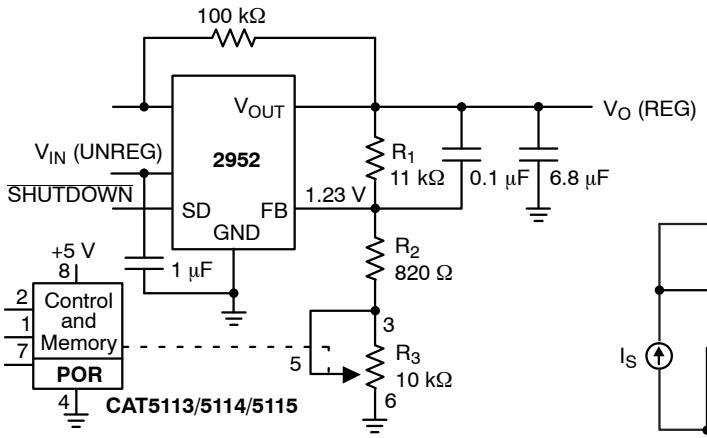


Figure 10. Programmable Voltage Regulator

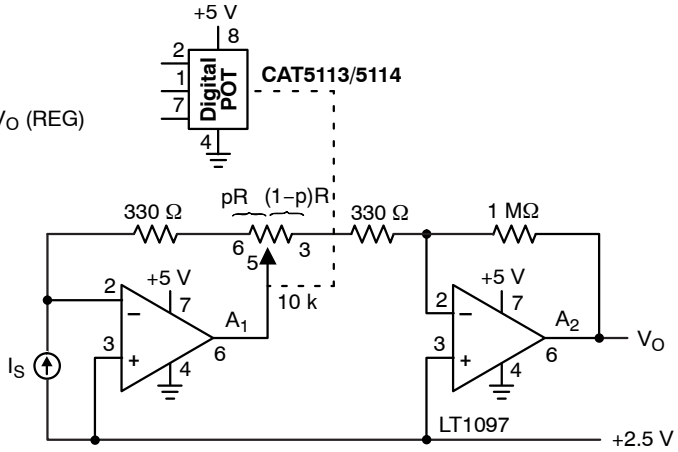


Figure 11. Programmable I to V Convertor

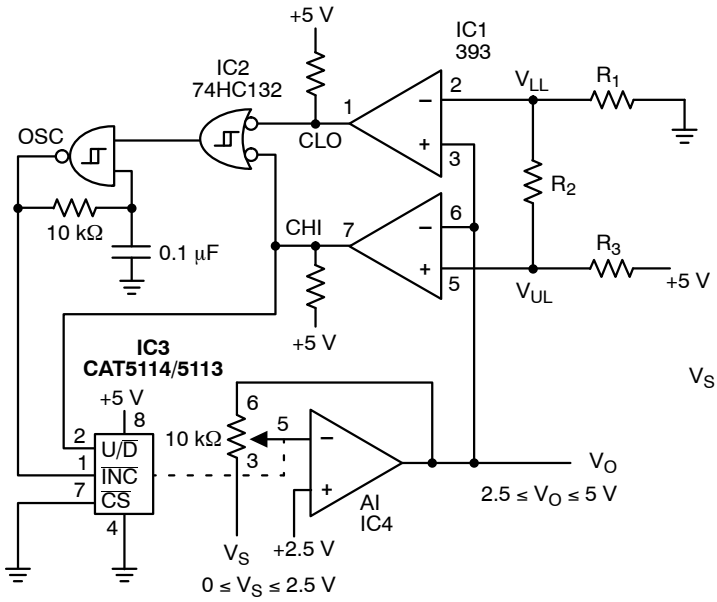


Figure 12. Automatic Gain Control

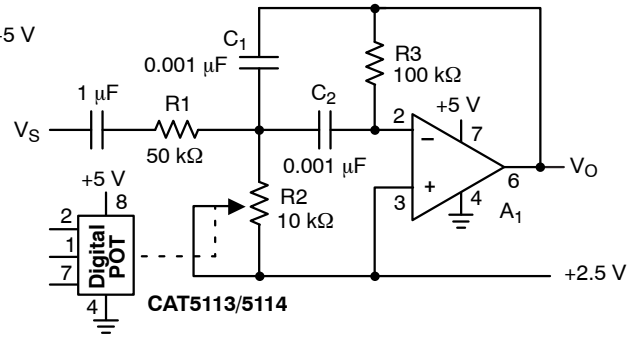


Figure 13. Programmable Bandpass Filter

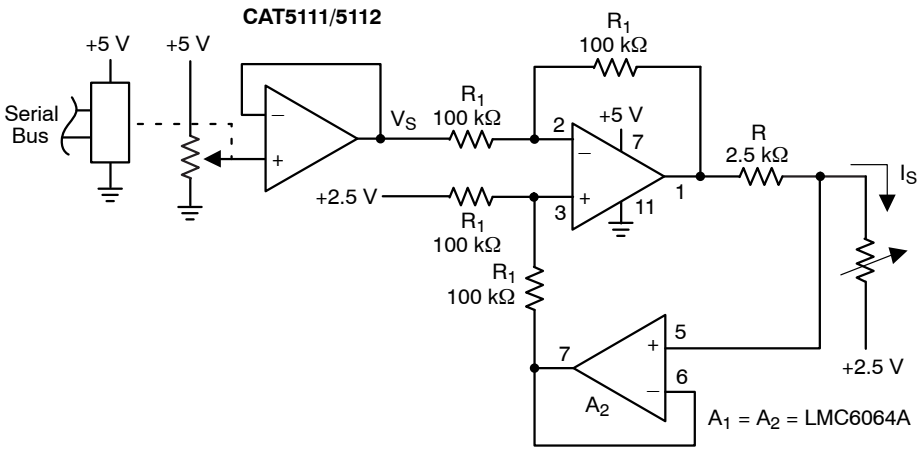


Figure 14. Programmable Current Source/Sink

Table 8. ORDERING INFORMATION

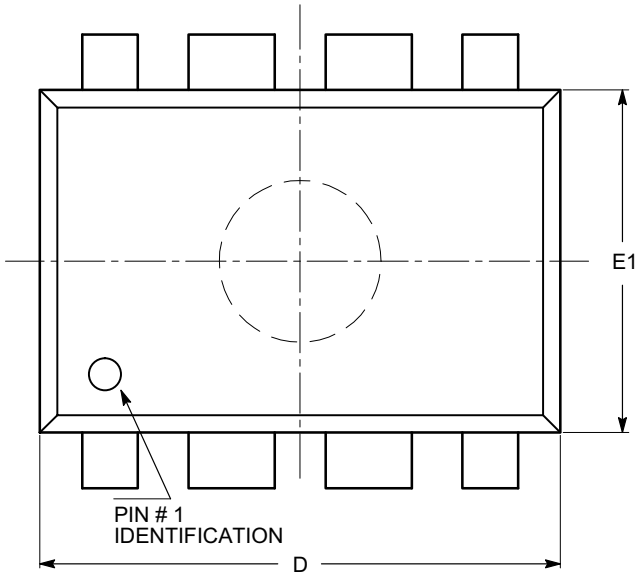
Orderable Part Numbers	Reset Threshold Voltage	Package−Pin	Lead Finish	Shipping†
CAT5115LI−10−G	10	PDIP−8	NiPdAu	50 Units / Tube
CAT5115LI−50−G	50			50 Units / Tube
CAT5115LI−00−G	100			50 Units / Tube
CAT5115VI−10−GT3	10	SOIC−8	NiPdAu	3000 / Tape & Reel
CAT5115VI−50−GT3	50			3000 / Tape & Reel
CAT5115VI−00−GT3	100			3000 / Tape & Reel
CAT5115YI−10−GT3	10	TSSOP−8	NiPdAu	3000 / Tape & Reel
CAT5115YI−50−GT3	50			3000 / Tape & Reel
CAT5115YI−00−GT3	100			3000 / Tape & Reel
CAT5115ZI−10−GT3	10	MSOP−8	NiPdAu	3000 / Tape & Reel
CAT5115ZI−50−GT3	50			3000 / Tape & Reel
CAT5115ZI−00−GT3	100			3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.
11. Contact factory for package availability.
12. All packages are RoHS-compliant (Lead-free, Halogen-free).
13. The standard lead finish is NiPdAu.
14. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

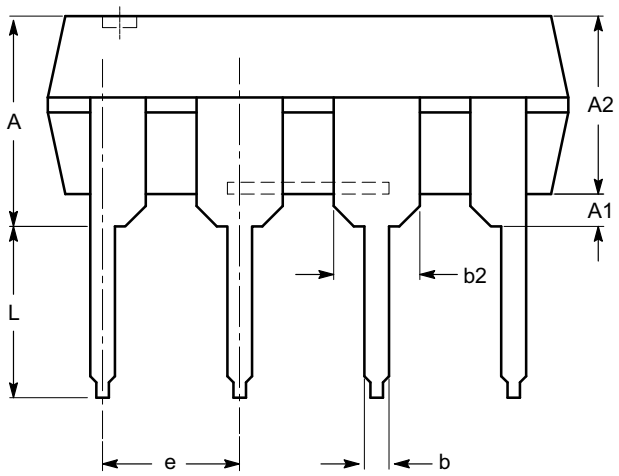
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA
ISSUE A

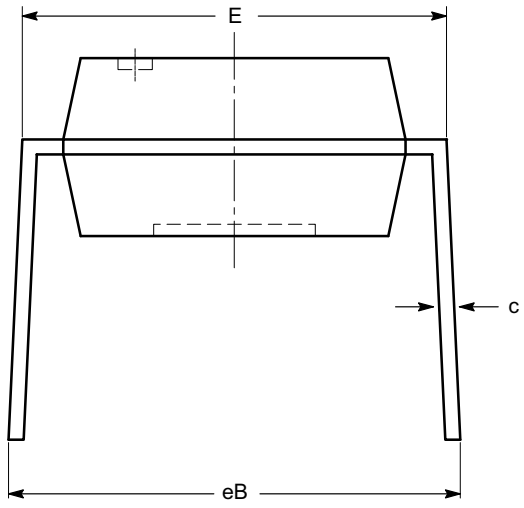


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

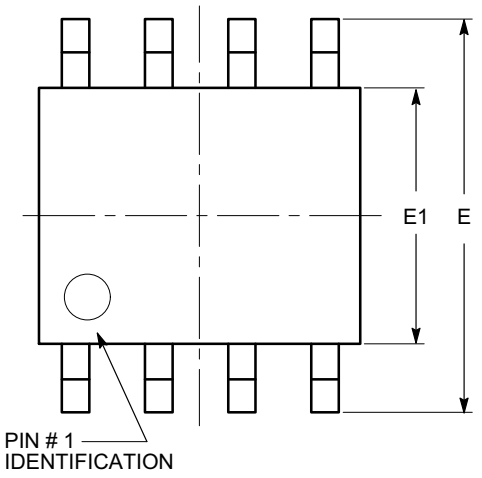


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

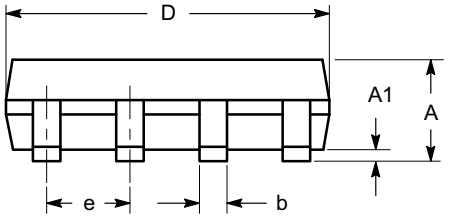
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD
ISSUE O

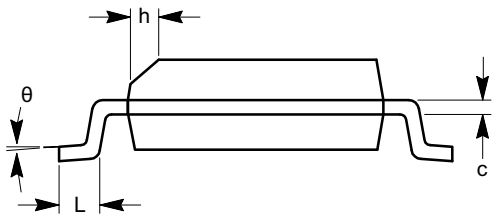


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

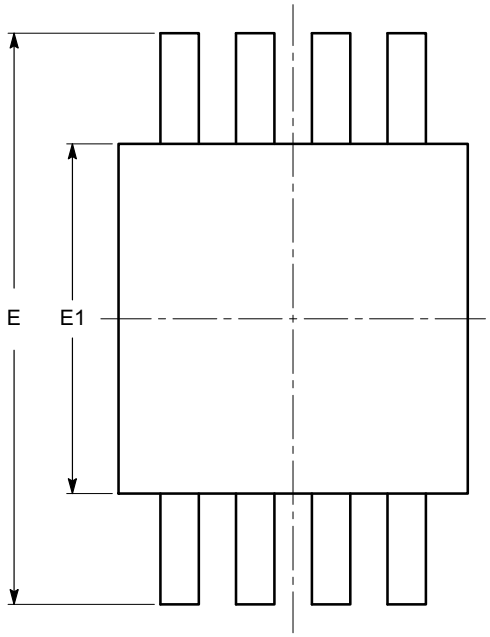


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

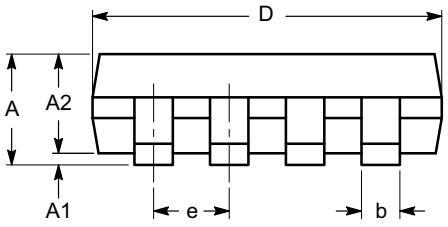
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD
ISSUE O

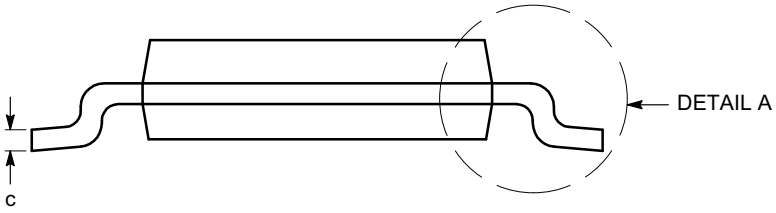


TOP VIEW

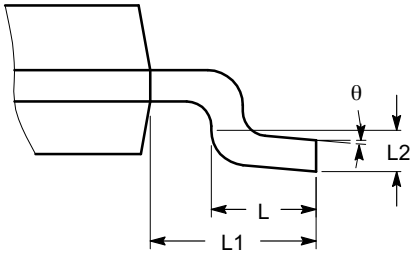
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW

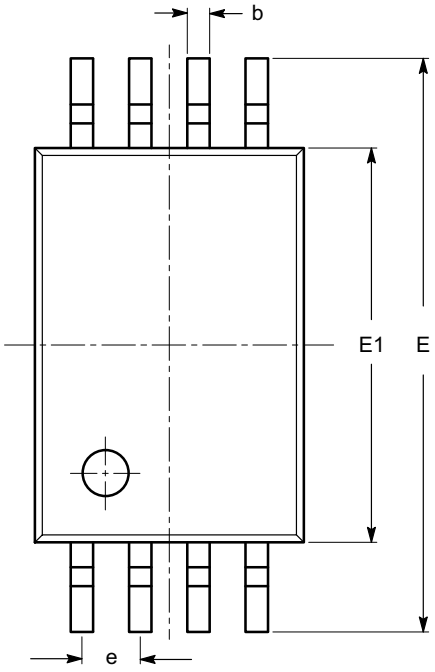


DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

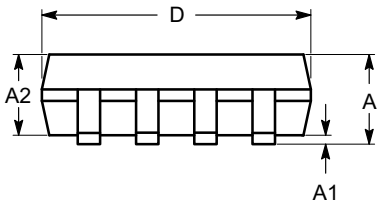
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL
ISSUE O

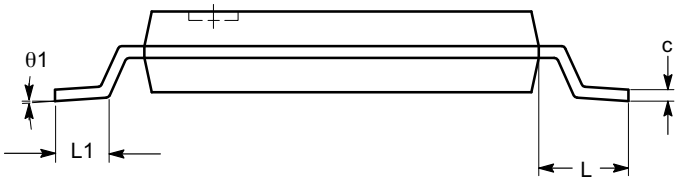


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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