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Nyfea product specification

PRODUCT SPECIFICATION

产品规格书

Customer 客户名称： _____

Product Name品名: Real Time Clock

PART NO. 型号规格: FRTC4111S

Issue Date发布日期: _____

Prepared 制作	Checked 审核	Customer Check客户核准
ChenTT	Zelig	

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Features

- Counters for seconds, minutes, hours, day, date, month, years and century
- 32 kHz crystal oscillator integrating load capacitance (12.5 pF) providing exceptional oscillator stability and high crystal series
- Serial interface supports I2C bus (400 kHz protocol)
- Ultra-low battery supply current of 0.4 μA (typ. at 3 V)
- 2.0 to 5.5 V clock operating voltage
- Automatic switchover and deselect circuitry
- 56 bytes of general purpose RAM
- Software clock calibration to compensate crystal deviation due to temperature
- Automatic leap year compensation
- Operating temperature of -40 to 85°C

Applications

- Portable instruments
- Electronic metering
- Battery powered products
- Telecom equipments

Description

The FRTC4111S is a low-power serial real-time clock (RTC) with 56 bytes of NVRAM. A built-in 32.768 kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary-coded decimal (BCD) ormat. Addresses and data are transferred serially via a two-line bidirectional bus. The built-in address register is incremented automatically after each write or read data byte.

The FRTC4111S clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium coin cell.

Typical data retention time is in excess of 5 years with a 50 mA/h, 3V lithium cell.

Ordering Information

Ordering Code	Package	Description
FRTC4111S	SOP8	pitch 1.27mm

Pb-free and Green

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Block Diagram

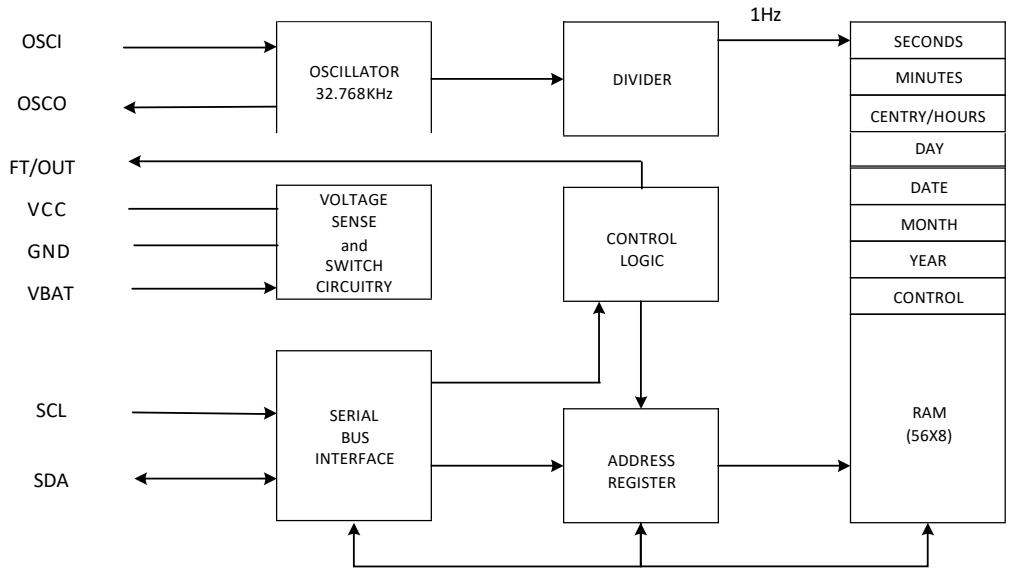

Figure 1. SOP8 Block Diagram

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Typical Application Circuit

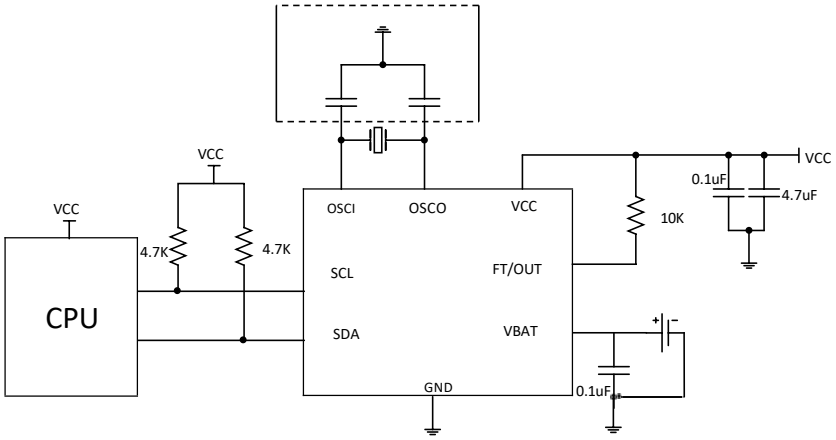

Figure 2. Typical Application Circuit

Notes:

1. FT/OUT open drain,need to add a pull resistor.
2. It is recommended to add 0.1uf capacitor to VBAT pin.

Pin Configuration

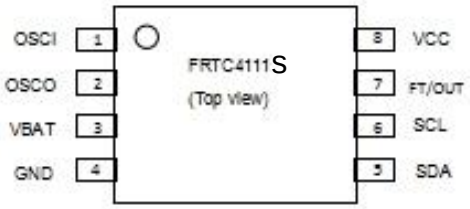

Figure 3. Pin Configuration

Pin Name	Pin No. SOP8	Type	Description
OSCI	1	Input	Oscillator input
OSCO	2	Output	Oscillator output
V_{BAT}	3	Power	Battery supply voltage
GND	4	GND	Ground
SDA	5	I/O	Serial data address input/output
SCL	6	Input	Serial clock.
FT/OUT	7	Output	Frequency test/output driver (open drain)
V_{CC}	8	Power	Supply voltage
N.C.		-	No connection

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Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	-55	-	+150	°C
V_{CC}	DC Supply Voltage	-0.3	-	6.0	V
V_{IO}	Input / Output Voltage	-0.3	-	6.0	V
IO	Output Current			20	mA

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	2.0	-	5.5	V
V_{IO}	I/O Pin Voltage	GND	-	5.5	V
T_A	Operating Temperature Range	-40	-	+85	°C

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DC Electrical Characteristics

DC characteristics

Symbol	Parameter	Test Condition*1	MIN	TYP	MAX	Unit
I_{LI}	Input leakage current	0V≤VIN ≤V_{CC}			±1	μA
I_{LO}	Output leakage current	0V ≤VOUT≤V_{CC}			±1	μA
I_{CC}	Supply current	SCL clock frequency = 400 kHz			150	μA
V_{IL}	Input low voltage		-0.3		0.3*V_{CC}	V
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.4	V
V_{PU}	Pull-up supply voltage (open drain)	FT/OUT			5.5	V
V_{BAT}	Battery supply voltage		2.5*2	3	3.5*3	V
I_{BAT}	Battery supply current	TA = 25°C, V_{CC} = 0 V, oscillator ON, V_{BAT} = 3 V		0.4	1	μA

Notes:
1. Valid for ambient operating temperature: TA = -40 to 85°C; VCC = 2.0 to 5.5 V (except where noted).
2. After switchover (V_{SO}), VBAT(min) can be 2.0 V for crystal with R_S = 40 k Ω.
3. For rechargeable back-up, VBAT(max) may be considered VCC.

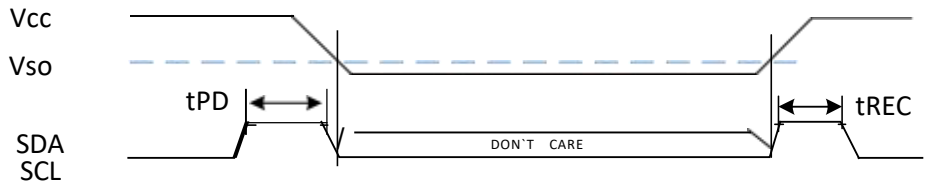
Crystal electrical characteristics

Symbol	Parameter*1*2	MIN	TYP	MAX	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			100	k Ω
C_L	Load capacitance		12.5		pF

Notes:
1. These values are externally supplied if using the SOIC8 package.Crystal selection needs to meet the above conditions.
2. Load capacitors are built in the FRTC4111S. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

AC Electrical characteristics

Power down/up mode AC waveforms



Power down/up AC characteristics

Symbol	Parameter*1*2	MIN	MAX	Unit
t_{PD}	SCL and SDA at VIH before power down	0		ns
t_{REC}	SCL and SDA at VIH after power up	10		μs

Notes:
1. Valid for ambient operating temperature: TA = -40 to 85°C; VCC = 2.0 to 5.5 V (except where noted).
2. VCC fall time should not exceed 5 mV/μs.

Power down/up trip points DC characteristics

Symbol	Parameter*1*2	MIN	TYP	MAX*3	Unit
V_{SO}	Battery backup switchover voltage	-	V_{BAT} - 0.80	-	V

Notes
1. Valid for ambient operating temperature: T_A = -40 to +85°C; V_{CC} = 2.0 to 5.5 V (except where noted).
2. All voltages referenced to GND.
3. After VCC is powered up initially, I2C required to read/write to activate the oscillator.
4. When VCC< V_{SO}, the device automatically switches over to the battery mode, at this time, I2C can not read and write. So For VCC=3.3V application, if initial battery voltage is ≥ VCC, it may necessary to reduce battery voltage.

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I2C AC Characteristics

(TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals	Fast mode			300	ns
		Standard mode			1000	
t_F	Fall Time of Both SDA and SCL Signals	Fast mode			300	ns
		Standard mode			300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			

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Application Information

Operation

The FRTC4111S operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: seconds register
- 2nd byte: minutes register
- 3rd byte: century/hours register
- 4th byte: day register
- 5th byte: date register
- 6th byte: month register
- 7th byte: years register
- 8th byte: control register
- 9th - 64th bytes: RAM

The FRTC4111S continually monitors VCC for an out of tolerance condition. When VCC falls below V_{SO}, the device automatically switches over to the battery mode.At this time inputs to the device will not be recognized to prevent erroneous data from being written to the device. Upon power-up, the device switches from battery mode to VCC mode at VCC>V_{SO} and recognizes inputs.

2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be pulled up via a pull-up resistors.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain high.

Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such away that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

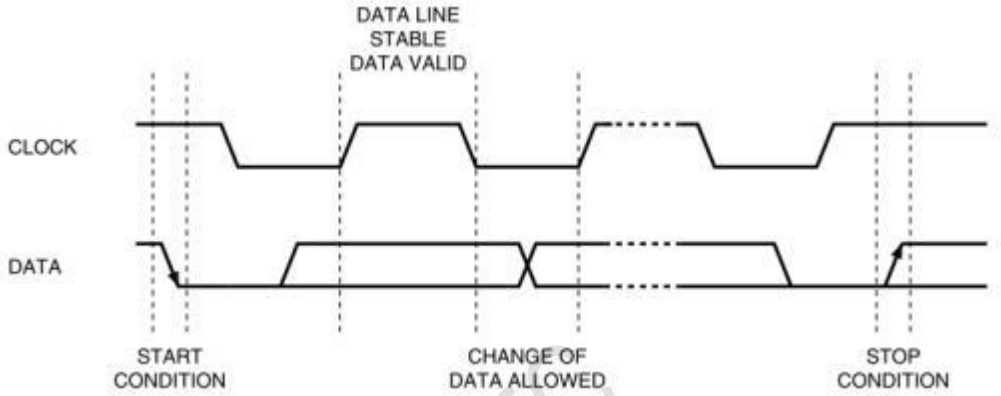

Figure4: Serial bus data transfer sequence

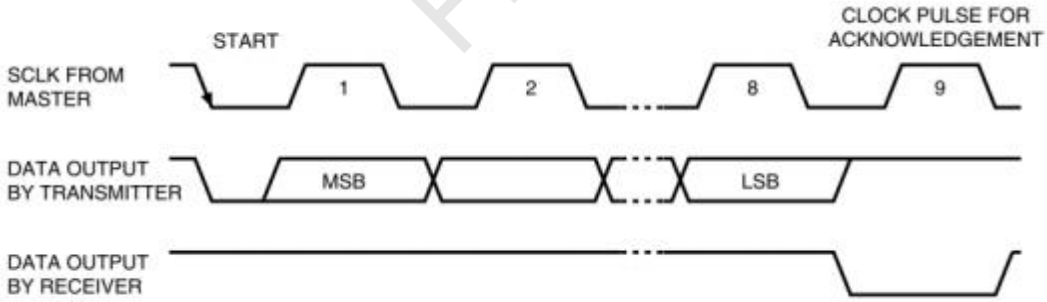

Figure5: Acknowledgement Sequence

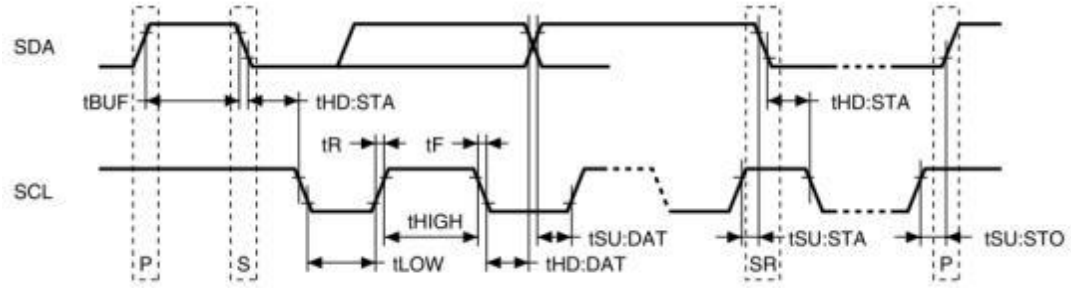

Figure6: Bus timing requirements sequence

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Read mode

In this mode,
the master reads the FRTC4111S slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The FRTC4111S slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

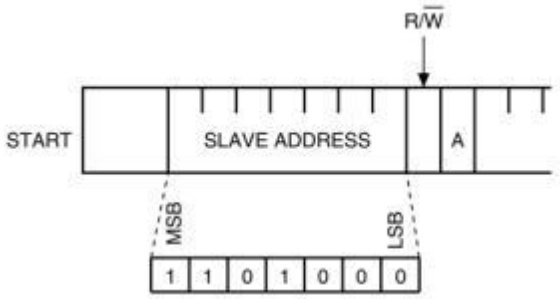

Figure7: Slave address location

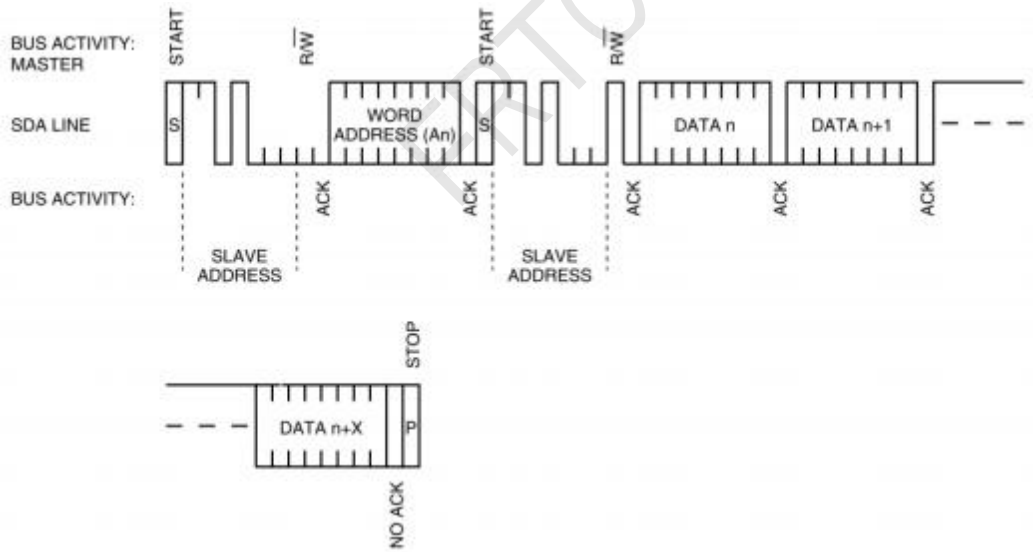

Figure8: Read Mode Sequence

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Write mode

In this mode the master transmitter transmits to the FRTC4111S slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The FRTC4111S slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

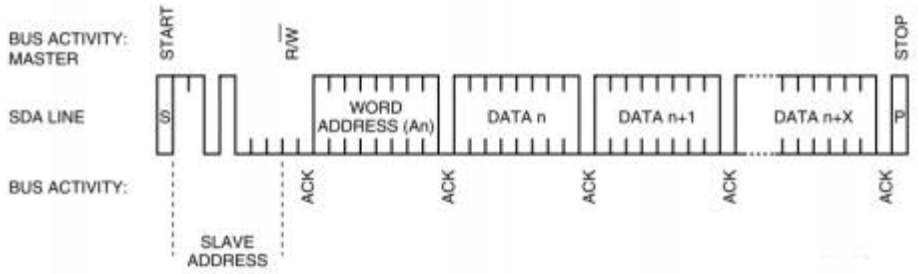

Figure9: Write mode sequence

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Register Configuration

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00H	ST	10 seconds			Seconds				Seconds	00-59
01H	X	10 minutes			Minutes				Minutes	00-59
02H	CEB	CB	10 hours		Hours				Century/hours	0-1/00-23
03H	X	X	X	X	X	Day			Day	01-07
04H	X	X	10 dates		Date				Date	01-31
05H	X	X	X	10 M.	Month				Month	01-12
06H	10 years				Years				Year	00-99
07H	OUT	FT	S	Calibration					Control	
08H-3FH									RAM 56 x 8	00H-FFH

Seconds register(0x00)

D7(ST)	D6	D5	D4	D3	D2	D1	D0
ST=1:oscillator stop ST=0:oscillator enable	10 seconds			Seconds			

Minutes register(0x01)

D7	D6	D5	D4	D3	D2	D1	D0
X	10 minutes			Minutes			

Century/hours register(0x02)

D7(CEB)	D6(CB)	D5	D4	D3	D2	D1	D0
CEB=1:Century enable CEB=0:Century disable	Set Century enable(CEB=1), CB will be toggled either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state)	10 hours		Hours			

Day register(0x03)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	Day		

Date register(0x04)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	10 dates		Date			

Month register(0x05)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	10M	Month			

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Year register(0x06)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

Control register(0x07)

D7(OUT)	D6(FT)	D5	D4	D3	D2	D1	D0
Output driver pin When D6(FT)=0 OUT=0 FT/OUT pin outputs low OUT=1 FT/OUT pin outputs high	FREQUENCY TEST bit FT=0 Output 512Hz Disable FT=1 Output 512Hz Enable	Calibration offset value **1**11111=+126.108 ... **1**00010=+8.136 **1**00001=+4.068 000000=0 **0**00001=-2.034 **0**00010=-4.068 ... **0**11111=-64.108					

RAM register(0x08-0x3F)

D7	D6	D5	D4	D3	D2	D1	D0
RAM 56 x 8							

Notes:
1.In order to guarantee oscillator startup after the initial power-up, set the ST bit to a '1,' then reset this bit to a '0.' This sequence enables a “kick start” circuit which aids the oscillator startup during worst case conditions of voltage and temperature.

2.The seven clock registers may be read one byte at a time, or in a sequential block. The control register (address location 7) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250 ms to allow the read to be completed before the update occurs. This will prevent a transition of data during the read.This 250 ms delay affects only the clock register update and does not alter the actual clock time.

Preferred initial power-on defaults

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a '1'. All other register bits will initially power on in a random state.After the chip is powered on for the first time, all registers are required to be initialized.

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Clock Calibration

The FRTC4111S is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each FRTC4111S improves to better than ±2 ppm at 25°C. The oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The FRTC4111S design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit calibration byte found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits (D4-D0) in the control register (addr 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64-minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or -5.35 seconds per month which corresponds to a total range of +5.5 or −2.75 minutes per month. Two methods are available for ascertaining how much calibration a given FRTC4111S may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude,
it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure.
All the designer has to do is provide a simple utility that accessed the calibration byte. The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the control register, is set to a '1', and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a -10(XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

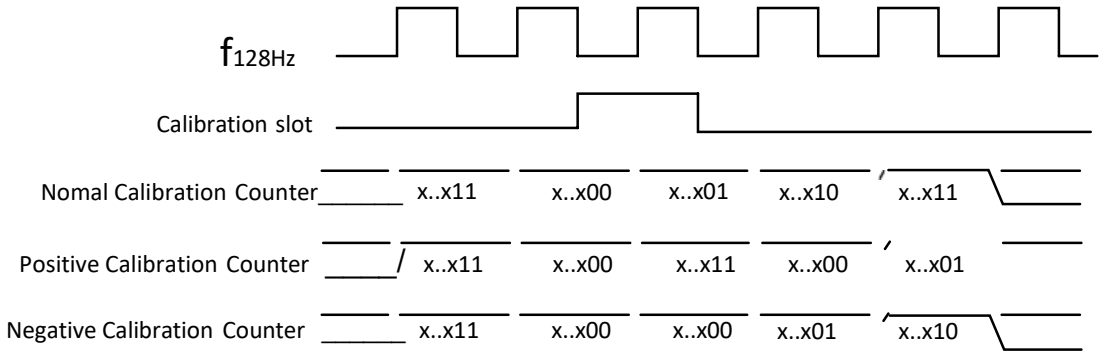

Figure10: Clock Calibration

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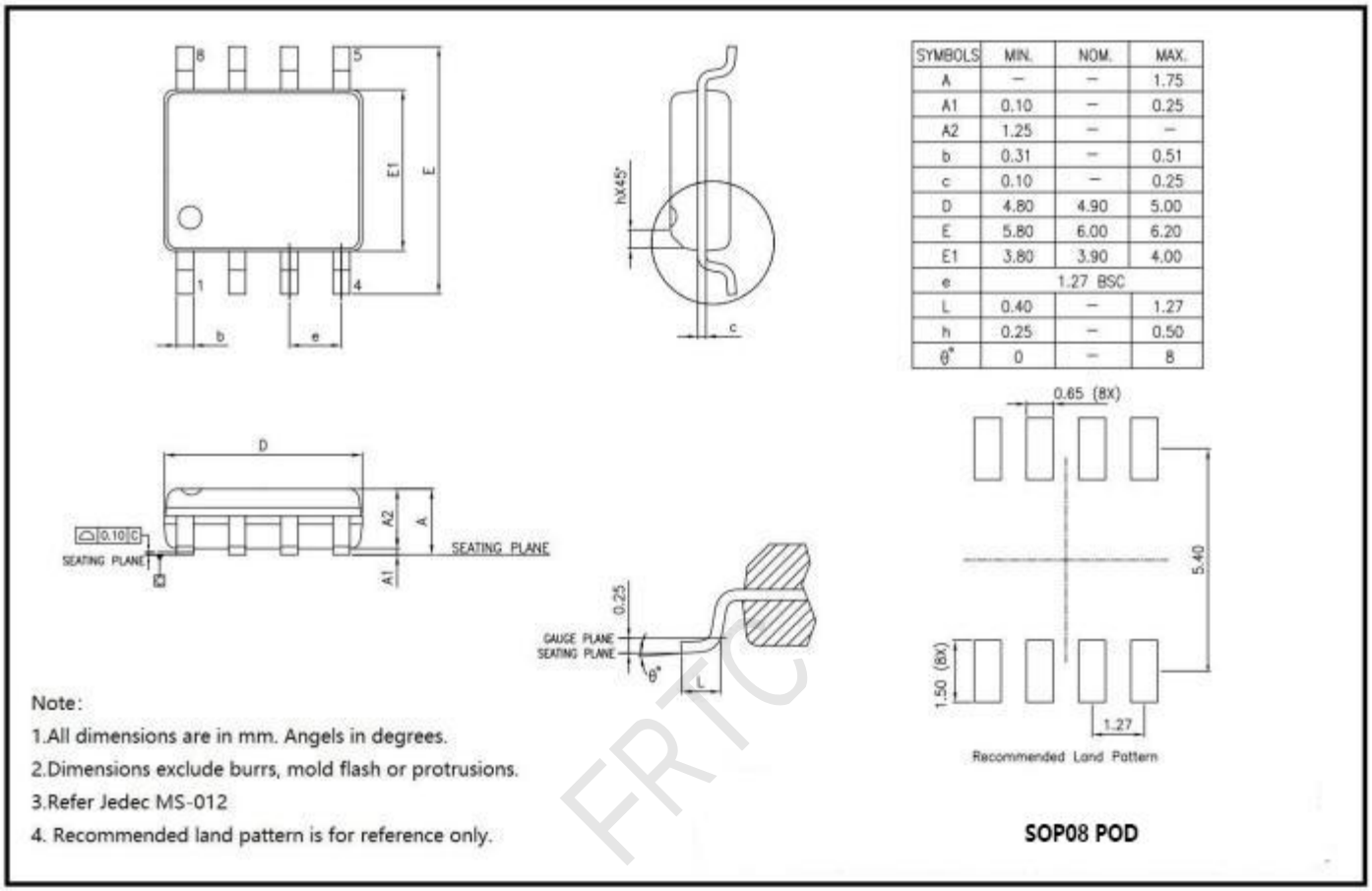
Package Information

FRTC4111S SOP-8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

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Revision History

Revision	Description	Date
V1.3		2024/11/1