A Product Line of
Diodes Incorporated

PI6C557-03

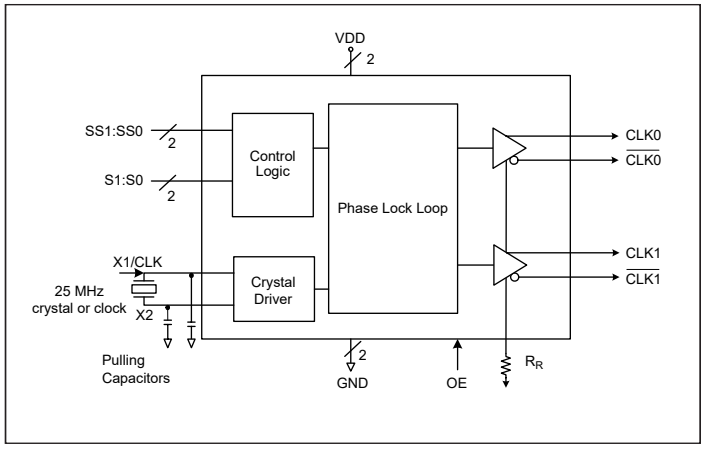
PCI Express Clock

Description

The PI6C557-03 is a spread spectrum clock generator supporting PCI Express and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The PI6C557-03 provides two differential (HCSL) spread spectrum outputs. The PI6C557-03 is configured to select spread and clock selection. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 25MHz, 100MHz, 125MHz and 200MHz clock frequencies. It also provides spread selection of ±0.25%, -0.5%, -0.75%, and no spread.

Block Diagram



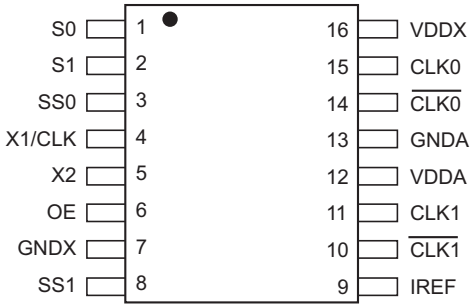
Features

- LVDS Compatible Outputs
- Supply Voltage of 3.3V ±10%
- 25MHz Input Frequency
- HCSL Outputs, 0.7V Current Mode Differential Pair
- Jitter 60ps Cycle-to-cycle (typical)
- Spread of ±0.25%, -0.5%, -0.75%, and No Spread
- Industrial Temperature Range
- Packaging: (Pb-free and Green)
  - 16-pin, TSSOP (L)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin Number	Pin Name	I/O Type	Description
1	S0	Input	Select pin 0 (Internal pull-up resistor). See Table 1.
2	S1	Input	Select pin 1 (Internal pull-up resistor). See Table 1.
3	SS0	Input	Spread Select pin 0 (Internal pull-up resistor). See Table 2.
4	X1/CLK	Input	Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
5	X2	Output	Crystal connection. Leave unconnected for clock input.
6	OE	Input	Output enable. Internal pull-up resistor.
7	GNDX	Power	Crystal ground pin.
8	SS1	Input	Spread Select pin 1 (Internal pull-up resistor). See Table 2.
9	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
10	$\overline{\text{CLK1}}$	Output	HCSL compliment clock output
11	CLK1	Output	HCSL clock output
12	VDDA	Power	Connect to a +3.3V source.
13	GNDA	Power	Output and analog circuit ground.
14	$\overline{\text{CLK0}}$	Output	HCSL compliment clock output
15	CLK0	Output	HCSL clock output
16	VDDX	Power	Connect to a +3.3V source.

Table 1. Output Select Table

S1	S0	CLK(MHz)
0	0	25
0	1	100
1	0	125
1	1	200

Table 2. Spread Selection Table

SS1	SS0	Spread
0	0	Center ±0.25
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between each V_{DD} pin and the ground plane and placed as close to the V_{DD} pin as possible.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors

C_L = Crystals's load capacitance in pF

Crystal Capacitors (pF) = (C_L - 8) *2

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16-8)*2=16.

Current Source (Iref) Reference Resistor - R_R

If board target trace impedance is 50Ω,
then R_R = 475Ω providing an IREF of 2.32 mA. The output
current (I_{OH}) is 6*IREF.

Output Termination

The PCI Express differential clock outputs of the PI6C557-03 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6C557-03 can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

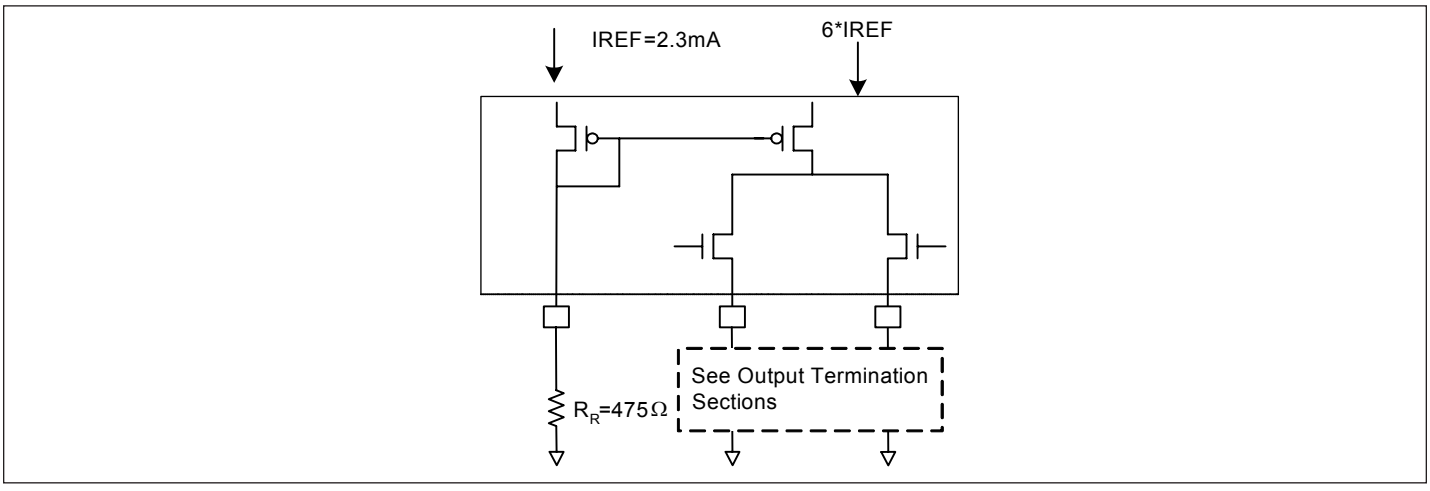


Figure 1. Output Structures

PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω

Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	0.225 min to 12.6 max	inch

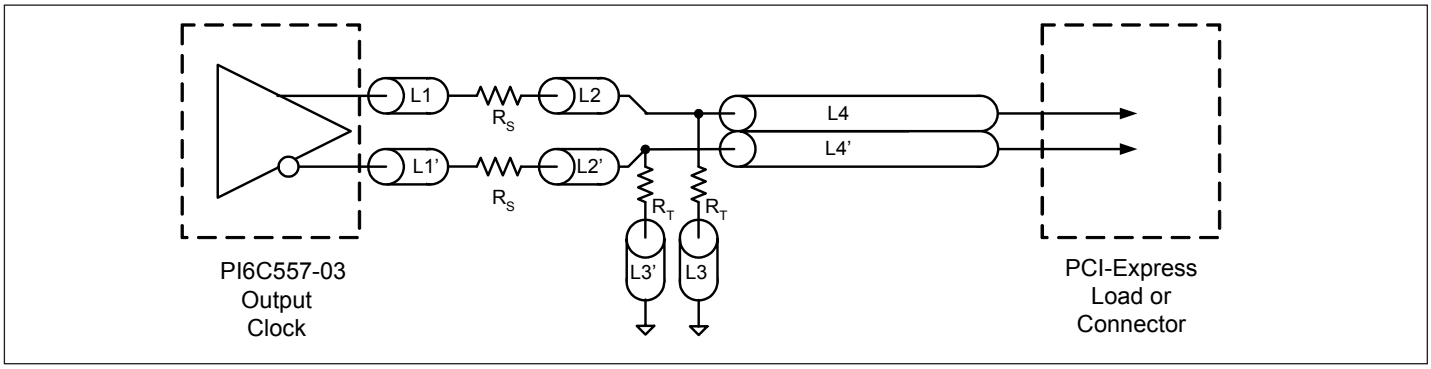


Figure 2. PCI Express Device Routing

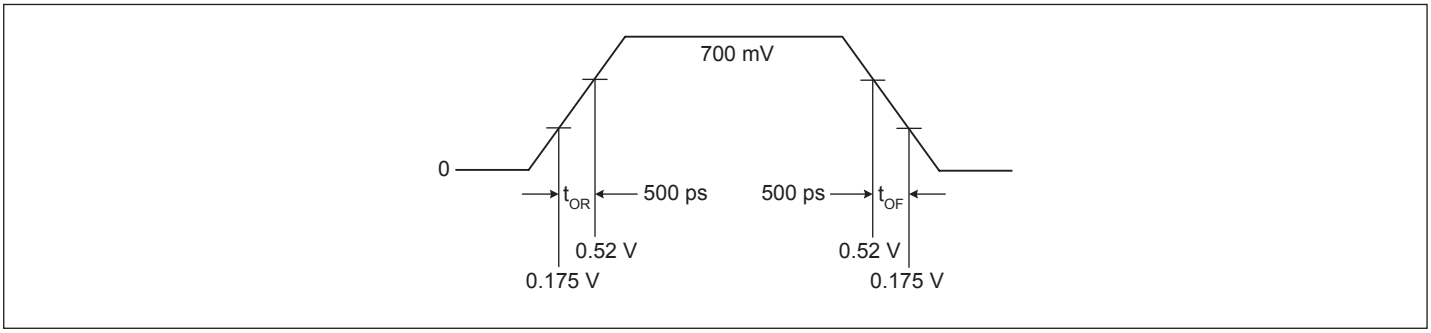


Figure 3. Typical PCI Express (HCSL) Waveform

Application Information

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_P	100	Ω
R_Q	100	Ω
R_T	150	Ω
L3 length, route as 100Ω differential trace.		
L3 length, route as 100Ω differential trace.		

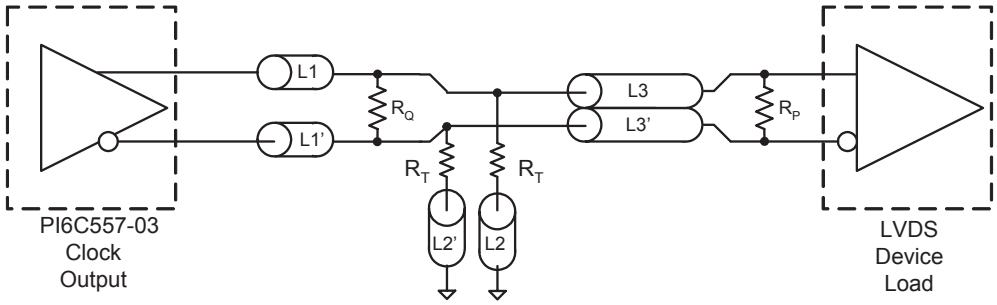


Figure 4. LVDS Device Routing

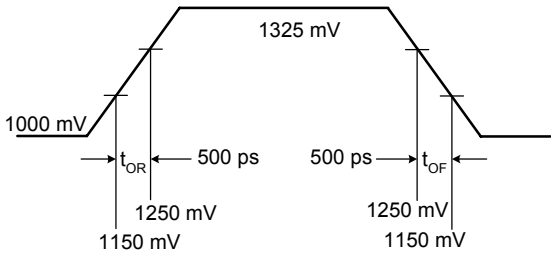


Figure 5. Typical LVDS Waveform

Maximum Ratings

Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to V_{DD}+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Characteristics

V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.60	V
V_{IH}	Input High Voltage(1)	S0, S1, OE, CLK, SS0, SS1		2.0		V_{DD} +0.3	V
V_{IL}	Input Low Voltage(1)	S0, S1, OE, CLK, SS0, SS1		GND -0.3		0.8	V
I_{IL}	Input Leakage Current	0 < V_{IN} < V_{DD}	With input pull-up and pull-downs	-20		20	µA
			Without input pull-up and pull-downs	-5		5	
I_{DD}	Operating Supply Current	R_L = 50Ω, C_L = 2pF				95	mA
I_{DDOE}		OE = LOW				50	mA
C_{IN}	Input Capacitance	Input pin capacitance				7	pF
C_{OUT}	Output Capacitance	Output pin capacitance				6	pF
L_{PIN}	Pin Inductance					5	nH
R_{OUT}	Output Resistance	CLK Outputs		3.0			kΩ

Notes:
1. Single edge is monotonic when transitioning through region.

AC Characteristics

V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{IN}	Input Frequency			25		MHz
V_{OUT}	Output Frequency		25		200	MHz
V_{OH}	Output High Voltage(1,2)	@V_{DD} = 3.3V	660	700	850	mV
V_{OL}	Output Low Voltage(1,2)		-150	0		mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			60	100	ps
M_F	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
t_{OR}	Rise Time(1,2)	From 0.175V to 0.525V	175	332	700	ps
t_{OF}	Fall Time(1,2)	From 0.525V to 0.175V	175	344	700	ps
$\Delta T_R/\Delta T$	Rise/Fall Time Variation(1,2)				125	ps
T_{SKEW}	Skew between outputs	$V_{DD}/2$			50	ps
$T_{DUTY-CYCLE}$	Duty Cycle(1,3)		45		55	%
T_{OE}	Output Enable Time(5)	All outputs		0.1		µs
T_{OT}	Output Disable Time(5)	All outputs		0.1		µs
t_{STABLE}	From power-up to V_{DD} = 3.3V		1.6	3.0		ms
t_{SPREAD}	Setting period after spread change			3.0		ms
Ferror	Synthesizer Error	PLL locked, xtal load is matched and SSC off		0		ppm

Notes:

1. RL = 50Ω with CL = 2pF and RR = 475Ω
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Thermal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			90	°C/W
θ_{JC}	Thermal Resistance Junction to Case				24	°C/W

Recommended Crystal Specification

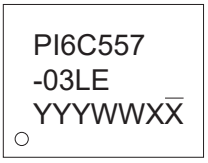
Diodes recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm
https://www.diodes.com/datasheet/download/FL.pdf

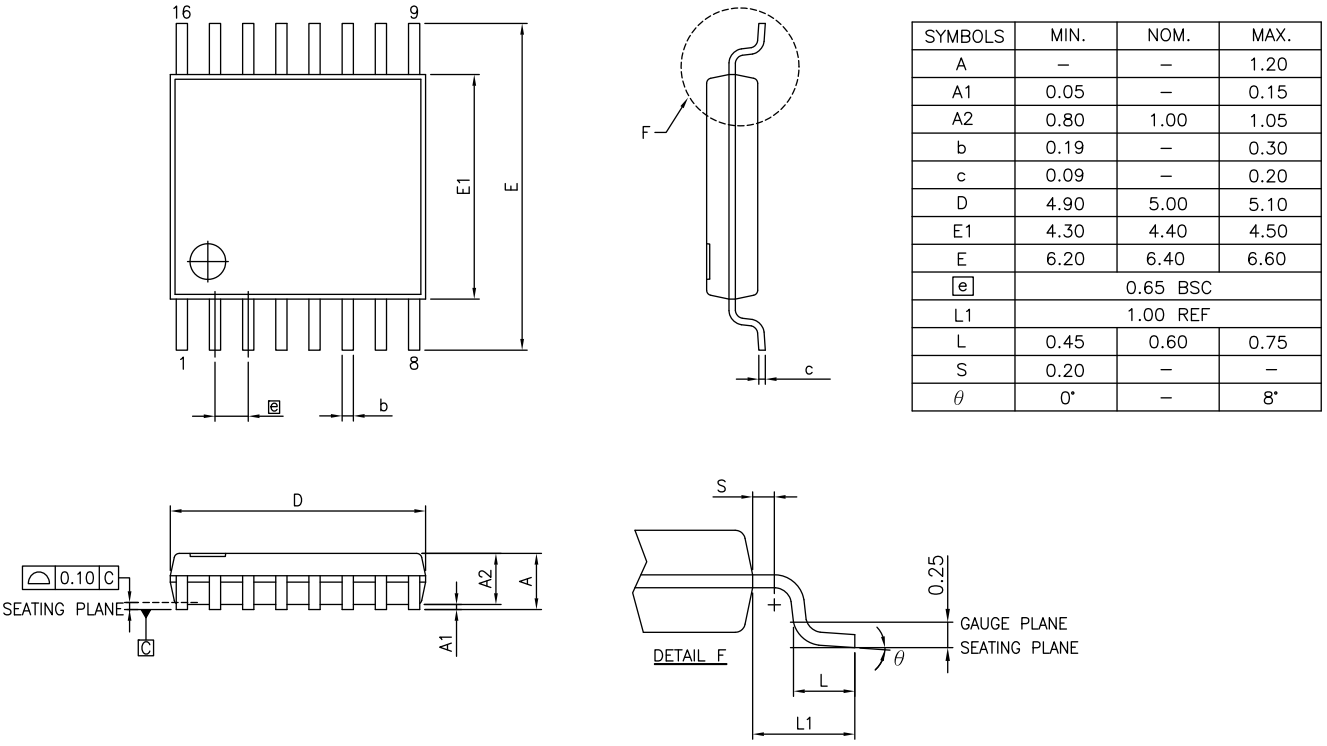
Part Marking



1st Y: Die Rev
2nd & 3rd Y: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical

16-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/24/16

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L16)

DOCUMENT CONTROL #: PD-1310 REVISION: G

16-0061

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Number	Package Code	Package Description
PI6C557-03LEX	L	16-Pin, 173mil Wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

www.diodes.com