CKS32F103x8
CKS32F103xB

Performance line ARM-based 32-bit MCU with 64 or 128KB flash

Features

◆ **ARM 32-bit Cortex™-M3 CPU Core**
– 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
– Single-cycle multiplication and hardware division

◆ **Memories**
– 64 or 128 Kbytes of Flash memory
– 20 Kbytes of SRAM

◆ **Clock, reset and supply management**
– 2.0 to 3.6 V application supply and I/Os
– POR, PDR, and programmable voltage detector (PVD)
– 4-to-16 MHz crystal oscillator
– Internal 8 MHz factory-trimmed RC
– Internal 40 kHz RC
– PLL for CPU clock
– 32 kHz oscillator for RTC with calibration

◆ **Low power**
– Sleep, Stop and Standby modes
– V_{BAT} supply for RTC and backup registers

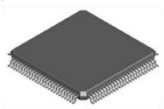
◆ **2 x 12-bit, 1 µs A/D converters (up to 16 channels)**
– Conversion range: 0 to 3.6 V
– Dual-sample and hold capability
– Temperature sensor

◆ **DMA**
– 7-channel DMA controller
– Peripherals supported: timers, ADC, SPIs, I^2Cs and USARTs


QFN36 6 x 6 mm


LQFP48 7 x 7 mm


LQFP64 10 x 10 mm


LQFP100 14 x 14 mm

◆ **Up to 80 fast I/O ports**
– 26/37/51/80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant

◆ **Debug mode**
– Serial wire debug (SWD) & JTAG interfaces

◆ **7 timers**
– Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
– 16-bit, motor control PWM timer with dead-time generation and emergency stop
– 2 watchdog timers (Independent and Window)
– SysTick timer 24-bit downcounter

◆ **Up to 9 communication interfaces**
– Up to 2 × I^2C interfaces (SMBus/PMBus)
– Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
– Up to 2 SPIs (18 Mbit/s)
– CAN interface (2.0B Active)
– USB 2.0 full-speed interface

◆ **CRC calculation unit, 96-bit unique ID**

◆ **Packages are ECOPACK®**

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1. Introduction

This datasheet provides the ordering information and mechanical device characteristics of the CKS32F103x8 and CKS32F103xB performance line microcontrollers.
The CKS32Fxx datasheet should be read in conjunction with the other reference manuals.
For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address:http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2. Description

The CKS32F103xx medium-density performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The devices operate from a 2.0 to 3.6 V power supply. They are available in the –40 to +105 ℃ temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The CKS32F103xx medium-density performance line family includes devices in four different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included. The description below gives an overview of the complete range of peripherals proposed in this family.

These features make the CKS32F103xx medium-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

2.1 Device overview

Table 1. CKS32F103xx medium-density device features and peripheral counts

Peripheral		CKS32F103Tx		CKS32F103Cx		CKS32F103Rx		CKS32F103Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM-Kbytes		20		20		20		20	
Timers	General-purpose	3		3		3		3	
	Advanced-control	1		1		1		1	
Communication	SPI	1		2		2		2	
	I^2C	1		2		2		2	
	USART	2		3		3		3	
	USB	1		1		1		1	
	CAN	1		1		1		1	
GPIOs		26		37		51		80	
12-bit synchronized ADC Number of channels		2 10 channels		2 10 channels		2 16 channels		2 16 channels	
CPU frequency		72MHz							
Operationg voltage		2.0 to 3.6V							
Operating temperatures		Ambient temperatures: -40 to +105 ℃							
Packages		QFN36		LQFP48		LQFP64		LQFP100	

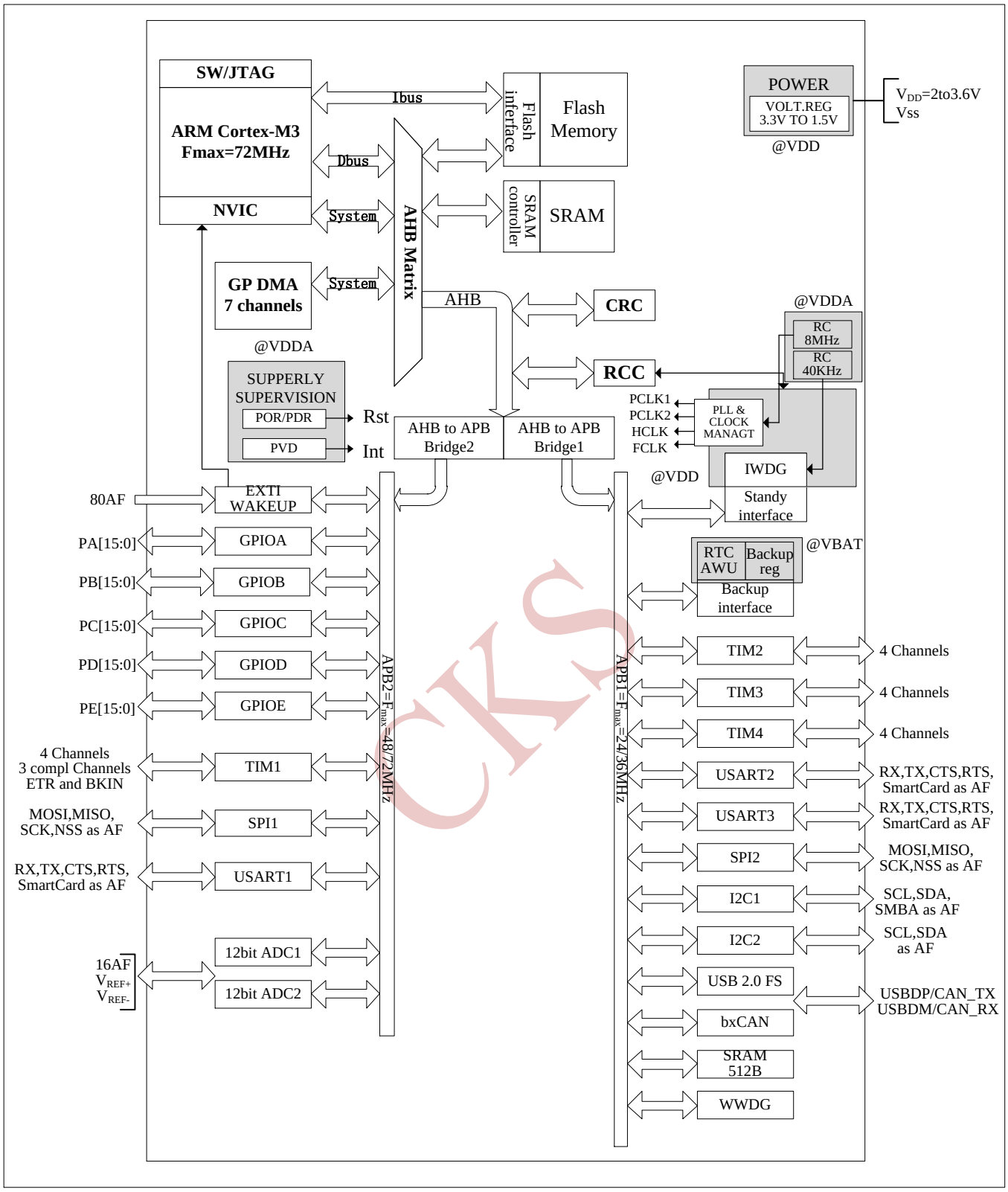


Figure 1. CKS32F103xx performance line block diagram

1. AF =alternate function on I/O port pin.

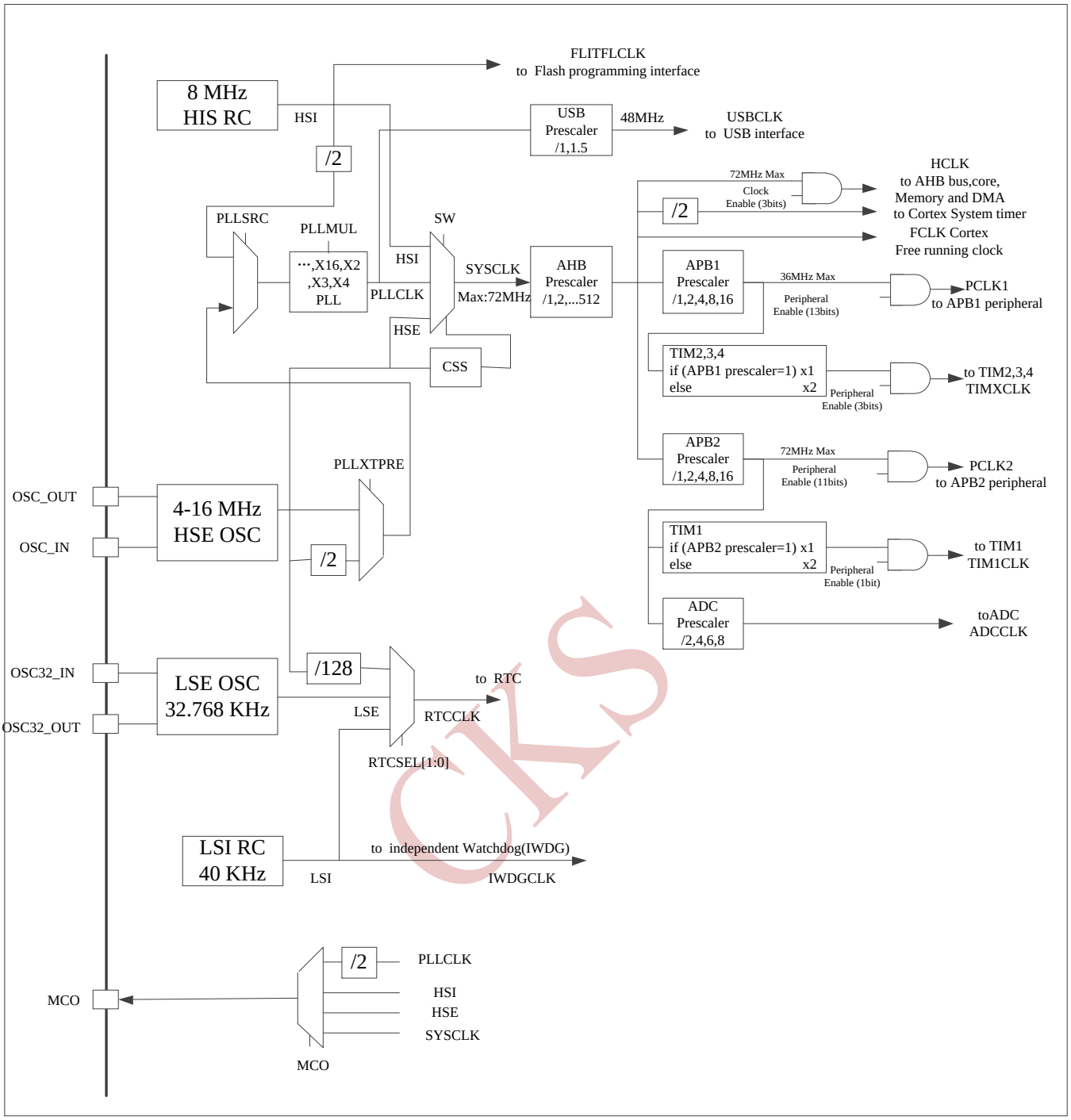


Figure 2. CLOCK TREE

1. HSE=high-speed external clock signal; HIS= high-speed internal clock signal; LSI= low- internal clock signal; LSE= low-speed external clock signal;
2. When the HIS is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64MHz;
3. For the USB function to be available, both HSE and PLL must be enabled, with USBCLK running at 48MHz;
4. To have an ADC conversion time of 1µs, APB2 must be at 14MHz, 28MHz or 56MHz.

2.2 Full compatibility throughout the family

The CKS32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. The CKS32F103x8 and CKS32F103xB are referred to as medium-density devices
Low- and high-density devices are an extension of the CKS32F103x8/B devices, they are specified in the CKS32F103x4/6 and CKS32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less

timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I^2S and DAC, while remaining fully compatible with the other members of the CKS32F103xx family.
The CKS32F103x4, CKS32F103x6, CKS32F103xC, CKS32F103xD and CKS32F103xE are a drop-in replacement for CKS32F103x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.
Moreover, the CKS32F103xx performance line family is fully compatible with all existing CKS32F101xx access line and CKS32F102xx USB access line devices.

Table 2. CKS32F103xx family

Pinout	Low-density devices		Medium-density devices		High-density devices		
	16KB Flash	32KB Flash	64 KB Flash	128 KB Flash	256 KB Flash	384 KB Flash	512 KB Flash
	8KB RAM	10 KB RAM	20 KB RAM	20 KB RAM	48 KB RAM	64 KB RAM	46 KB RAM
100			3×USARTs 3×16-bit timers 2×SPI,2×I^2Cs,USB,CAN 1×PWM timer 2×ADCs		5×USARTs 4×16-bit timers 3×SPI,2×I^2Ss, 2×I^2Cs,USB,CAN 2×PWM timers, 3×ADCs,2×DACs,1×SDIO		
64	2×USARTs 2×16-bit timers 1×SPI,1×I^2C,USB,CAN 1×PWM timer 2×ADCs						
48							
36							

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.
The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.
The CKS32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Twenty Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The CKS32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining

- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See Figure 2 for details on the clock tree.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

2.3.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to Figure 10.

2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.3.12 Low-power modes

The CKS32F103xx performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when

an interrupt/event occurs.

- **Stop** mode The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.5 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode. The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.
- **Standby** mode The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.5 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry. The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.
The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and advanced-control timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.
The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Timers and watchdogs

The medium-density CKS32F103xx performance line devices include an advanced-control timer, three general-purpose timers, two watchdog timers and a SysTick timer.
Table 3compares the features of the advanced-control and general-purpose timers.

Table 3. Timer feature comparison

Timers	Counter Resolution	Counter Type	Prescaler Factor	DMA request geneartion	Capture/compare channels	Complementary outputs
TIM1	16-bit	up, down, up/down	Any integer Between 1 and 65536	YES	4	YES
TIM2, TIM3, TIM4	16-bit	up, down, up/down	Any integer Between 1 and 65536	YES	4	NO

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge-or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM

generator, it has full modulation capability (0-100%).
In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.
Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the CKS32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages. The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.
These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.3.16 I₹C bus

Up to two I₹C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.
They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.17 Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.
All USART interfaces can be served by the DMA controller.

2.3.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.
Both SPIs can be served by the DMA controller.

2.3.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.20 Universal serial bus (USB)

The CKS32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and

suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.
The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.
I/Os on APB2 with up to 18 MHz toggling speed.

2.3.22 ADC (analog-to-digital converter)

Two 12-bit analog-to-digital converters are embedded into CKS32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.
Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.
An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.
The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

2.3.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.Pinouts and pin description

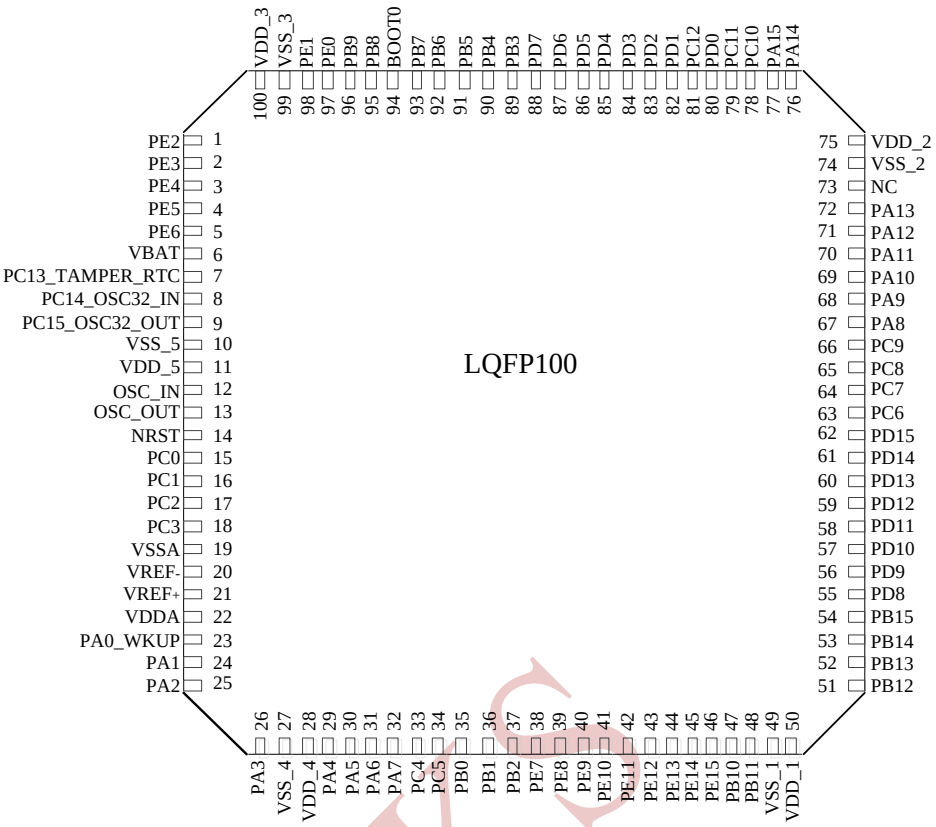


Figure 3. CKS32F103xx performance line LQFP100 pinout

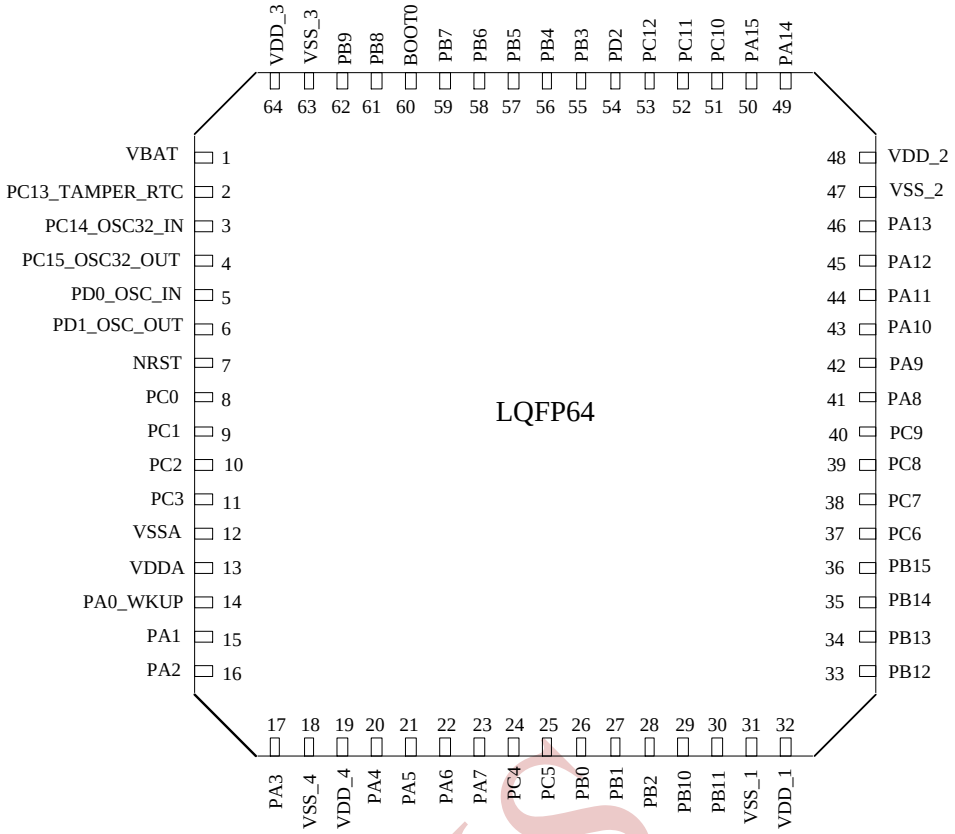


Figure 4. CKS32F103xx performance line LQFP64 pinout

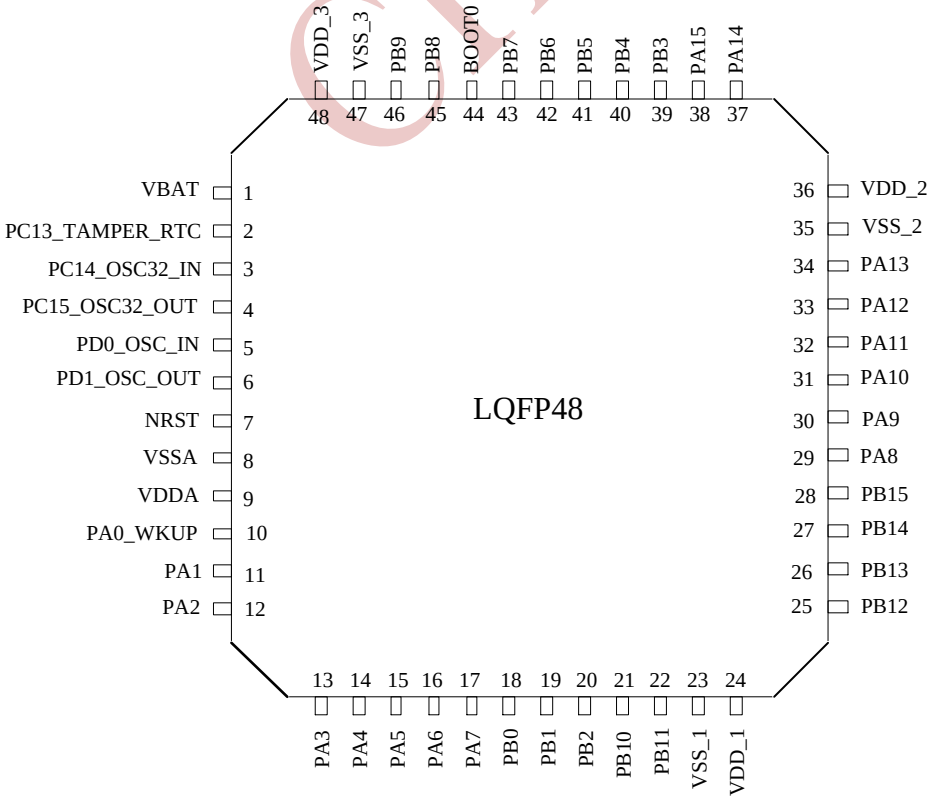


Figure 5. CKS32F103xx performance line LQFP48 pinout

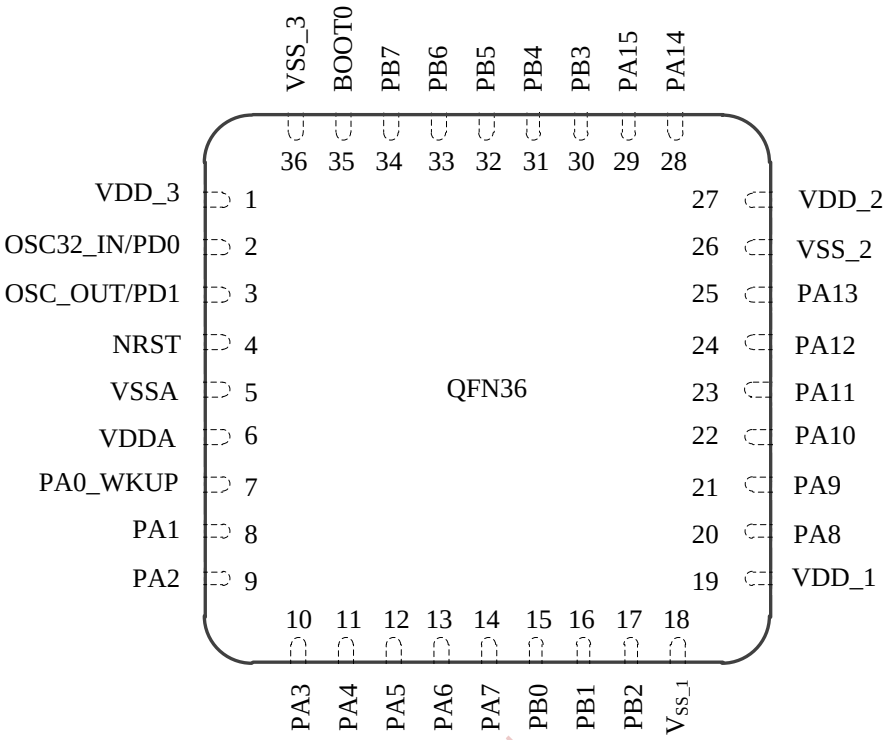


Figure 6. CKS32F103xx performance line QFN36 pinout

Table 4. Medium-density CKS32F103xx pin definitions

Pins				Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP48	LQFP64	LQFP100	QFN36					Defult	Remap
-	-	1	-	PE2	I/O	FT	PE2	TRACECK	
-	-	2	-	PE3	I/O	FT	PE3	TRACED0	
-	-	3	-	PE4	I/O	FT	PE4	TRACED1	
-	-	4	-	PE5	I/O	FT	PE5	TRACED2	
-	-	5	-	PE6	I/O	FT	PE6	TRACED3	
1	1	6	-	V_{BAT}	S	FT	V_{BAT}		
2	2	7	-	PC13-TAMPER -RTC[5]	I/O	FT	PC13[6]	TAMPER -RTC	
3	3	8	-	PC14-OSC21-IN[5]	I/O	FT	PC14[6]	OSC_IN	
4	4	9	-	PC15-OSC32-OUT[5]	I/O	FT	PC15[6]	OSC_OUT	
-	-	10	-	V_{SS_5}	S		V_{SS_5}		
-	-	11	-	V_{DD_5}	S		V_{DD_5}		
5	5	12	2	OSC_IN	I/O	FT	OSC_IN		PD0[7]
6	6	13	3	OSC_OUT	I/O	FT	OSC_OUT		PD1[7]
7	7	14	4	NRST	I/O	FT	NRST		
-	8	15	-	PC0	I/O	FT	PC0	ADC12_IN10	
-	9	16	-	PC1	I/O	FT	PC1	ADC12_IN11	
-	10	17	-	PC2	I/O	FT	PC2	ADC12_IN12	
-	11	18	-	PC3	I/O	FT	PC3	ADC12_IN13	
8	12	19	5	V_{SSA}	S	FT	V_{SSA}		
-	-	20	-	V_{REF-}	S		V_{REF-}		
-	-	21	-	V_{REF+}	S		V_{REF+}		
9	13	22	6	V_{DDA}	S	FT	V_{DDA}		
10	14	23	7	PA0_WKUP	I/O	FT	PA0	WKUP/ USART2_CTS[8] ADC12_IN0/ TIM2_CH1_ETR[8]	
11	15	24	8	PA1	I/O	FT	PA1	USART2_RTS[8] ADC12_IN1/ TIM2_CH2[8]	
12	16	25	9	PA2	I/O	FT	PA2	USART2_TX[8] ADC12_IN2/ TIM2_CH3[8]	
13	17	26	10	PA3	I/O	FT	PA3	USART2_RX[8] ADC12_IN3/ TIM2_CH4[8]	
-	18	27	-	V_{SS_4}	S	FT	V_{SS_4}		
-	19	28	-	V_{DD_4}	S	FT	V_{DD_4}		
14	20	29	11	PA4	I/O	FT	PA4	SPI1_NSS[8]/ USART2_CK[8]/ ADC12_IN4	
15	21	30	12	PA5	I/O	FT	PA5	SPI1_SCK[8]/ ADC12_IN5	
16	22	31	13	PA6	I/O	FT	PA6	SPI1_MISO[8]/ ADC12-IN6/ TIM3_CH1[8]	TIM1_BKIN
17	23	32	14	PA7	I/O	FT	PA7	SPI1_MOSI/ ADC12_IN7/ TIM3_CH2	TIM1_CHI1
-	24	33	-	PC4	I/O	FT	PC4	ADC12_IN14	
-	25	34	-	PC5	I/O	FT	PC5	ADC12_IN15	

18	26	35	15	PB0	I/O	FT	PB0	ADC12-IN8/ TIM3_CH3(8)	TIM1_CH2N
19	27	36	16	PB1	I/O	FT	PB1	ADC12-IN9/ TIM3_CH4(8)	TIM1_CH3N
20	28	37	17	PB2	I/O	FT	PB2/BOOT1		
-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
-	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(8)	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(8)	TIM2_CH4
23	31	49	18	V_{SS_1}	S	FT	V_{SS_1}		
24	32	50	19	V_{DD_1}	S	FT	V_{DD_1}		
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBA/ USART3_CK(8)/ TIM1_BKIN(8)	
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(8)/ TIM1_CH1N(8)	
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(8)/ TIM1_CH2N(8)	
28	36	54		PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(8)	
-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1/ USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
-	37	63		PC6	I/O	FT	PC6		TIM3_CH1
-	38	64		PC7	I/O	FT	PC7		TIM3_CH2
-	39	65		PC8	I/O	FT	PC8		TIM3_CH3
-	40	66		PC9	I/O	FT	PC9		TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(8)/ MCO	
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX(8)/ TIM1_CH2(8)	
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX(8)/ TIM1_CH3(8)	
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(8)/ USBDM/ TIM1_CH4(8)	

33	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX[8]/ USBDP/ TIM1_ETR[8]	
34	46	72	25	PA13	I/O	FT	JTMS/SWDIO		PA13
-	-	73	-	Not connected					
35	47	74	26	V_{SS_2}	S		V_{SS_2}		
36	48	75	27	V_{DD_2}	S		V_{DD_2}		
37	49	76	28	PA14	I/O	FT	JTCK/SWCLK		PA14
38	50	77	29	PA15	I/O	FT	JTDI		TIM2_CH1_ ETR/PA15/ SPI1_NSS
-	51	78	-	PC10	I/O	FT	PC10		USART3_TX
-	52	79	-	PC11	I/O	FT	PC11		USART3_RX
-	53	80	-	PC12	I/O	FT	PC12		USART3_CK
-	-	81	2	PD0	I/O	FT	OSC_IN[8]		CAN_RX
-	-	82	3	PD1	I/O	FT	OSC_OUT[8]		CAN_TX
-	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	
-	-	84	-	PD3	I/O	FT	PD3		USART2_CT S
-	-	85	-	PD4	I/O	FT	PD4		USART2_RT S
-	-	86	-	PD5	I/O	FT	PD5		USART2_TX
-	-	87	-	PD6	I/O	FT	PD6		USART2_RX
-	-	88	-	PD7	I/O	FT	PD7		USART2_CK
39	55	89	30	PB3	I/O	FT	JTDO		TIM2_CH2/ PB3/ TRACESWO/ SPI1_SCK
40	56	90	31	PB4	I/O	FT	JNTRST		TIM3_CH1/ PB4/ SPI`_MISO
41	57	91	32	PB5	I/O	FT	PB5	I2C1_SMBA	TIM3_CH2/ SPI1_MOSI
42	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL[8]/ TIM3_CH1[8]	USART1_TX
43	59	93	34	PB7	I/O	FT	PB7	T2C1_SDA[8]/ TUN4_CH2[8]	USART1_RX
44	60	94	35	BOOT0	I	FT	BOOT0		
45	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3[8]	I2C1_SCL/ CANRX
46	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4[8]	I2C1_SDA/ CANTX
-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	
-	-	98	-	PE1	I/O	FT	PE1		
47	63	99	36	V_{SS_3}	S	FT	V_{SS_3}		
48	64	100	1	V_{DD_3}	S	FT	V_{DD_3}		

1. I=input, O=output, S=supply;
2. FT=5V tolerant
3. Function availability depends on the chosen device. For devices having reduces peripheral counts, it is always the lower number of peripheral that is included .For example , if a device has only one SPI and two USARTs, they will be called SP1 and USART1 & USART2 , respectively.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset).
7. The pins number 2 and 3 in the QFN36 package ,5 and 6 in the LQFP48 and LQFP64 packages are configured as OSC_IN/OSC_OUT after reset, however the functionality to PD0 and PD1 can be remapped by software on these pins. For the LQFP 100 package,PD0 and PD1 are available by default, so there is no need for remapping.
8. This alternate function can be remapped by software to some other port pins (if available on the used package).

4. Memory mapping

The memory map is shown in Figure 7.

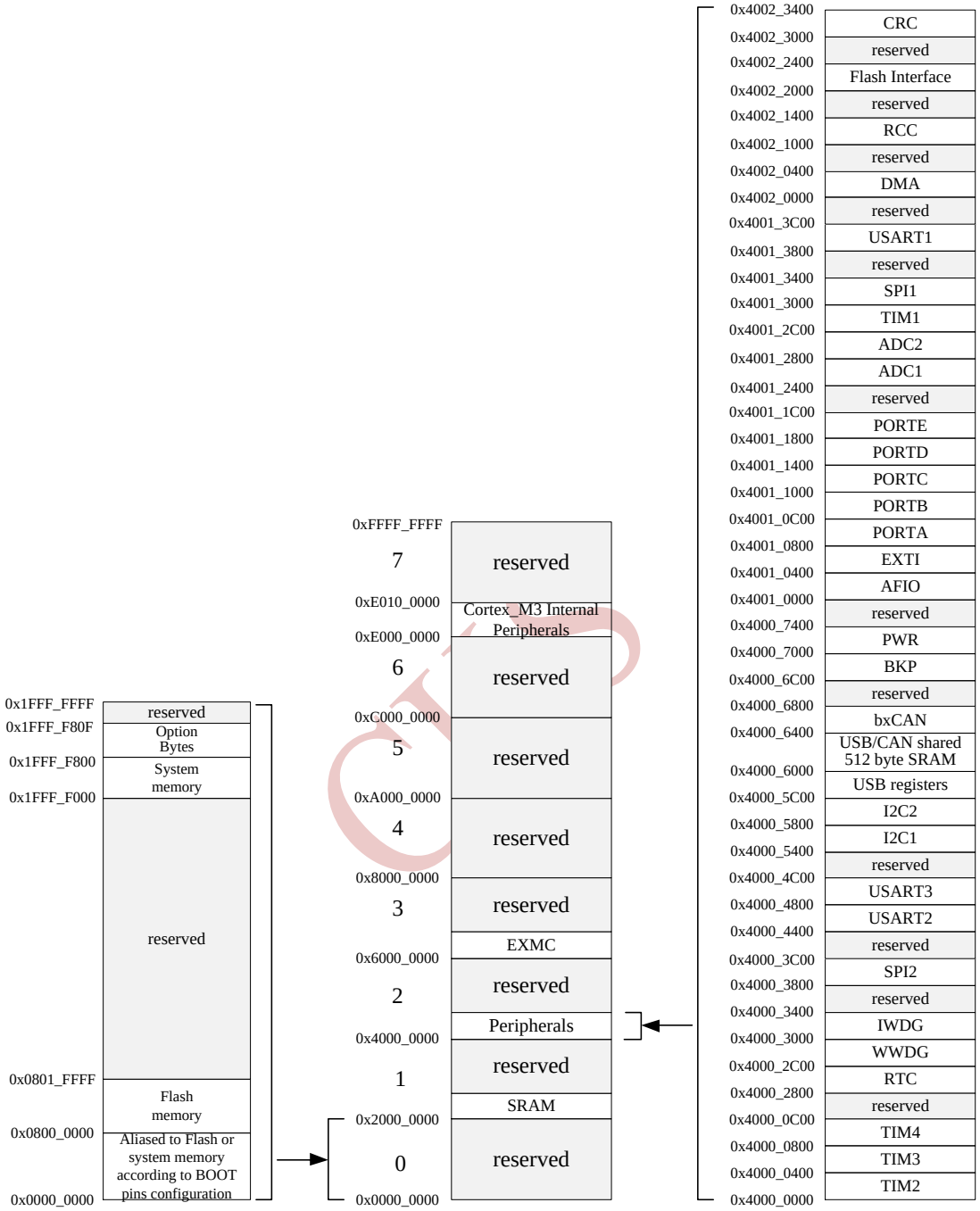


Figure 7. Memory map

5. Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{ss}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 ℃ and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 ℃, V_{DD} = 3.3 V (for the 2V ≤V_{DD}≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 8.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 9.

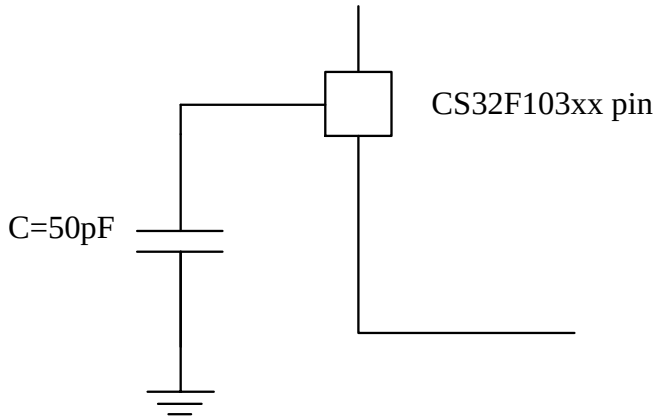


Figure 8. Pin loading conditions

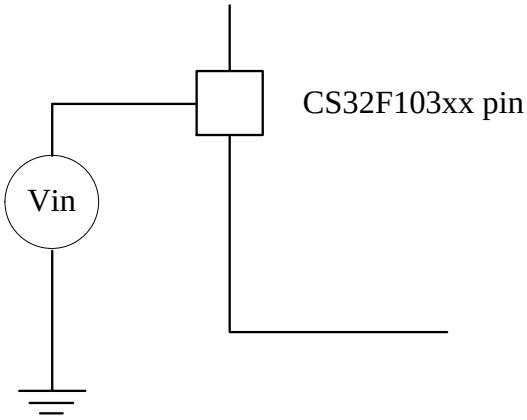


Figure 9. Pin input voltage

5.1.6 Power supply scheme

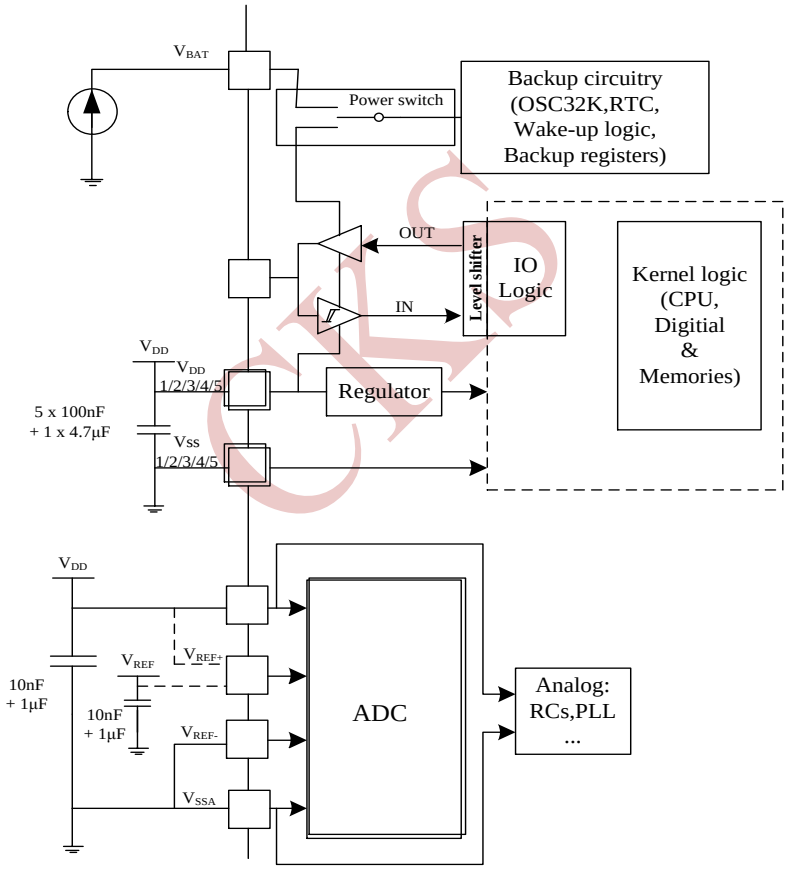


Figure 10. Power supply scheme

In Figure 10, the 4.7µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

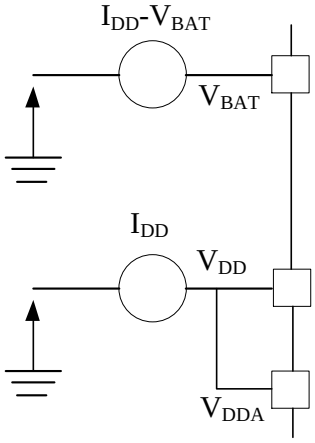


Figure 11. Current consumption measurement scheme

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 5,Table 6 and Table 7 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage(including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS}-0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{EDS(HSBM)}$	Electrostatic discharge voltage(human body model)	See Section 5.3.11		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to Table 6 for the maximum allowed injected current values

Table 6. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines(source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines(sink) (1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$I_{INJ(PIN)}$	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device.

3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to Table 5 for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to Table 5 for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	℃
T_J	Maximum junction temperature	150	℃

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency			0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency			0	36	
f_{PCLK2}	Internal APB2 clock frequency			0	72	
V_{DD}	Standard operating voltage			2	3.6	V
V_{DDA}	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)		2	3.6	
	Analog operating voltage (ADC used)			2.4	3.6	
V_{BAT}	Backup operating voltage			1.8	3.6	
V_{IN}	I/O input voltage	Standard IO		-0.3	V_{DD}+0.3	
		FT IO	2V≤V_{DD}≤3.6V	-0.3	5.5	
			V_{DD}=2V	-0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A=85℃ for suffix 6 or T_A=105 ℃ for suffix 7	LQFP100			434	mW
		LQFP64			444	
		LQFP48			363	
		QFN36			1110	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation		-40	85	℃
		Low power dissipation		-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation		-40	105	
		Low power dissipation		-40	125	
T_J	Junction temperature range	6 suffix version		-40	105	
		7 suffix version		-40	125	

1. When the ADC is used, refer to Table 44.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	μs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in Table 10 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000(rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000(falling edge)	2	2.07	2.16	
		PLS[2:0]=001(rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001(falling edge)	2.09	2.17	2.27	
		PLS[2:0]=010(rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010(falling edge)	2.18	2.27	2.38	
		PLS[2:0]=011(rising edge)	2.38	2.47	2.58	
		PLS[2:0]=011(falling edge)	2.28	2.37	2.48	
		PLS[2:0]=100(rising edge)	2.47	2.57	2.69	
		PLS[2:0]=100(falling edge)	2.37	2.46	2.59	
		PLS[2:0]=101(rising edge)	2.57	2.67	2.79	
		PLS[2:0]=101(falling edge)	2.47	2.56	2.69	
		PLS[2:0]=110(rising edge)	2.66	2.77	2.9	
		PLS[2:0]=110(falling edge)	2.56	2.66	2.8	
		PLS[2:0]=111(rising edge)	2.76	2.86	3.0	
		PLS[2:0]=111(falling edge)	2.66	2.76	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
$V_{PVD/PDR}$		Falling edge	1.8(1)	1.87	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}$(2)				50		mV
$T_{RSTTEMPO}$(2)			1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production

5.3.4 Embedded reference voltage

The parameters given in Table 11 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃<T_A<+105℃	1.16	1.20	1.26	V
		-40℃<T_A<+85℃	1.16	1.20	1.24	
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5.1	17.1	μS
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD}=3V ±100mV			10	mV
T_{Coeff}(2)	Temperature coefficient				100	ppm/℃

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in Figure 11. All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Paramter	Conditions	f_{HCLK}	Max		Unit
				T_A=85℃	T_A=105℃	
I_{DD}	Supply current in Run mode	External clock(2),all peripherals enabled	72MHz	50	50.3	mA
			48 MHz	36.1	36.2	
			36MHz	28.6	28.7	
			24 MHz	19.9	20.1	
			16 MHz	14.7	14.9	
			8 MHz	8.6	8.9	
		External	72MHz	32.8	32.9	

		clock(2),all peripherals disabled	48 MHz	24.4	24.5	
			36MHz	19.8	19.9	
			24 MHz	13.9	14.2	
			16 MHz	10.7	11	
			8 MHz	6.8	7.1	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	**Paramter**	**Conditions**	**f_{HCLK}**	**Max**		**Unit**
				T_A=85℃	**T_A=105℃**	
I_{DD}	Supply current in Run mode	External clock(2),all peripherals enabled	72MHz	48	50	mA
			48 MHz	31.5	32	
			36MHz	24	25.5	
			24 MHz	17.5	18	
			16 MHz	12.5	13	
			8 MHz	7.5	8	
		External clock(2),all peripherals disabled	72MHz	29	29.5	
			48 MHz	20.5	21	
			36MHz	16	16.5	
			24 MHz	11.5	12	
			16 MHz	8.5	9	
			8 MHz	5.5	6	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	**Paramter**	**Conditions**	**f_{HCLK}**	**Max**		**Unit**
				T_A=85℃	**T_A=105℃**	
I_{DD}	Supply current in Sleep mode	External clock(2),all peripherals enabled	72MHz	30	32	mA
			48 MHz	20	20.5	
			36MHz	15.5	16	
			24 MHz	11.5	12	
			16 MHz	8.5	9	
			8 MHz	5.5	6	

		External clock(2),all peripherals disabled	72MHz	7.5	8	
			48 MHz	6	6.5	
			36MHz	5	5.5	
			24 MHz	4.5	5	
			16 MHz	4	4.5	
			8 MHz	3	4	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15.Typical and maximum current consumption in Stop and Standby modes

Symbol	Paramter	Conditions	Typ			Max		Unit
			V_{DD}/V_{BAT} =2.0V	V_{DD}/V_{BAT} =2.4V	V_{DD}/V_{BAT} =3.3 V	T_A=85℃	T_A=105℃	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	22.7	23.2	200	370	μA
		Regulator in Low Power mode, low speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	9.1	9.6	180	340	
	Supply current in Standy mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.4	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.3	3.5	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low speed oscillator and RTC OFF	-	1.5	2.5	4	5	
I_{DD_VBAT}	Backup domain	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9(2)	2.2	

	supply current							

1. Typical values are measured at T_A = 25 ℃.
2. Based on characterization, not tested in production

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$,$f_{ADCCLK}=f_{PCLK2}/4$

Table 16. Typical current consumption in Run mode ,code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enable(2)	All eripherals disable	
I_{DD}	Supply current in Run mode	External clock(3)	72MHz	28.5	13.7	mA
			24MHz	9.7	5.2	
			8MHz	3.8	2.2	

1. Typical values are measures at TA=25℃,VDD=3.3V.
2. Add an additional power consumption of 0.8mA per ADC for the analog part. In application, this consumption occurs only while the ADC is on.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 17.The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  – with all peripherals clocked off
  – with only one peripheral clocked on
  – ambient operating temperature and V_{DD} supply voltage conditions summarized in Table 5.

Table 17. Peripheral current consumption(1)

Peripheral		Typical consumption at 25℃	Unit
APB1	TIM2	1.2	mA
	TIM3	1.2	
	TIM4	0.9	
	SPI2	0.2	
	USART2	0.35	
	USART3	0.35	
	I2C1	0.39	
	I2C2	0.39	

	USB	0.65	
	CAN	0.72	
APB2	GPIO A	0.47	mA
	GPIO B	0.47	
	GPIO C	0.47	
	GPIO D	0.47	
	GPIO E	0.47	
	ADC1(2)	1.81	
	ADC2	1.78	
	TIM1	1.6	
	SPI1	0.43	
	USART1	0.85	

1. f_{HCLK} = 72 MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral.
2. Specific conditions for ADC: f_{HCLK} = 56 MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, f_{ADCCLK} = f_{APB2}/4, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in Table 18 result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table 8.

Table 18. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{HSE_ext}	User external clock source frequency(1)		1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		2.2	-	3.3	V
V_{HSEl}	OSC_IN input pin low level voltage		0	-	2.2	
$T_{w(HSE)}$ $T_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
Ducy(HSE)	Duty cycle		45	50	55	%
I_L	OSC_IN input leakage current	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$	-	0.3	±1	μA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in Table 19 result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table 8.

Table 19. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)		-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		1.8	-	3.3	V
V_{LSEl}	OSC32_IN input pin low level voltage		V_{SS}	-	0.3 V_{DD}	
$T_{w(LSE)}$ $T_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns

$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
Ducy(LSE)	Duty cycle		30	50	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$	-	-0.4	±1	μA

1. Guaranteed by design, not tested in production.

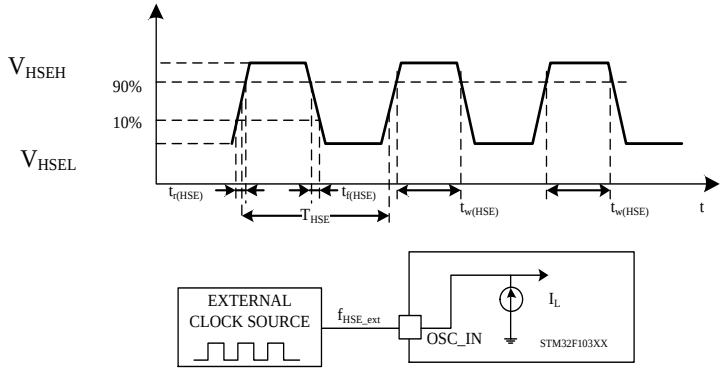


Figure 12. High-speed external clock source AC timing diagram

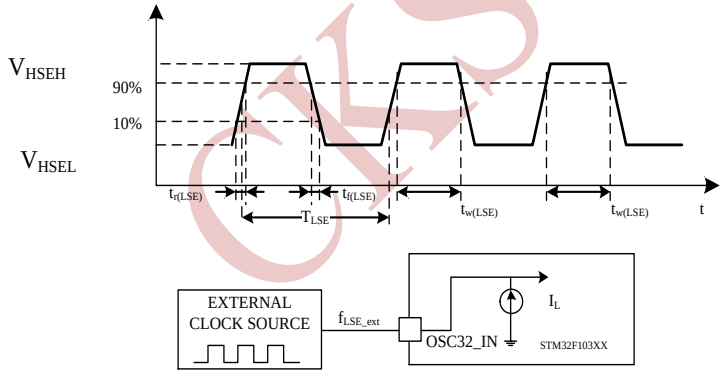


Figure 13. Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 20. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 20. HSE 4-16MHz oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	16	MHz
R_F	Feedback resistor		-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_s=30Ω	-	30	-	pF

i_2	HSE driving current	V_{DD}=3.3V，V_{IN}=V_{SS} with 30pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{su(HSE)}$(4)	startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 14). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

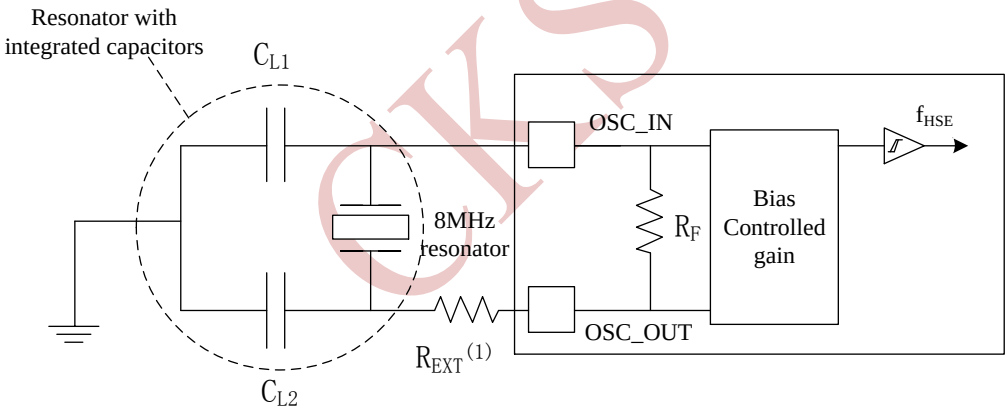


Figure 14. Typical application with an 8 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 21. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 21. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1) (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor			-	5	-	MΩ
C	Recommended load capacitance versus	Rs=30KΩ		-	-	15	pF

	equivalent serial resistance of the crystal (RS)						
I_2	LSE driving current	V_{DD}=3.3V V_{IN}=V_{SS}		-	-	1.4	μA
g_m	Oscillator transconductance			5	-	-	μA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A=50℃	-	1.5	-	s
			T_A=25℃	-	2.5	-	
			T_A=10℃	-	4	-	
			T_A=0℃	-	6	-	
			T_A=-10℃	-	10	-	
			T_A=-20℃	-	17	-	
			T_A=-30℃	-	32	-	
			T_A=-40℃	-	60	-	

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and $C_{L2,}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. Load capacitance C_L has the following formula: C_L = C_{L1} x C_{L2} / (C_{L1} + C_{L2}) + C_{stray} where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance C_L ⩽7 pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

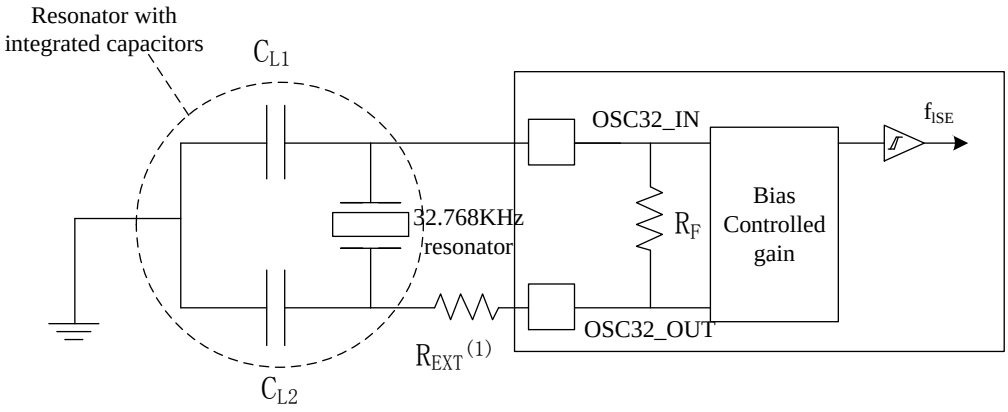


Figure 15. Typical application with a 32.768 kHz crystal

5.3.7 Internal clock source characteristics

The parameters given in Table 22 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

High-speed internal (HSI) RC oscillator

Table 22. HSI oscillator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency			-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle			45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(1)		-	-	1(2)	
		Factory-calibrated(3)(4)	T_A=--40 to 105℃	-2	-	2.5	
			T_A=-10 to 85℃	-1.5	-	2.2	
			T_A=0 to 70℃	-1.3	-	2	
			T_A=25℃	-1.1	-	1.8	
$T_{su(HSI)}$(3)	HSI oscillator startup time			1	-	2	μs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption			-	80	100	μA

1. Refer to application note AN2868 'CKS32F10xxx internal RC oscillator (HSI) calibration' available from the ST website www.st.com.
2. Guaranteed by design, not tested in production.
3. Based on characterization, not tested in production.
4. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 23. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	μs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.65	1.2	μA

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in Table 24 is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

Table 24. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	μs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	2.6	
	Wakeup from Stop mode (regulator in low power mode)	5.1	

$t_{WUSTDBY}$(1)	Wakeup from Standby mode	52	

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in Table 25 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

Table 25. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	72	MHz
t_{LOCK}	PLL lock time	-	43	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

4.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 ℃ unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A=-40 to +105℃	-	-	20	μs
t_{ERASE}	Page (1KB) erase time	T_A=-40 to +105℃	-	-	2	ms
t_{ME}	Mass erase time	T_A=-40 to +105℃	-	-	10	
I_{DD}	Supply current	Read mode f_{HCLK}=72MHz with 2 wait states,V_{DD}=3.3V	-	-	21.6	mA
		Write/Erase modes f_{HCLK}=72MHz, V_{DD}=3.3V	-	-	3	
		Power-down mode/Halt, V_{DD}=3.0 to 3.6V	-	-	1	μA

1. Guaranteed by design, not tested in production.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max(1)	
N_{END}	Endurance	T_A=-40 to +85℃(6 suffix version)	100	-	-	kcycle
		T_A=-40 to +105℃(7 suffix version)				
t_{RET}	Data retention	T_A=-40 to +85℃	10	-	-	years

1. Based on characterization, not tested in production.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 28. They are based on the EMS levels and classes defined in application note AN1709.

Table 28. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=3.3V,T_A=+25℃, f_{HCLK}=72MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=3.3V,T_A=+25℃, f_{HCLK}=72MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 29. EMI characteristics

Symbol	Parameter	Condition	Monitored frequency band	Max(f_{HSE}/f_{HCLK})		Uint
				8/48MHz	8/72MHz	
S_{EMI}	Peak level	V_{DD}= 3.3 V，T_A= 25 ℃，LQFP100package compliant with IEC 61967-2	0.1~30MHz	12	12	dBμV
			30~130MHz	22	19	
			130MHz~1GHz	23	29	
			SAM EMI Levle	4	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts ×(n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 30. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25℃ conforming to JESD22-A14	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=+25℃ conforming to JESD22-C1011	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A=+105℃ conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device

characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in Table 32

Table 32. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics General input/output characteristics

Unless otherwise specified, the parameters given in Table 33are derived from tests performed under the conditions summarized in Table 8. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	$0.28\times(V_{DD}-2V)+0.8V$	V
		IO FT(3) input low level voltage	-	-	$0.32\times(V_{DD}-2V)+0.75V$	
		All I/Os except BOOT0	-	-	$0.35\ V_{DD}$	
V_{IH}	High level input voltage	Standard IO input high level voltage	$0.41\times(V_{DD}-2V)+1.3V$	-	-	
		IO FT(3) input high level voltage	2	-	-	
		All I/Os except BOOT0	$0.65\ V_{DD}$	-	-	
V_{hys}	Standard IO Schmitt trigger voltage		200	-	-	mV

	hysteresis(4)					
	IO FT Schmitt trigger voltage hysteresis(4)		5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current(6)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	±1	μA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN}=V_{SS}$	30	40	50	KΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN}=V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation
2. Tested in production
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see Table 6).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see Table 6).

Output voltage levels

Unless otherwise specified, the parameters given in Table 34 are derived from tests performed under

ambient temperature and V_{DD} supply voltage conditions summarized in Table 8. All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(2) I_{IO}=+8mA 2.7V<V_{DD}<3.6V		0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(2) I_{IO}=+8mA 2.7V<V_{DD}<3.6V		0.4	
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+20mA 2.7V<V_{DD}<3.6V		1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-1.3		
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+6mA 2 V<V_{DD}<2.7V		0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.4		

1. The IIO current sunk by the device must always respect the absolute maximum rating specified in Table 6 and the sum of IIO (I/O ports and control pins) must not exceed IVSS
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52
3. The IIO current sourced by the device must always respect the absolute maximum rating specified in Table 6 and the sum of IIO (I/O ports and control pins) must not exceed IVDD.
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 16 and Table 35, respectively.

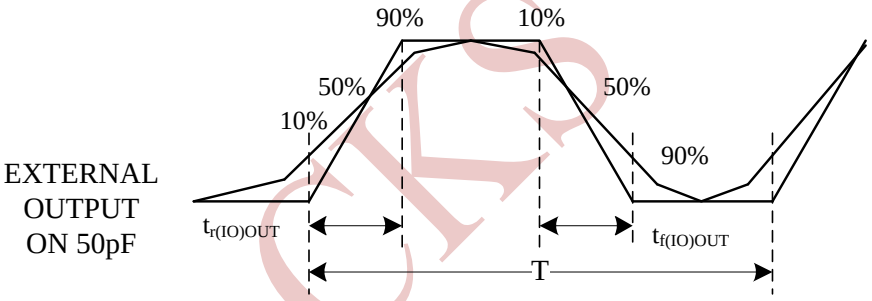
Unless otherwise specified, the parameters given in Table 35 are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

Table 35. I/O AC characteristics(1)

MODEx[1:0] Bit value	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L=50pF,V_{DD}=2V to 3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L=50pF,V_{DD}=2V to 3.6V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L=50pF,V_{DD}=2V to 3.6V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L=50pF,V_{DD}=2V to 3.6V	-	25(3)	ns

	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$ $t_{f(IO)out}$	Maximum frequency(2) Output high to low level fall time	C_L=30pF,V_{DD}=2.7V to 3.6V	-	50	MHz
			C_L=50pF,V_{DD}=2.7V to 3.6V	-	30	
			C_L=30pF,V_{DD}=2V to2.7V	-	20	
	$f_{max(IO)out}$ $t_{f(IO)out}$	Maximum frequency(2) Output high to low level fall time	C_L=30pF,V_{DD}=2.7V to 3.6V	-	5(3)	ns
			C_L=50pF,V_{DD}=2.7V to 3.6V	-	8(3)	
			C_L=30pF,V_{DD}=2V to2.7V	-	12(3)	
	$f_{max(IO)out}$	Maximum frequency(2)	C_L=30pF,V_{DD}=2.7V to 3.6V	-	5(3)	
			C_L=50pF,V_{DD}=2.7V to 3.6V	-	8(3)	
			C_L=30pF,V_{DD}=2V to2.7V	-	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the CKS32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in Figure 16.
3. Guaranteed by design, not tested in production



Maximum frequency is achieved if (t_r+t_f)≤2/3T and if the duty cycle is (45-55%) when loaded by 50pF

Figure 16. I/O AC characteristics definition

5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 33).

Unless otherwise specified, the parameters given in Table 36 are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 8.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse		-	-	100	ns

$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

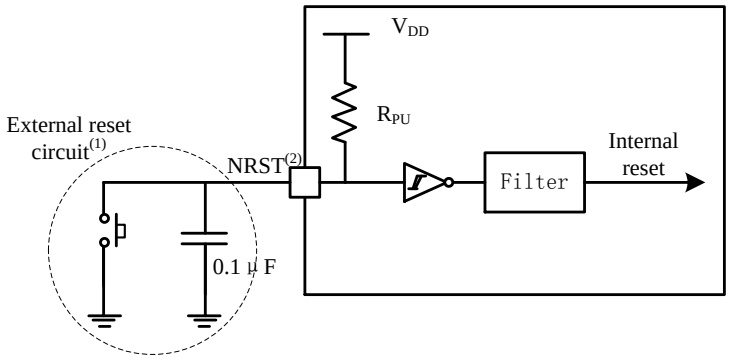


Figure 17. Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 36. Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in Table 37 are guaranteed by design.

Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 37. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=72MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK/2}$	MHz
		$f_{TIMxCLK}$=72MHz	0	36	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=72MHz	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count		-	65536×65539	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=72MHz	-	59．6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I^2C interface characteristics

The CKS32F103xx performance line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not ‘true’ open-drain. When configured as open-drain, the PMOS connected between the I/O pin and

V_{DD} is disabled, but is still present.

The I^2C characteristics are described in Table 38.Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 38. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6		
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1 C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I^2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

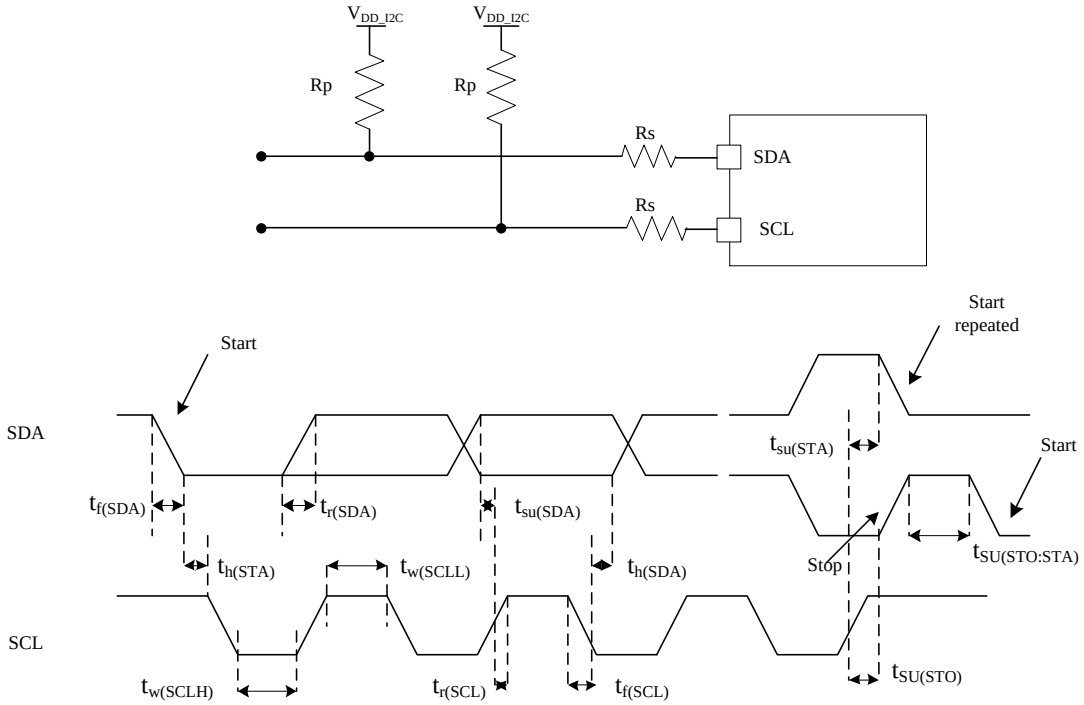


Figure 18. I²C bus AC waveforms and measurement circuit

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. R_s = Series protection resistors, R_p = Pull-up resistors, V_{DD_I2C} = I²C bus supply.

Table 39. SCL frequency (f_{PCLK1}= 36 MHz,V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL}(KHz)	I2C_CCR value
	R_p=4.7KΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. RP = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed±2%. These variations depend on the accuracy of the external components used to design the application

SPI interface characteristics

Unless otherwise specified, the parameters given in Table 40 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 8. Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 40. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SPI clock frequency	Master mode	-	18	MH
		Slave mode	-	18	z
$t_{r(SCK)}$	SPI clock rise and fall	Capacitive load:C=30pF	-	8	ns

$t_{f(SCK)}$	time				
$Ducy_{(SCK)}$	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK}=36MHz,presc=4	50	60	
$t_{su(MI)}$(1) $t_{su(SI)}$(1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(1)		Slave mode	4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK}=20MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)		5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

1. Based on characterization, not tested in production
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

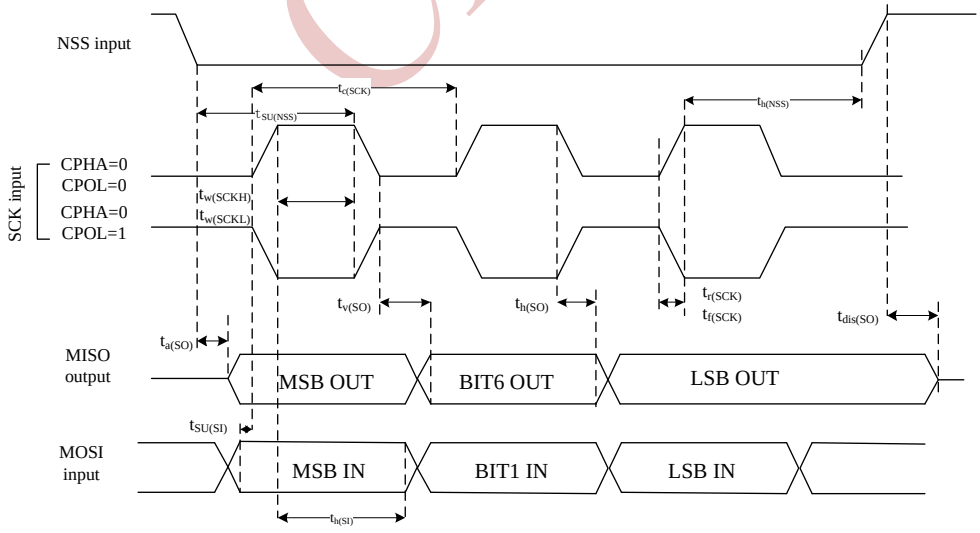


Figure 19. SPI timing diagram - slave mode and CPHA = 0

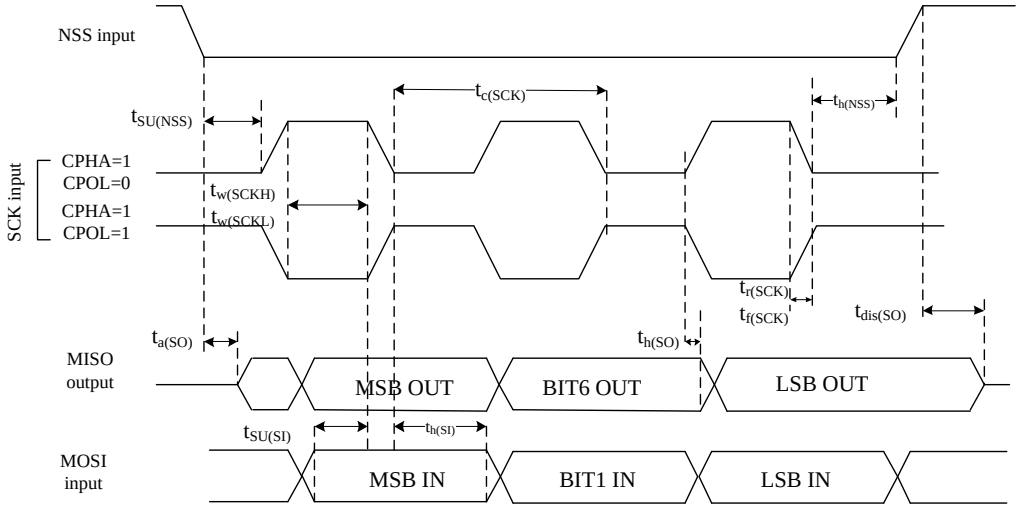


Figure 20. SPI timing diagram - slave mode and CPHA = 1(1)

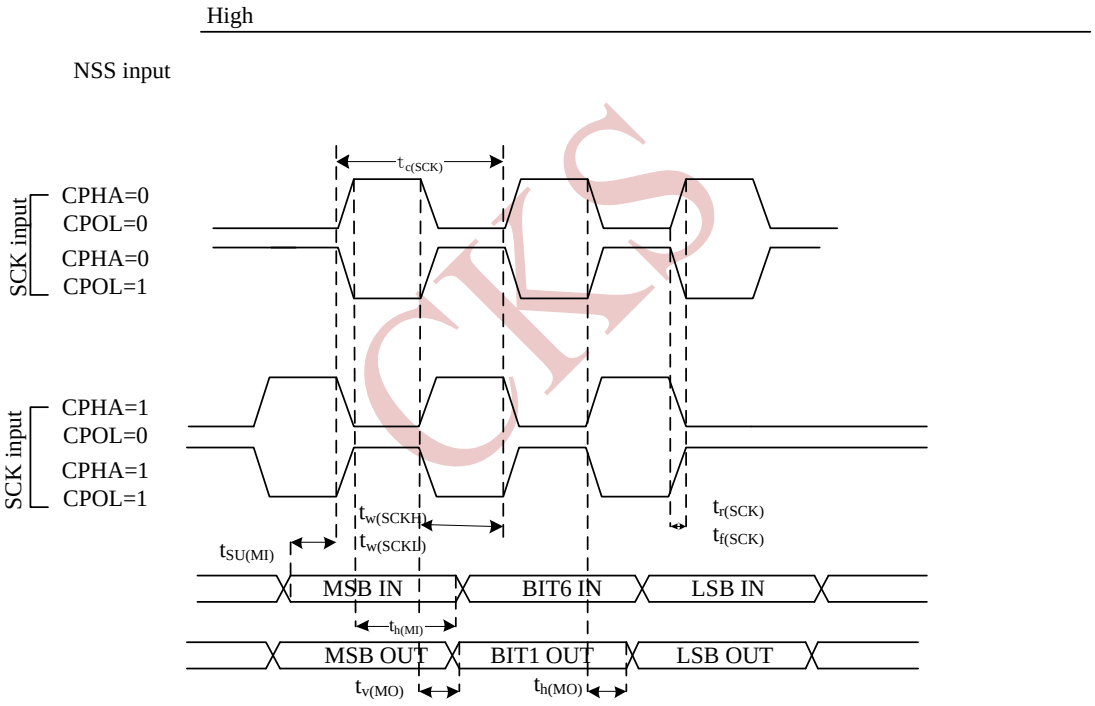


Figure 21. SPI timing diagram - master mode(1)

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 41. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 42. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP,USBDM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 13.5kΩ to 3.6V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15kΩ toV_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential。
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulledup with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The CKS32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers

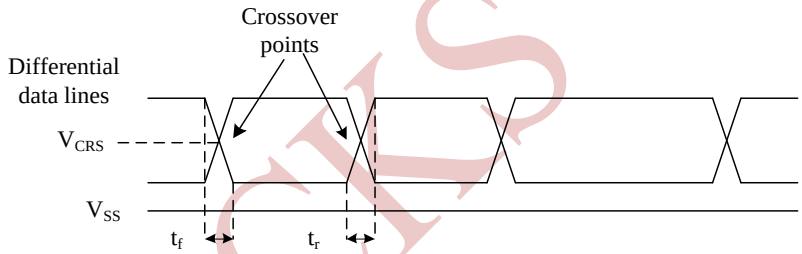


Figure 22. USB timings: definition of data signal rise and fall time

Table 43. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Driver characteristics					
t_r	Rise time(2)	CL ≤ 50pF	4	20	ns
t_f	Fall time(2)	CL ≤ 50pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal.

5.3.17 CAN (controller area network) interface

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.18 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 44 are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in Table 8.

Note: It is recommended to perform a calibration after each power-up.

Table 44. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4	-	3.6	V
V_{REF+}	Positive reference voltage		2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	μA
f_{ADC}	ADC clock frequency		0.6	-	14	MHz
f_S(2)	Sampling rate		0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC}=14MHz	-	-	823	KHz
			-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range		0(V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance		-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance		-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC}=14MHz	5.9			μs
			8.3			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC}=14MHz	-	-	0.214	μs
			-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC}=14MHz	-	-	0.143	μs
			-	-	2(4)	$1/f_{ADC}$
t_s(2)	Sampling time	f_{ADC}=14MHz	0.107	-	17.1	μs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	μs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC}=14MHz	1	-	18	μs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. In devices delivered in QFN and LQFP packages, V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in Table 44.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 45. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s(cycles)	t_s(μs)	R_{AIN}max(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4

28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Based on characterization, not tested in production

Table 46. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2}=56MHz,	±1.3	±2	LSB
EO	Offset error	f_{ADC}=14MHz,R_{AIN}<10 kΩ,	±1	±1.5	
EG	Gain error	V_{DDA}=3V to 3.6V,T_A=25℃	±0.5	±1.5	
ED	Differential linearity error	Measurements made after	±0.7	±1	
EL	Integral linearity error	ADC calibration	±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\sum I_{INJ(PIN)}$ in Section 5.3.12 does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Table 47. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2}=56MHz,	±2	±5	LSB
EO	Offset error	f_{ADC}=14MHz,R_{AIN}<10 kΩ,	±1.5	±2.5	
EG	Gain error	V_{DDA}=2.4V to 3.6V	±1.5	±3	
ED	Differential linearity error	Measurements made after	±1	±2	
EL	Integral linearity error	ADC calibration	±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\sum I_{INJ(PIN)}$ in Section 5.3.12 does not affect the ADC accuracy.
4. Based on characterization, not tested in production

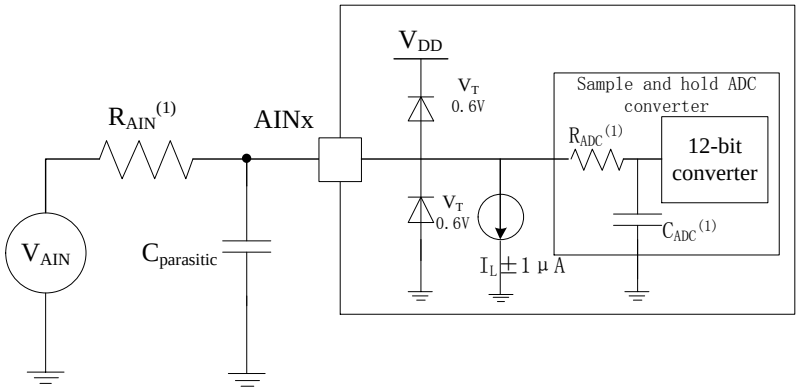


Figure 23. Typical connection diagram using the ADC

General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 24 and Figure 25, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

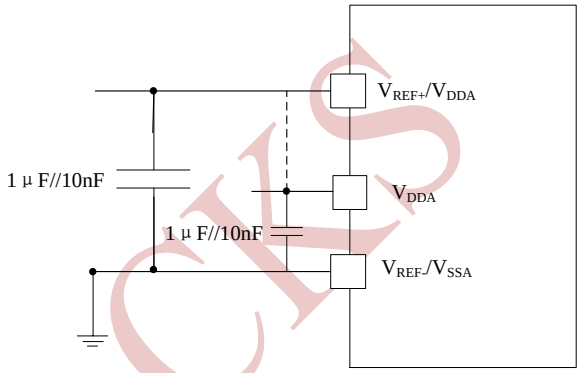


Figure 24. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

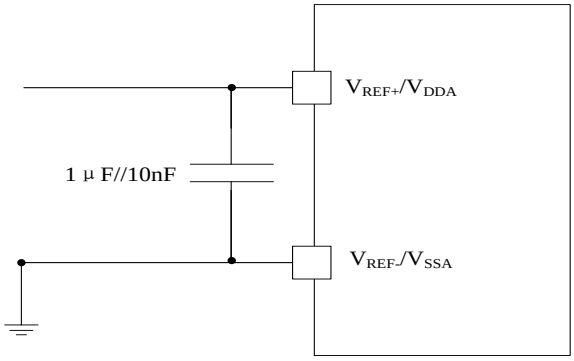


Figure 25. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 Temperature sensor characteristics Table 50. TS characteristics

Table 48. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	℃

$Avg\_Slope^{(1)}$	Average slope	4.0	4.3	4.6	mV/℃
$V_{25}^{(1)}$	Voltage at 25℃	1.34	1.40	1.52	V
$t_{START}^{(2)}$	Startup time	4	-	10	μs
$T_{S\_temp}^{(2)(3)}$	ADC sampling time when reading the temperature	-	-	17.1	μs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 .Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, CS offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance.

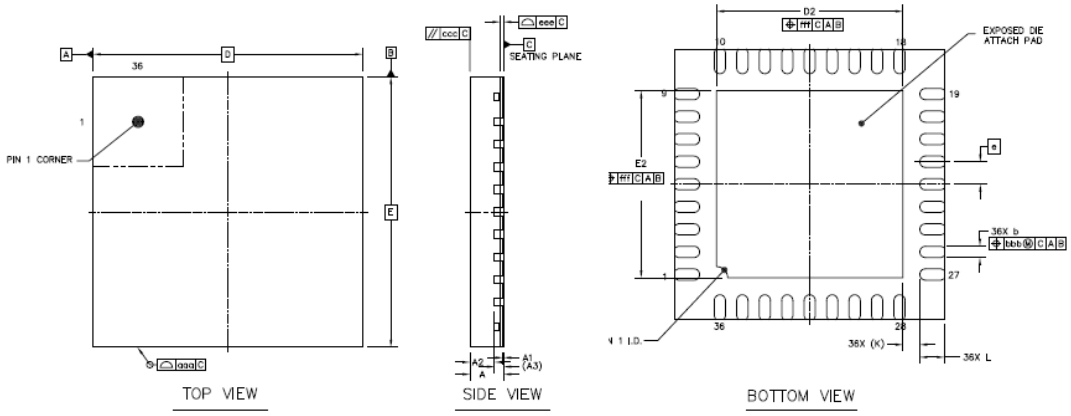


Figure 26. QFN36,package outline

Table 49. QFN36,package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	6 BSC		
E	6 BSC		
e	0.5 BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
K	0.375 REF		
L	0.45	0.55	0.65
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

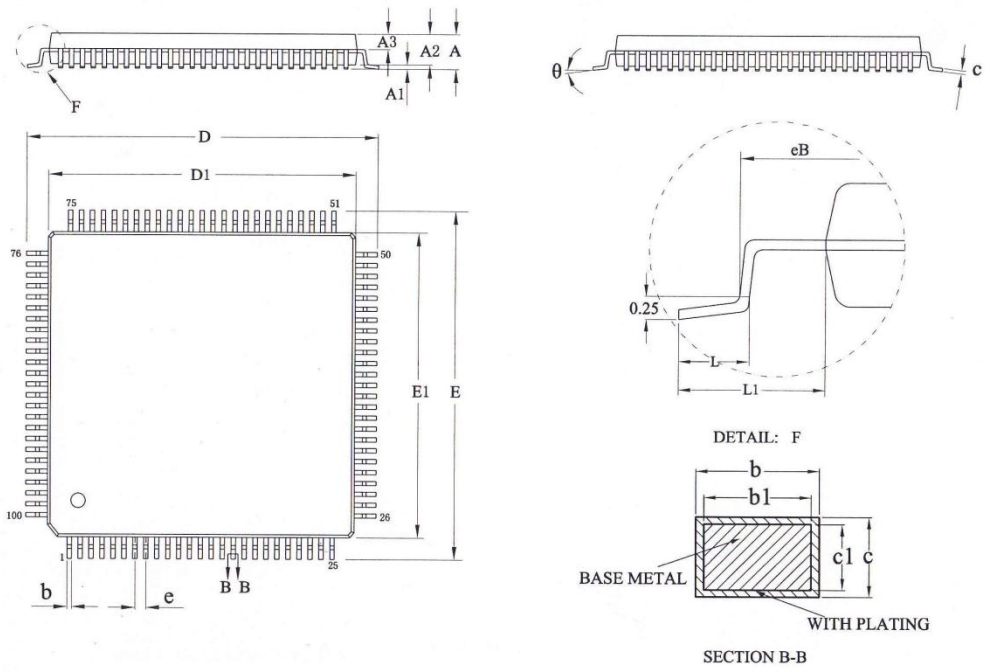


Figure 27. LQPF100, 100-pin low-profile quad flat package outline

Table 50. LQPF100, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Min
A			1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.20
eB	15.05	-	15.35
e	0.50 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0	-	7 °

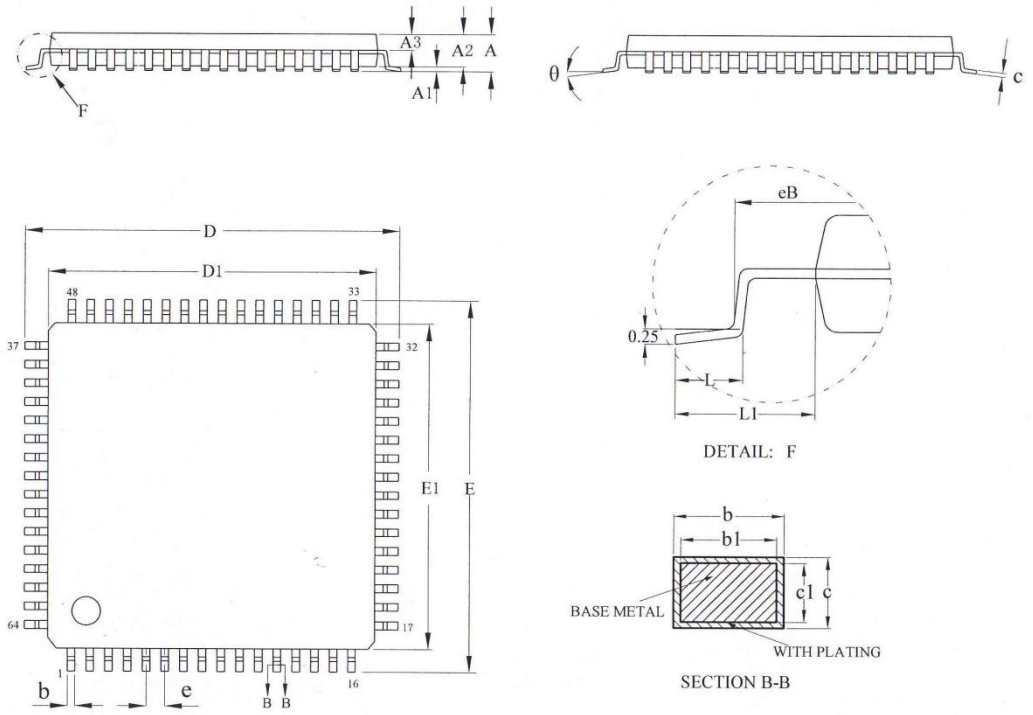


Figure 28. LQFP64, 64-pin low-profile quad flat package outline(1)

Table 51. LQFP64, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Min
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.25	-	11.45
E1	9.90	10.00	10.10
e	0.50 BSC		
θ	0 °	-	7 °
L	0.45	-	0.75
L1	1.00 REF		

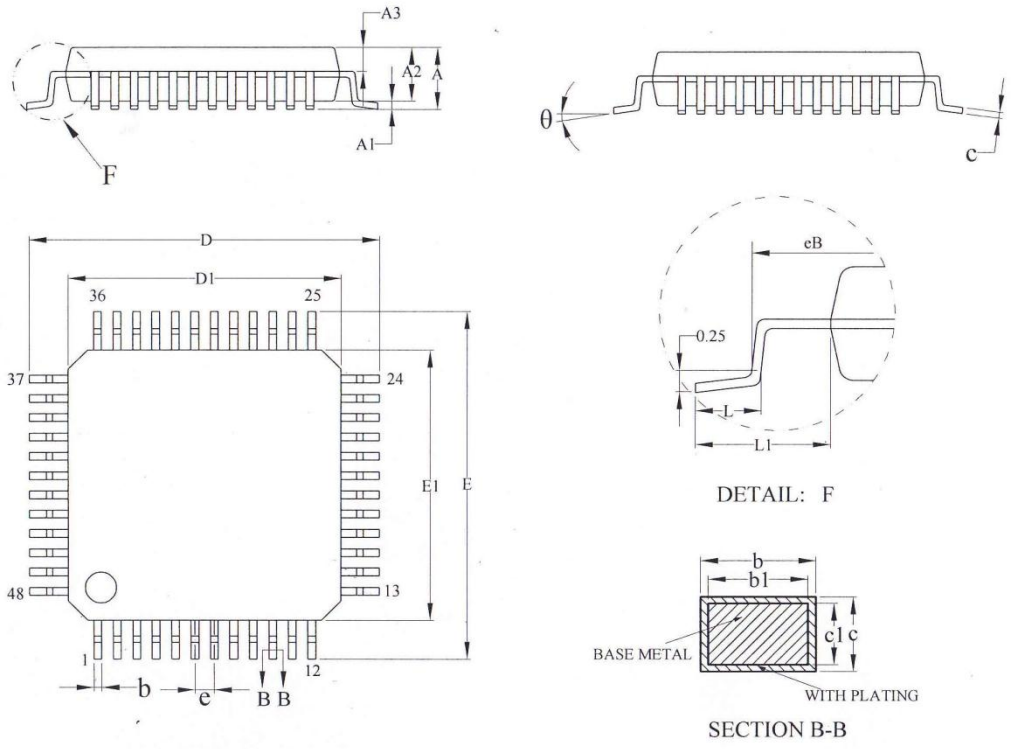


Figure 29. LQFP48, 48-pin low-profile quad flat package outline(1)

Table 52. LQFP48, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Min
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.20
eB	8.10	-	8.25
e	0.50 BSC		
L	0.40	-	0.65
L1	1.00 REF		
k	0	-	7 °

6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given inTable 8.
The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_{J\ max} = T_{A\ max} + (P_{D\ max} \times \Theta_{JA})$$

Where:

- $T_{A\ max}$ is the maximum ambient temperature in℃,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in℃/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_{D\ max} = P_{INT\ max} + P_{I/O max}$),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:
$P_{I/O}$ max = Σ ($V_{OL} \times I_{OL}$) + Σ(($V_{DD} - V_{OH}$) × I_{OH}),
taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 53. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	℃/W
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air).

6.2.2 Selecting the product temperature range

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.
As applications do not commonly use the CKS32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.