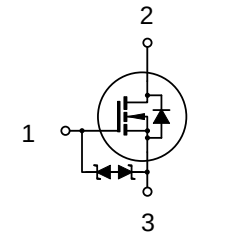
9A, 900V N-CHANNEL MOSFET

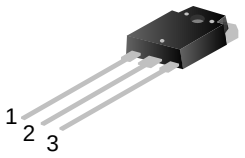
DESCRIPTION

SVF3878PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



1.Gate 2.Drain 3.Source



TO-3P

FEATURES

- 9A, 900V, $R_{DS(on)\ (typ.)}$=1. 0Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF3878PN	TO-3P	3878	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_A=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	900	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	9.0	A
	T_C=100°C		5.7	
Drain Current Pulsed		I_{DM}	27.0	A
Power Dissipation (T_C=25°C)		P_D	150	W
-Derate above 25°C			1.2	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	966	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{θJC}$	0.83	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{θJA}$	50	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	900	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=900V, V_{GS}=0V	--	--	100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±10.0	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.5	--	4.5	V
On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.5A	--	1.0	1.28	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	2009	--	pF
Output Capacitance	C_{oss}		--	208	--	
Reverse Transfer Capacitance	C_{rss}		--	47	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V, R_G=25Ω, I_D=4.0A (Note2,3)	--	22	--	ns
Turn-on Rise Time	t_r		--	28	--	
Turn-off Delay Time	$t_{d(off)}$		--	84	--	
Turn-off Fall Time	t_f		--	30	--	
Total Gate Charge	Q_g	V_{DD}=450V, V_{GS}=10V, I_D=9.0A (Note 2,3)	--	68	--	nC
Gate-Source Charge	Q_{gs}		--	10	--	
Gate-Drain Charge	Q_{gd}		--	39	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9.0	A
Pulsed Source Current	I_{SM}		--	--	27	
Diode Forward Voltage	V_{SD}	I_S=9.0A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=9.0A, V_{GS}=0V, dI_F/dt=100A/μS (Note2)	--	715	--	ns
Reverse Recovery Charge	Q_{rr}		--	6.5	--	μC

Notes:

1. L=30mH, I_{AS}=7.70A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

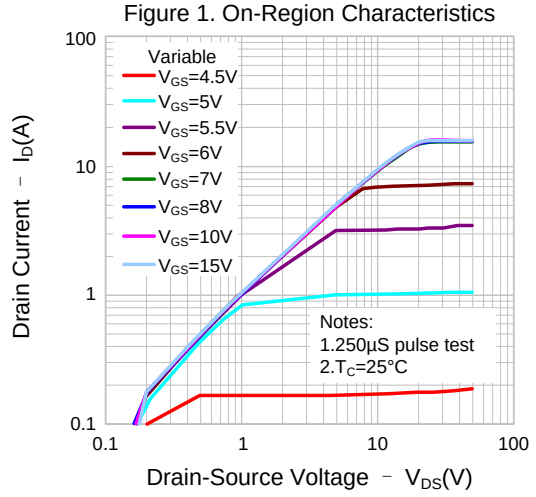


Figure 2. Transfer Characteristics

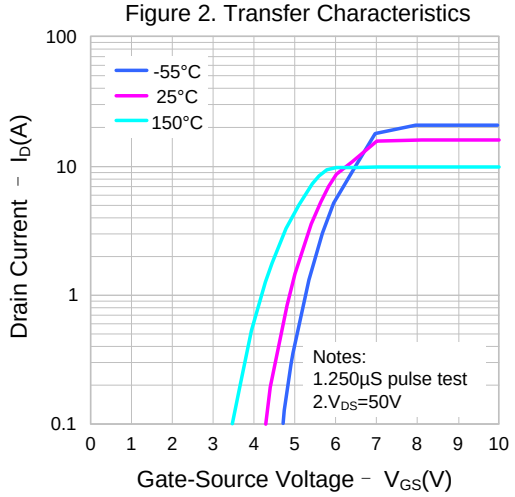


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

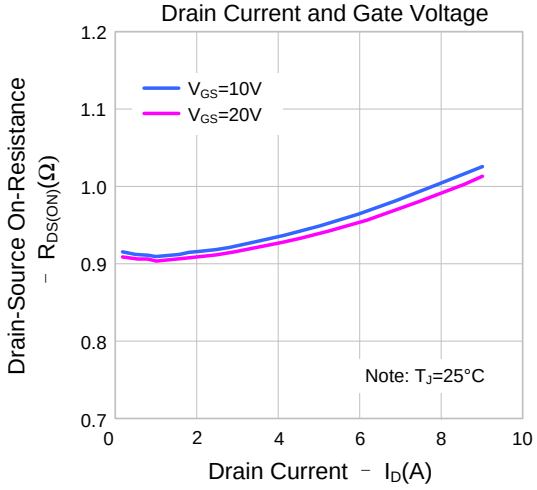


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

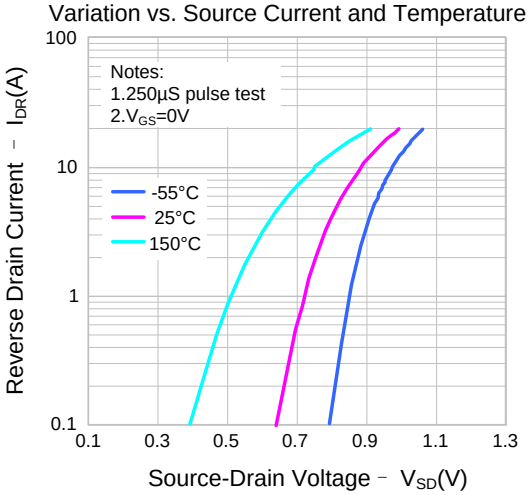


Figure 5. Capacitance Characteristics

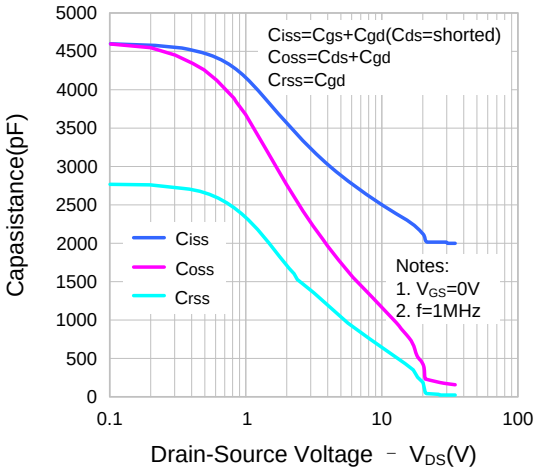
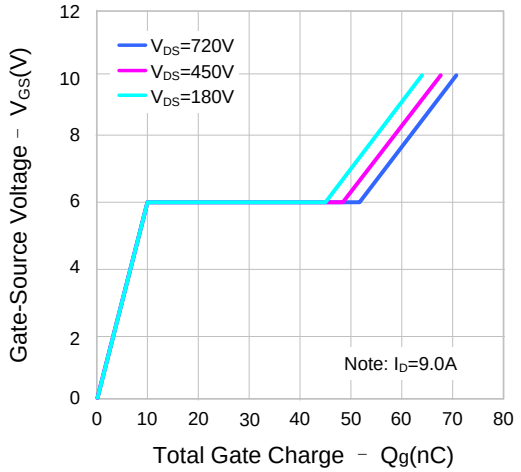


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

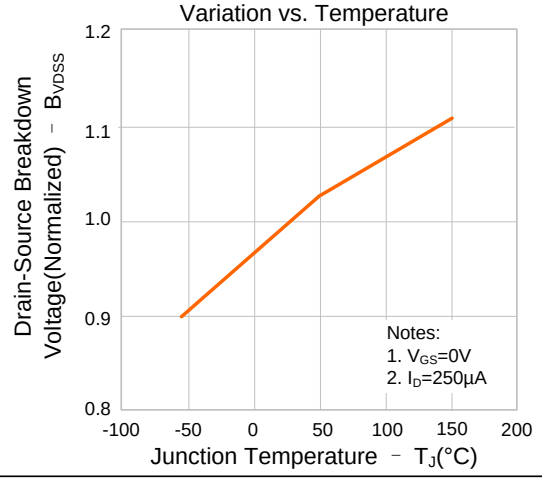


Figure 8. On-resistance Variation vs. Temperature

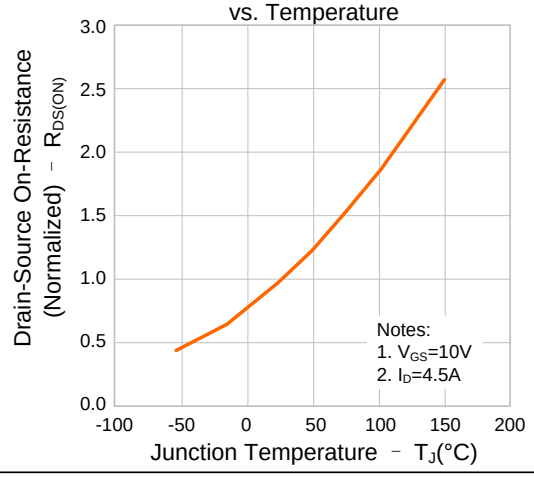


Figure 9. Max. Safe Operating Area

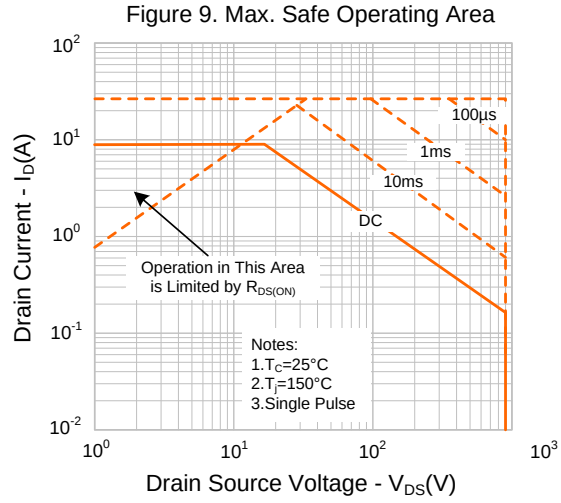
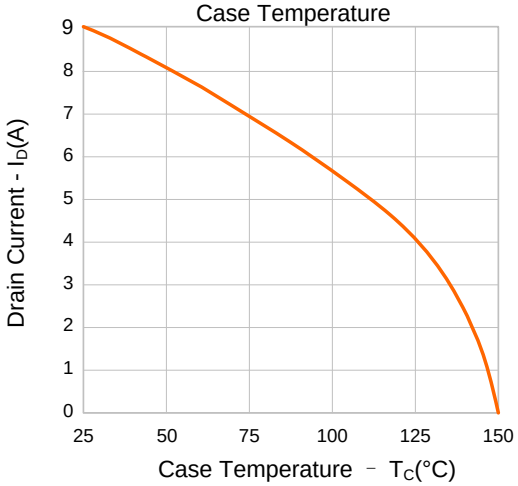
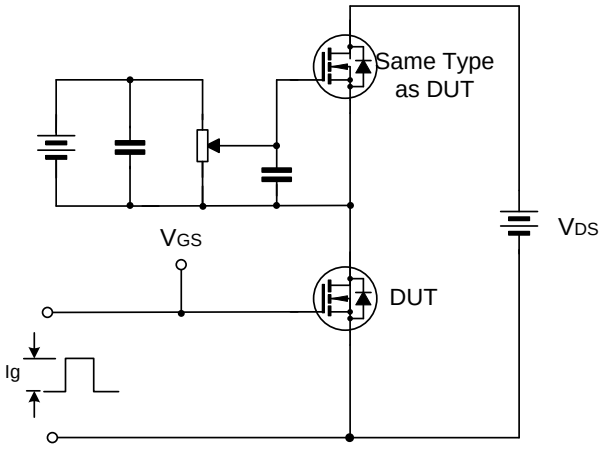


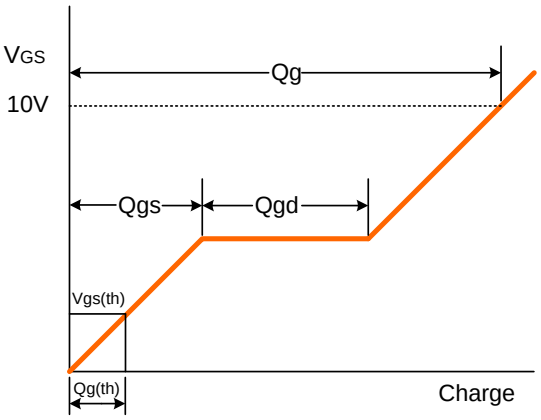
Figure 10. Maximum Drain Current vs. Case Temperature



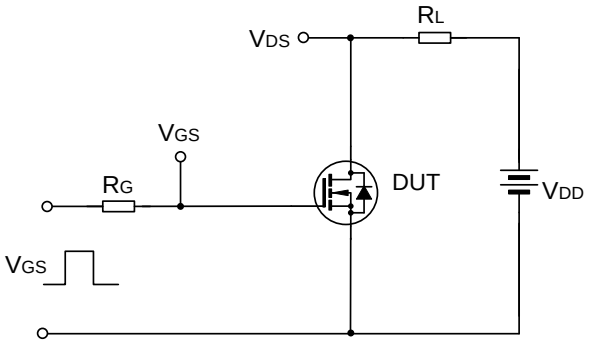
TYPICAL TEST CIRCUIT

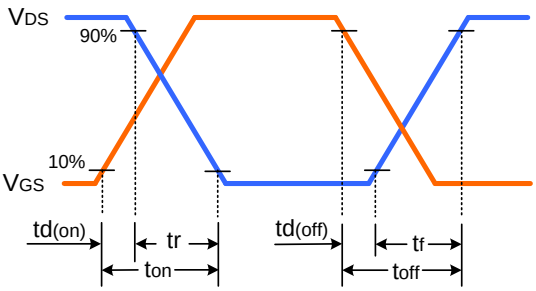
Gate Charge Test Circuit & Waveform



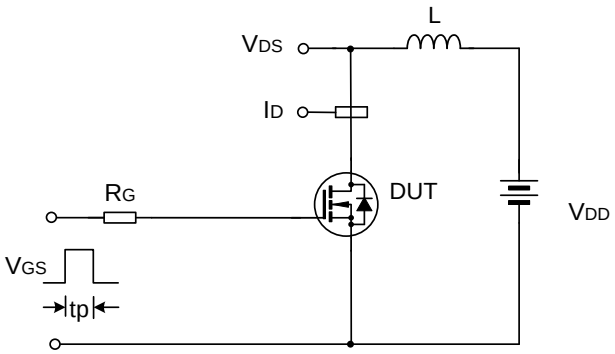


Resistive Switching Test Circuit & Waveform

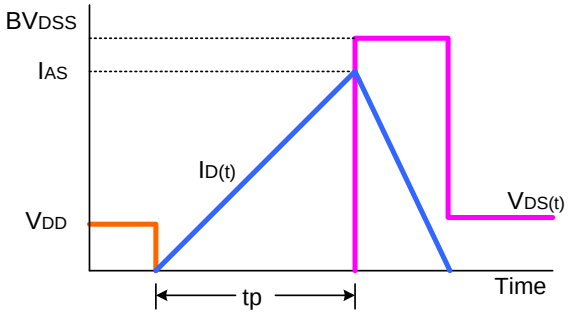




Unclamped Inductive Switching Test Circuit & Waveform

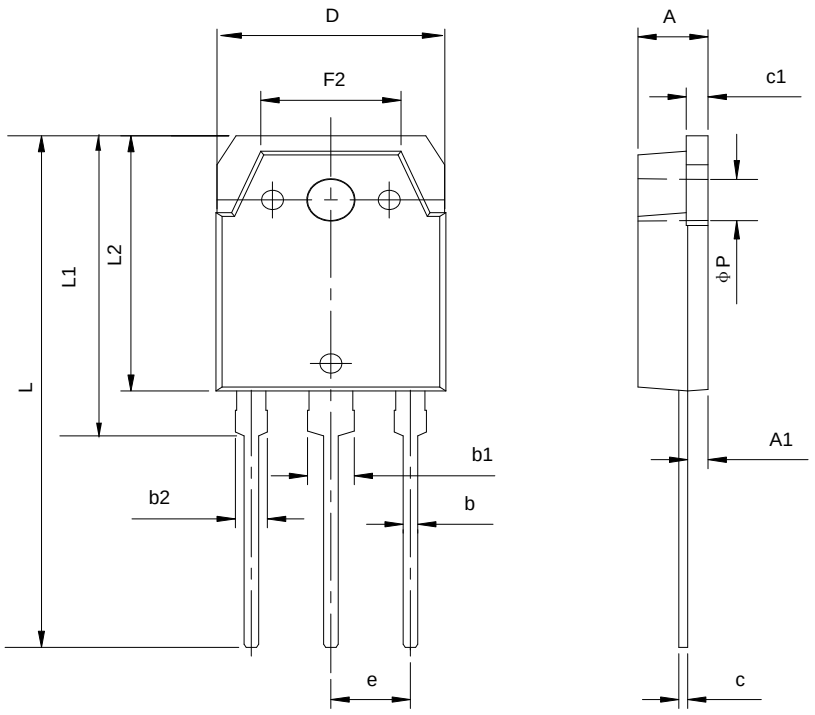


$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



PACKAGE OUTLINE

TO-3P **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.4	—	5.2
c1	1.2	—	1.8
A1	1.2	—	2.0
b	0.7	1.0	1.3
b1	2.7	3.0	3.3
b2	1.7	2.0	2.3
D	15.0	15.5	16.0
c	0.4	0.6	0.8
F2	8.5	—	10.0
e	5.45 TYP		
L1	22.6	—	23.6
L	39.0	—	41.5
L2	19.5	—	21.0
P	3.0	—	3.4

Important notice :

1. **The instructions are subject to change without notice!**
2. **Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.**
3. **Our products are consumer electronic products or the other civil electronic products.**
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Rev.: 1.1

Revision History:

1. Update electrical diagram and typical test circuit
2. Update curve template
3. Update package outline
4. Update important notice

Rev.: 1.0

Revision History:

1. First release