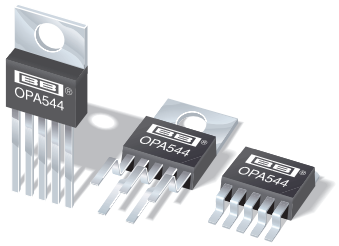
BURR - BROWN®



OPA544

High-Voltage, High-Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE: ±10 to ±35V
- SLEW RATE: 8V/µs
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: I_B = 100pA max
- 5-LEAD TO-220 PLASTIC PACKAGE
- 5-LEAD SURFACE MOUNT PACKAGE

APPLICATIONS

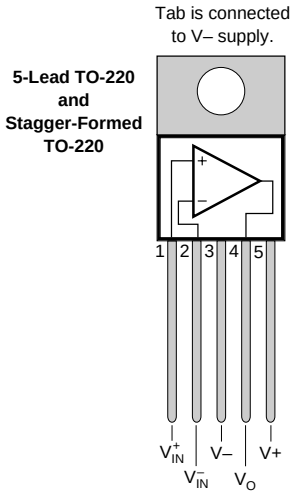
- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

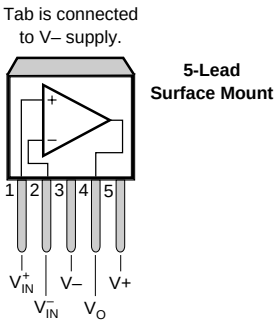
DESCRIPTION

The OPA544 is a high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. High performance FET op amp circuitry and high power output stage are combined on a single monolithic chip.

The OPA544 is protected by internal current limit and thermal shutdown circuits.

The OPA544 is available in industry-standard 5-lead TO-220 and 5-lead surface-mount power packages. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. It is specified for operation over the extended industrial temperature range, –40°C to +85°C.





International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1250B
Printed in U.S.A. September, 1995

SBOS038

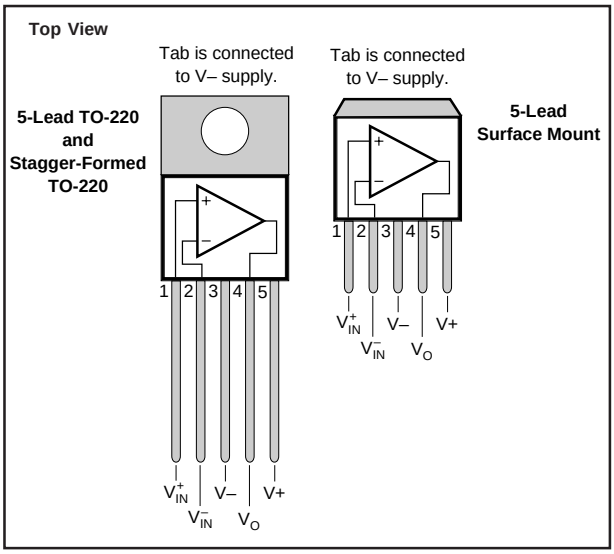
SPECIFICATIONS

At T_{CASE} = +25°C, V_S = ±35V, unless otherwise noted.

PARAMETER	CONDITION	OPA544T, OPA544T-1, OPA544F MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5	mV
vs Temperature	Specified Temperature Range		±10		µV/°C
vs Power Supply	V_S = ±10V to ±35V		±10	±100	µV/V
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		±15	±100	pA
vs Temperature			See Typical Curve		
Input Offset Current	V_{CM} = 0V		±10	±100	pA
NOISE					
Input Voltage Noise					
Noise Density, f = 1kHz			36		nV/√Hz
Current Noise Density, f = 1kHz			3		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range, Positive	Linear Operation	(V+) –6	(V+) –4		V
Negative	Linear Operation	(V–) +6	(V–) +4		V
Common-Mode Rejection	$V_{CM} = \pm V_S$ –6V	90	106		dB
INPUT IMPEDANCE					
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±30V, R_L = 1kΩ	90	103		dB
FREQUENCY RESPONSE					
Gain Bandwidth Product	R_L = 15Ω		1.4		MHz
Slew Rate	60Vp-p, R_L = 15Ω	5	8		V/µs
Full-Power Bandwidth			See Typical Curve		
Settling Time 0.1%	G = –10, 60V Step		25		µs
Total Harmonic Distortion			See Typical Curve		
OUTPUT					
Voltage Output, Positive	I_O = 2A	(V+) –5	(V+) –4.4		V
Negative	I_O = 2A	(V–) +5	(V–) +3.8		V
Positive	I_O = 0.5A	(V+) –4.2	(V+) –3.8		V
Negative	I_O = 0.5A	(V–) +4	(V–) +3.1		V
Current Output			See SOA Curves		
Short-Circuit Current			4		A
POWER SUPPLY					
Specified Operating Voltage			±35		V
Operating Voltage Range		±10		±35	V
Quiescent Current	I_O = 0		±12	±15	mA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JC}	f > 50Hz		2.7		°C/W
Thermal Resistance, θ_{JC}	DC		3		°C/W
Thermal Resistance, θ_{JA}	No Heat Sink		65		°C/W

NOTES: (1) High-speed test at T_J = 25°C.

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	70V
Output Current	See SOA Curve
Input Voltage	(V–) –0.7V to (V+) +0.7V
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering –10s)[1]	300°C

NOTE: (1) Vapor-phase or IR reflow techniques are recommended for soldering the OPA544F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA544T	5-Lead TO-220	315
OPA544T-1	5-Lead Stagger-Formed TO-220	323
OPA544F	5-Lead Surface-Mount	325

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

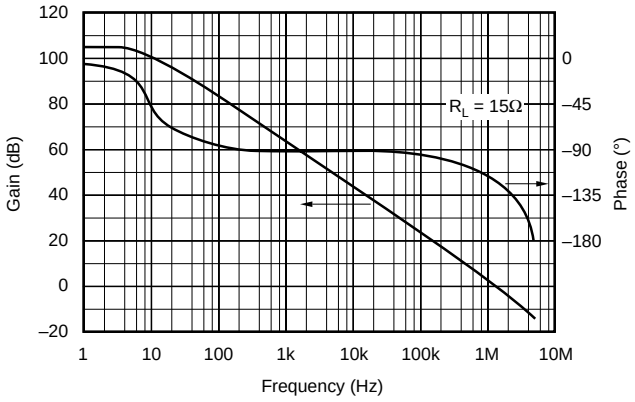
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

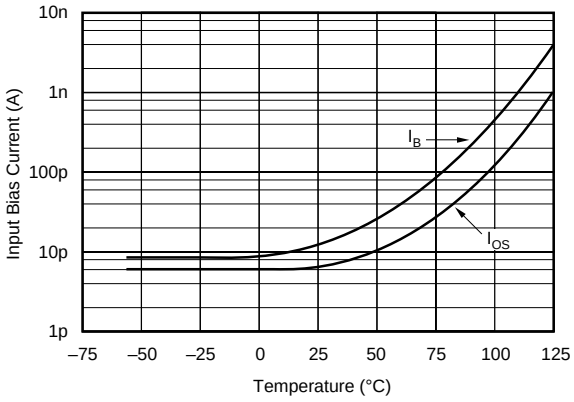
TYPICAL PERFORMANCE CURVES

At T_{CASE} = +25°C, V_S = ±35V, unless otherwise noted.

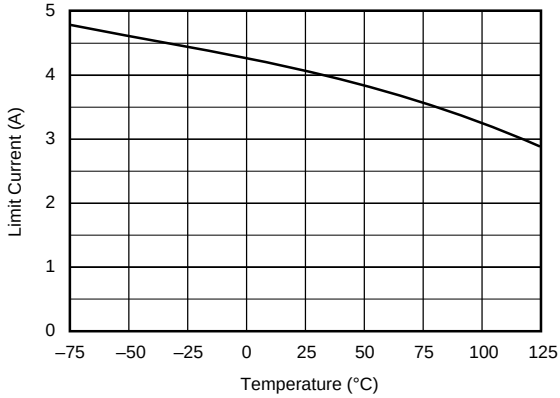
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



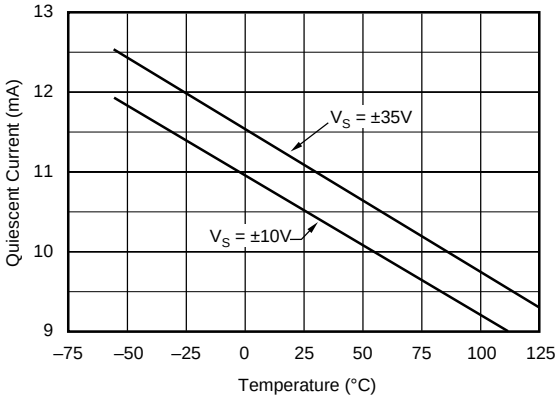
INPUT BIAS CURRENT vs TEMPERATURE



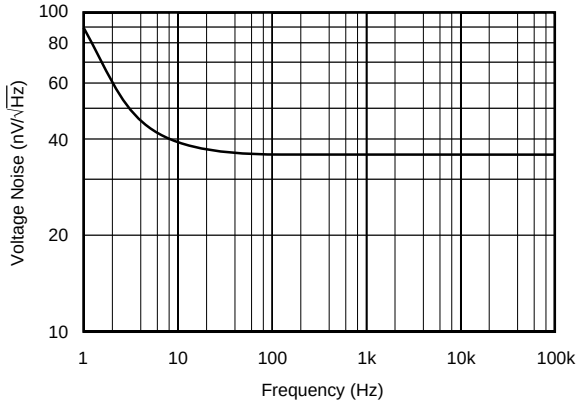
CURRENT LIMIT vs TEMPERATURE



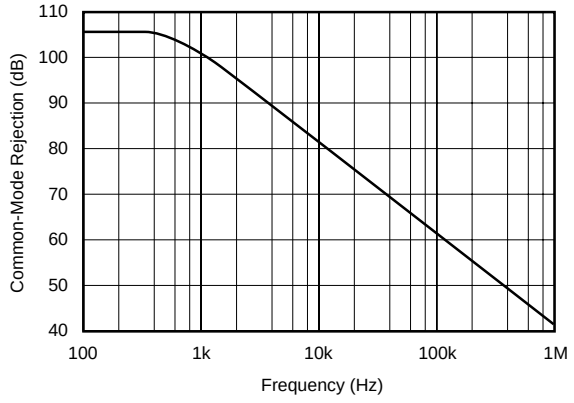
QUIESCENT CURRENT vs TEMPERATURE



VOLTAGE NOISE DENSITY vs FREQUENCY



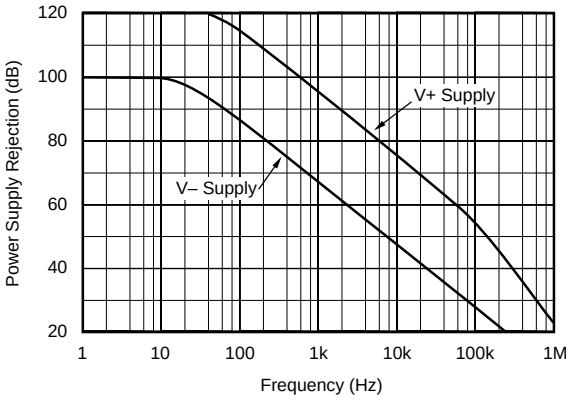
COMMON-MODE REJECTION vs FREQUENCY



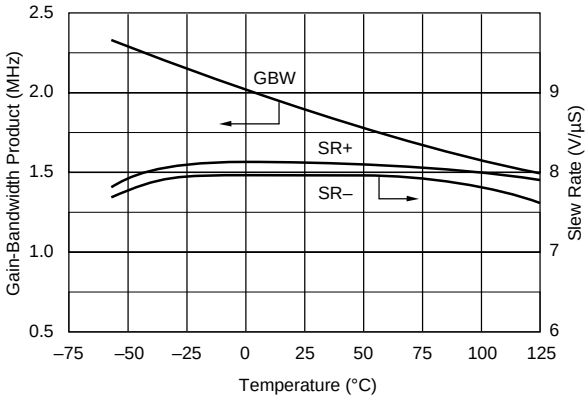
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_S = ±35V, unless otherwise noted.

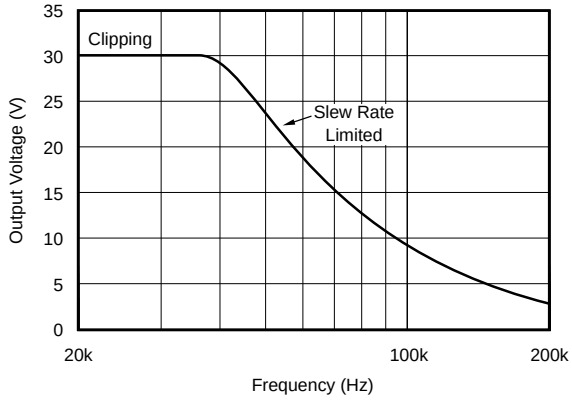
POWER SUPPLY REJECTION vs FREQUENCY



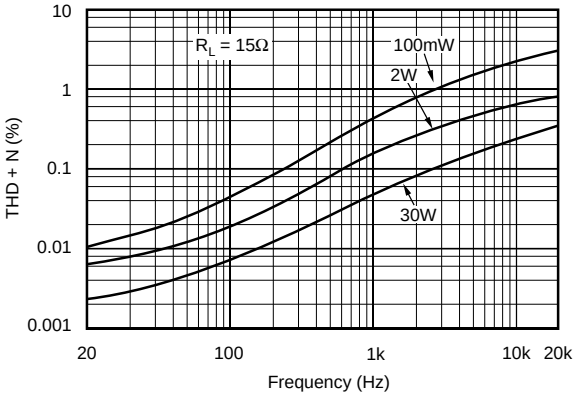
GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE



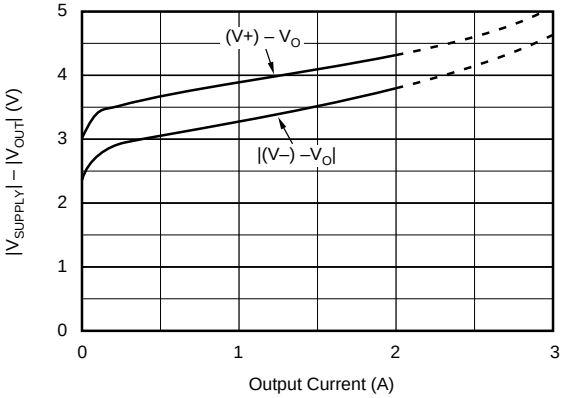
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



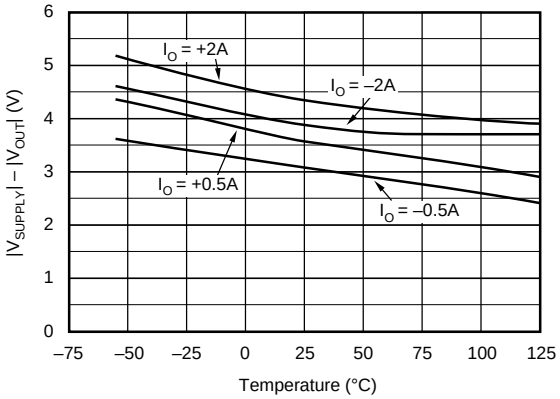
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



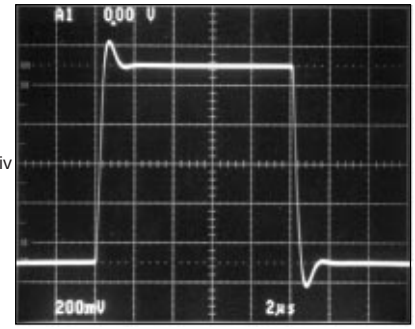
OUTPUT VOLTAGE SWING vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

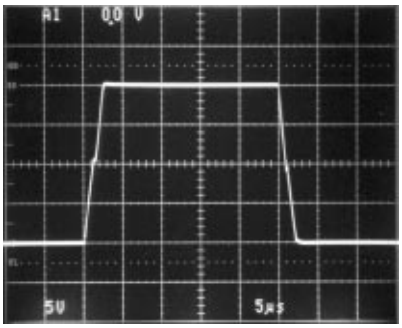
At T_{CASE} = +25°C, V_S = ±35V, unless otherwise noted.

SMALL SIGNAL RESPONSE
G = 3, C_L = 1nF



200MV/div

2µs/div



5V/div

APPLICATIONS INFORMATION

Figure 1 shows the OPA544 connected as a basic non-inverting amplifier. The OPA544 can be used in virtually any op amp configuration. Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel is recommended. Power supply wiring should have low series impedance and inductance.

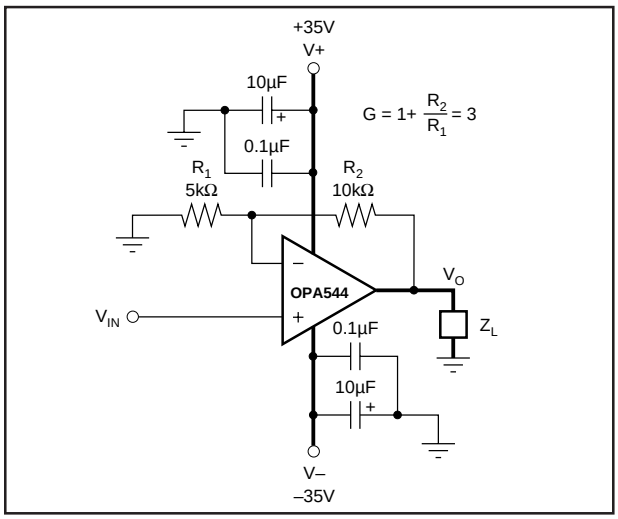


FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor, V_S–V_O. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_S–V_O. The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

The safe output current decreases as V_S–V_O increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V+ or V–) across the conducting transistor. With V_S = ±35V the safe output current is 1.5A (at 25˚C). The short-circuit current is approximately 4A which exceeds the SOA. This situation will activate the thermal shutdown circuit in the OPA544. For further insight on SOA, consult Application Bulletin AB-039.

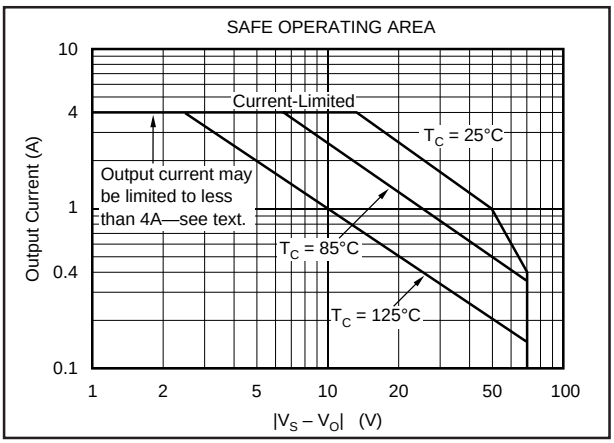


FIGURE 2. Safe Operating Area.

CURRENT LIMIT

The OPA544 has an internal current limit set for approximately 4A. This current limit decreases with increasing junction temperature as shown in the typical curve, Current Limit vs Temperature. This, in combination with the thermal shutdown circuit, provides protection from many types of overload. It may not, however, protect for short-circuit to ground, depending on the power supply voltage, ambient temperature, heat sink and signal conditions.

POWER DISSIPATION

Power dissipation depends on power supply, signal and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

HEATSINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The mounting tab of the surface-mount package version should be soldered to a circuit board copper area for good heat dissipation. Figure 3 shows typical thermal resistance from junction to ambient as a function of the copper area.

THERMAL PROTECTION

The OPA544 has thermal shutdown that protects the amplifier from damage. Any tendency to activate the thermal shutdown circuit during normal operation is indication of excessive power dissipation or an inadequate heat sink.

The thermal protection activates at a junction temperature of approximately 155˚C. For reliable operation, junction temperature should be limited to 150˚C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than 25˚C above the maximum expected ambient condition of your application. This produces a junction temperature of 125˚C at the maximum expected ambient condition.

Depending on load and signal conditions, the thermal protection circuit may produce a duty-cycle modulated output signal. This limits the dissipation in the amplifier, but the rapidly varying output waveform may be damaging to some loads. The thermal protection may behave differently depending on whether internal dissipation is produced by sourcing or sinking output current.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. Figure 3 shows an output series R/C compensation network (1Ω in series with 0.01µF) which generally provides excellent stability. Some variation in circuit values may be required with certain loads.

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA544 do not need to be equal. For example, a –6V negative power supply voltage assures that the inputs of the OPA544 are operated within their linear common-mode range, and that the output can swing to 0V. The V+ power supply could range from 15V to 65V. The total voltage (V– to V+) can range from 20V to 70V. With a 65V positive supply voltage, the device may not be protected from damage during short-circuits because of the larger V_{CE} during this condition.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 4. Fast-recovery rectifier diodes with a 4A or greater continuous rating are recommended.

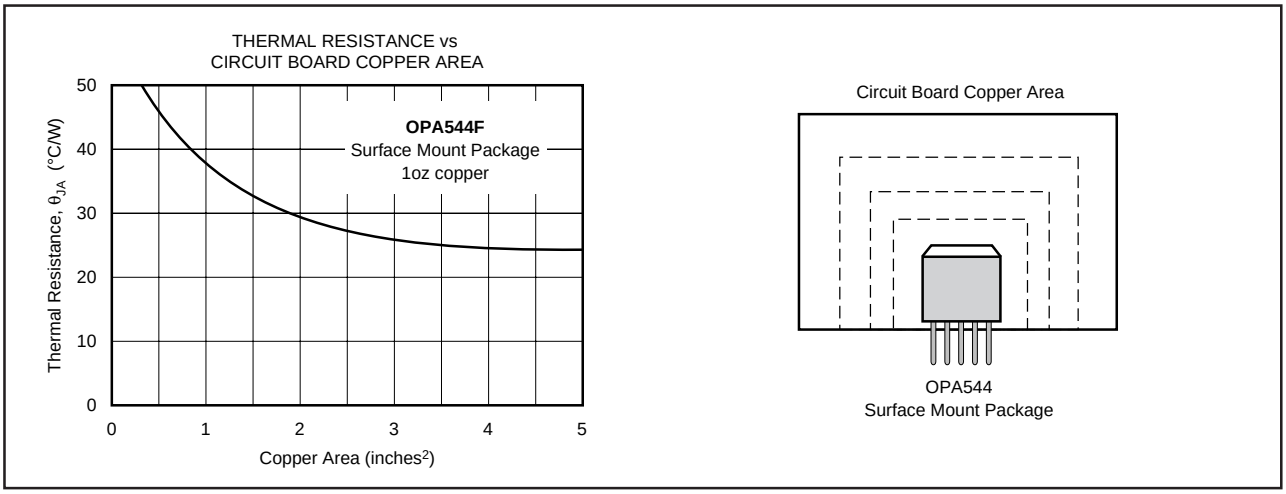


FIGURE 3. Thermal Resistance vs Circuit Board Copper Area.

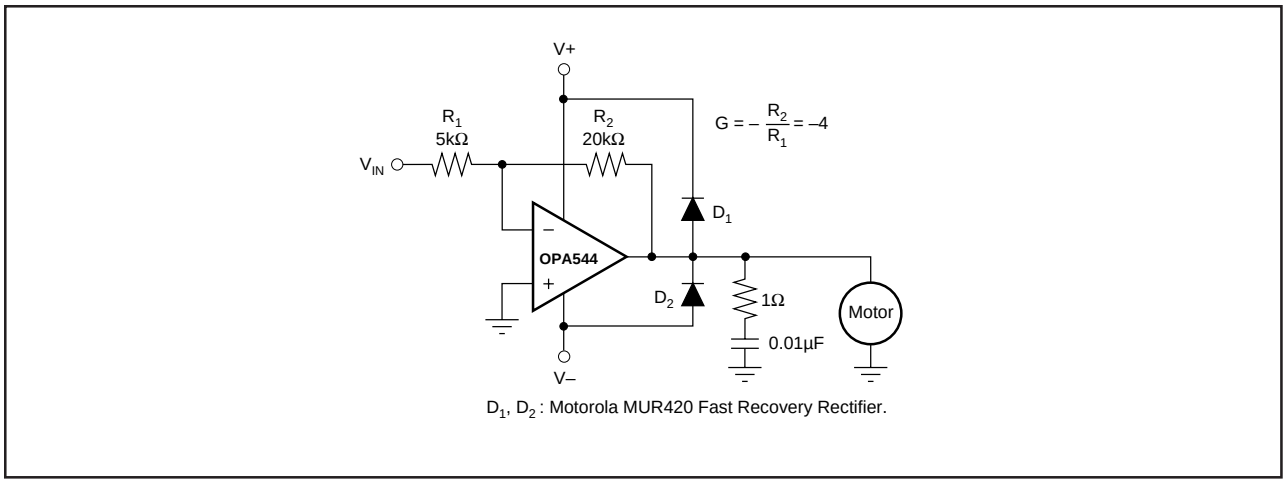


FIGURE 4. Motor Drive Circuit.

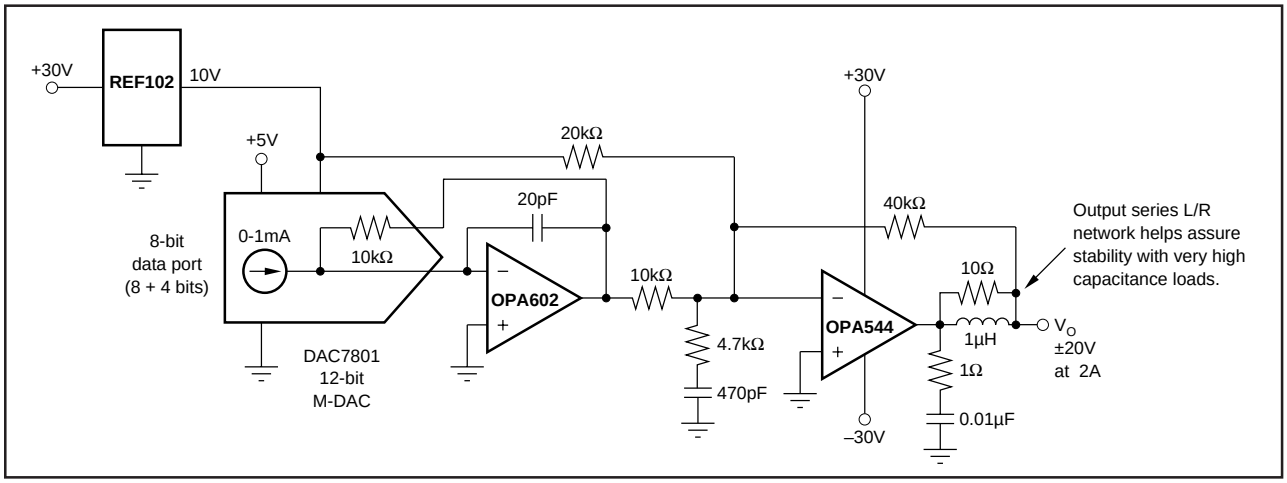


FIGURE 5. Digitally Programmable Power Supply.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA544F/500	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-	OPA544F
OPA544FKTTT	Active	Production	DDPAK/ TO-263 (KTT) | 5	250 | SMALL T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-	OPA544F
OPA544T	Active	Production	TO-220 (KC) | 5	49 | TUBE	Yes	Call TI | Sn	N/A for Pkg Type	-40 to 85	OPA544T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

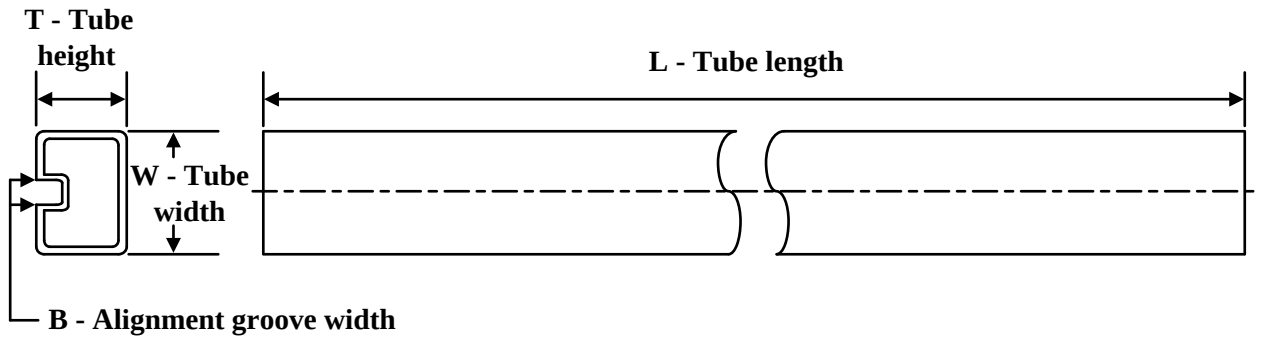
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

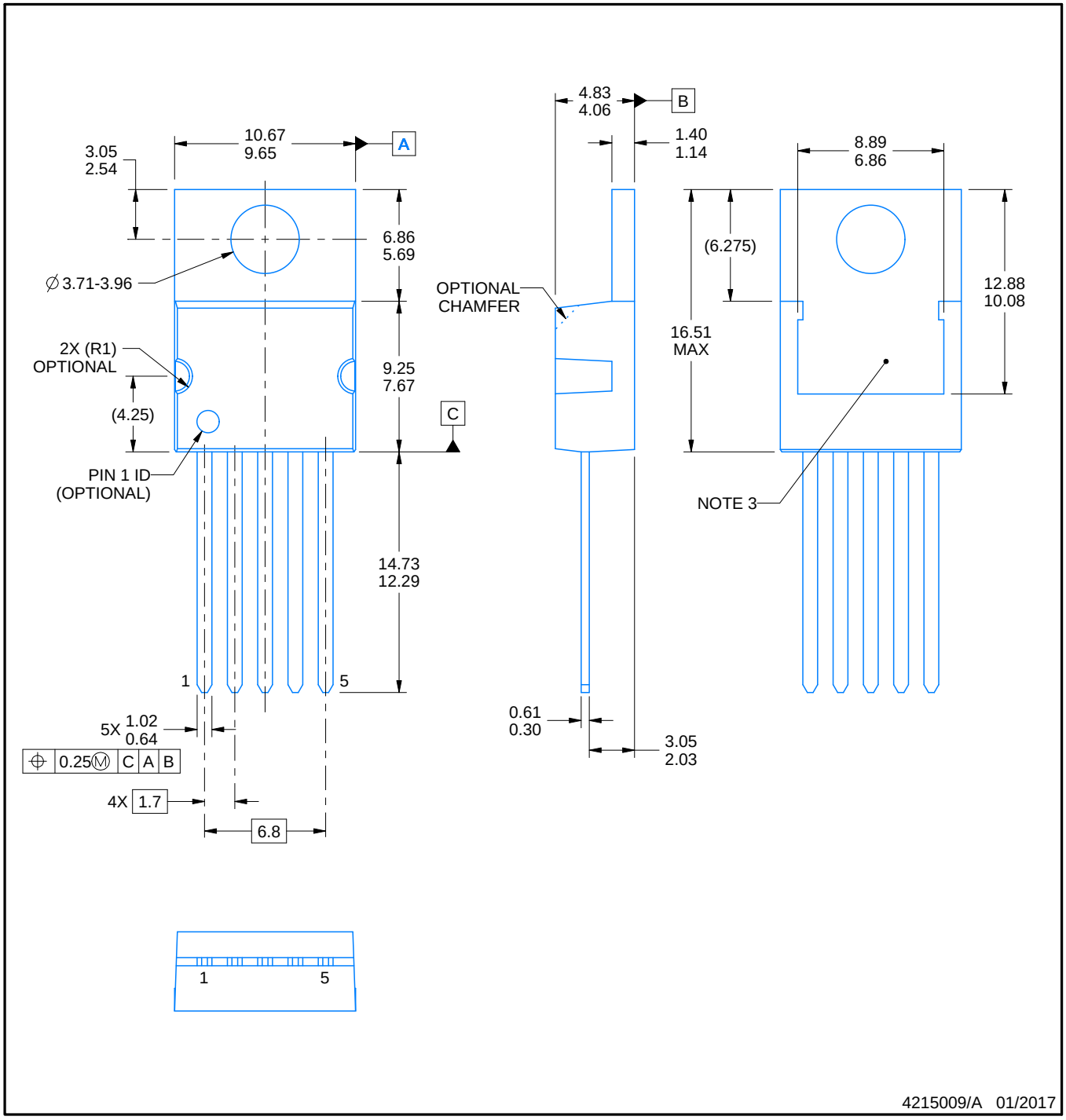
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA544T	KC	TO-220	5	49	546	31	11930	3.17

KC0005A

PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



NOTES:

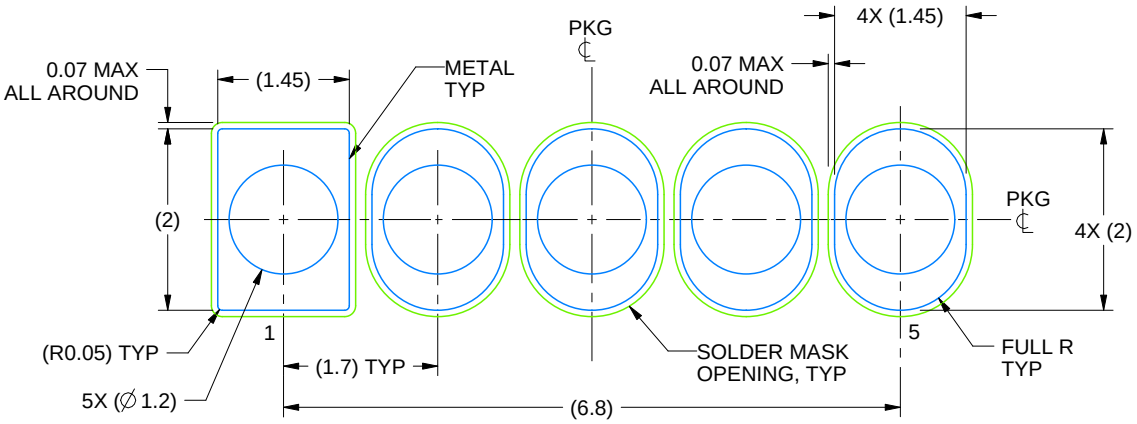
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

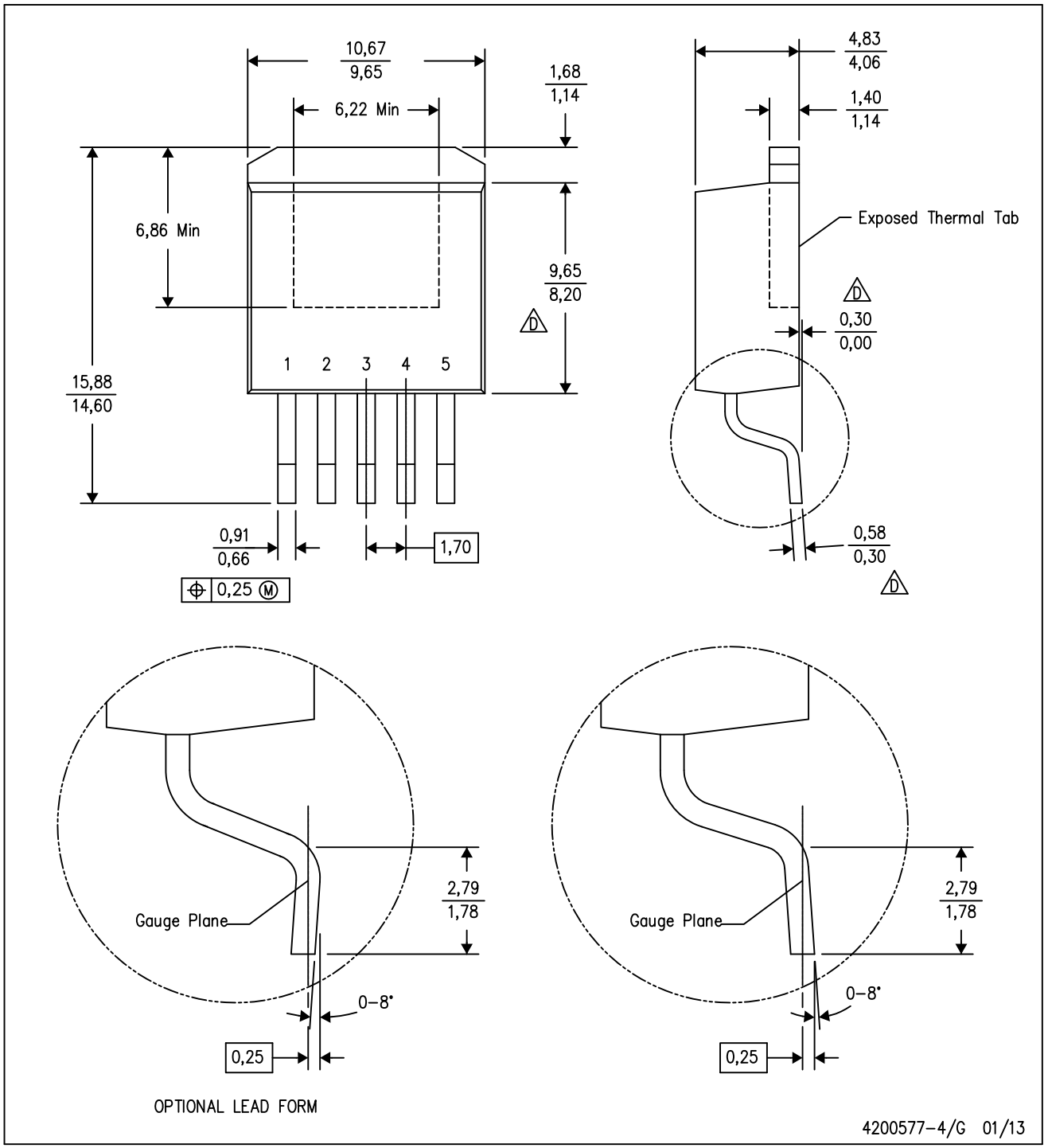
TO-220



LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

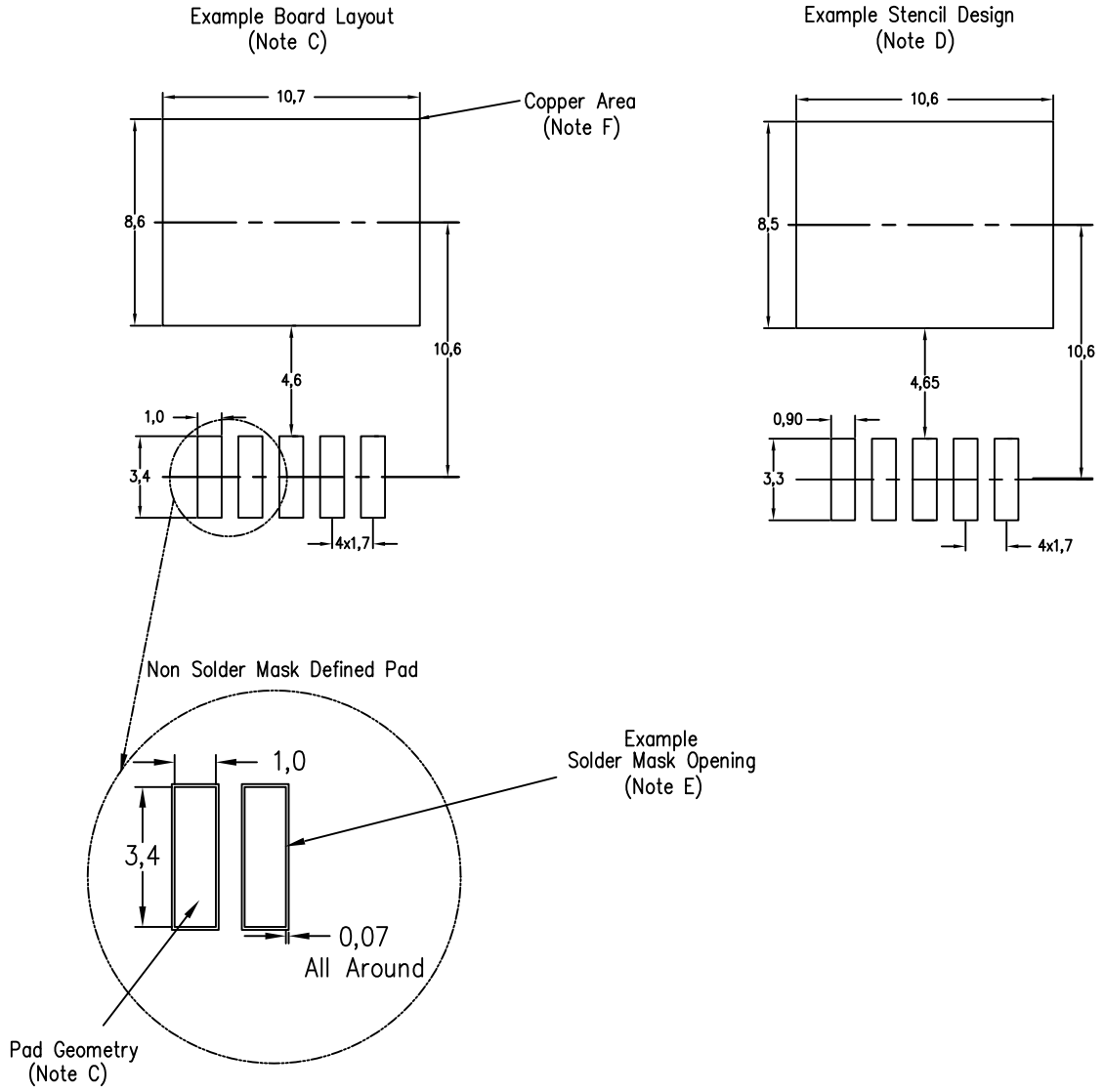
4215009/A 01/2017

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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