Si24R2H
datasheet

南京中科微

Si24R2H

Ultra-Low Power and High Performance 125KHz Receive and 2.4GHz GFSK Wireless Transmitter Single Chip

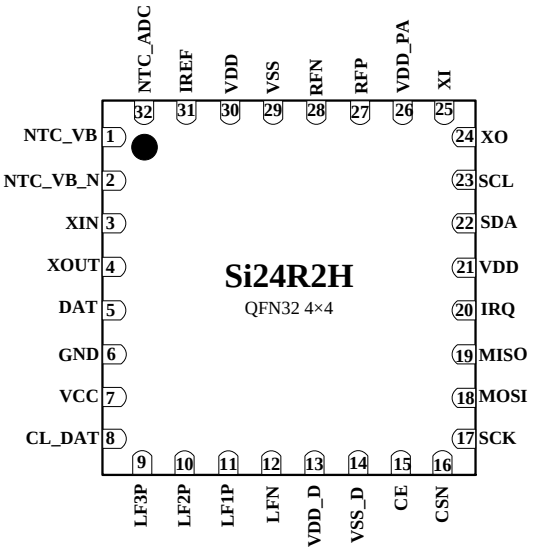
Main features

- Transmits in the 2.4GHz ISM band
- Transmitter compatible with BLE 4.2
- Receiving operation at 15KHz-150KHz
- Built-in 32 times programmable NVM memory
- 3.3V programming voltage
- Integrated low voltage automatic alarm function
- Integrated temperature alarm and anti-tampering alarm
- Integrated anti-conflict communication mechanisms
- Ultra-low power auto-transmit/125KHz trigger transmit function
- Built-in three-channel low-power ASK receiver
- Programmable 16bit/32bit Manchester code wake-up
- 125KHz receive sensitivity 60uVRMS
- Integrated 125KHz triggered entry and exit door auto-detection and positioning function
- Integrated 125KHz wireless programming
- External NTC/SHT21/MLX90615 temperature sensor
- Built-in 10bit digital temperature sensor
- Built-in 3KHz RCOSC and hardware watchdog
- Transmit modulation：GFSK/FSK
- Receiving modulation：ASK
- Transmit data rate:2Mbps/1Mbps/250Kbps
- Minimum standby current 1uA
- Wide supply voltage range:2.1-3.6V(transmitter)
- Wide digital IO voltage range:1.9V-3.6V
- Programmable transmit power:14dBm~-3dBm
- Transmit current:18mA(0dBm)
- 125KHz minimum monitoring current 3.3uA
- Up to 10MHz 4-wire SPI interface
- Transmit data hardware interrupt output
- QFN32 4x4 package
- 32.768KHz optional crystal oscillator
- Low cost 16M crystal oscillator:16MHz±20ppm
- Compatible with Si24R1 and Si24R2X transmit funtion

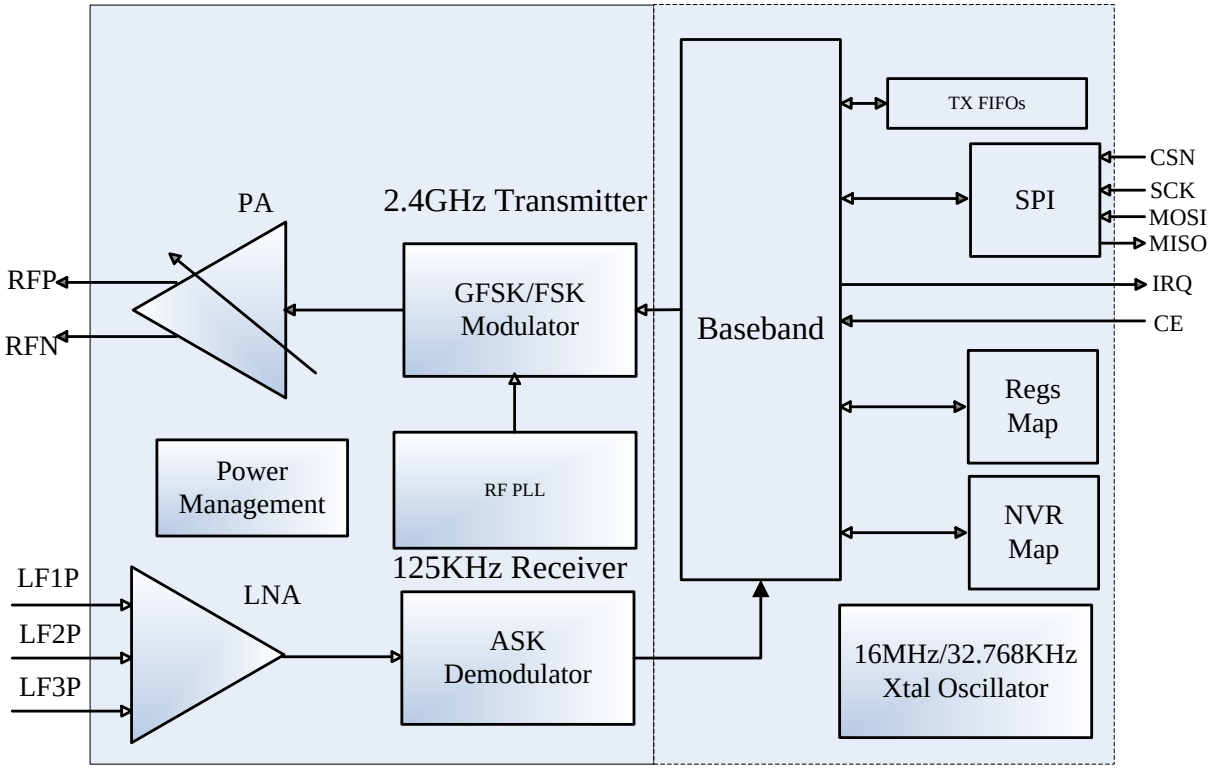
Application

- Ultra low power active RFID system
- Smart campus card management system
- Electric bicycle movement monitoring system
- Intelligent cold chain temperature transportation management system
- Livestock raising management system
- Other IoT systems
- Car PKE keyless entry

Package outline



Block diagram



Abbreviations

Abbreviation	Description
ARQ	Auto Repeat-reQuest
ART	Auto ReTransmission
ARD	Auto Retransmission Delay
ATR	Auto Transmission
BER	Bit Error Rate
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select
DPL	Dynamic Payload Length
GFSK	Gaussian Frequency Shift Keying
IRQ	Interrupt Request

ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
Mbps	Megabit per second
MCU	Micro Controller Unit
MHz	Mega Hertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
NVM	Non-volatile Memory
PA	Power Amplifier
PID	Packet Identity
PLD	Payload
RX	RX
TX	TX
PWR_DWN	Power Down
PWR_UP	Power UP
RF_CH	Radio Frequency Channel
RSSI	Received Signal Strength Indicator
RX	Receiver
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TX	Transmitter
TX_DS	Transmit Data Sent
XTAL	Crystal
Watchdog	Hardware Watchdog

Contents

1 Introduction

The Si24R2H is a wireless transceiver IC designed for ultra-low power wireless applications with embedded baseband, operating in the 2.4GHz ISM band for transmit and 125KHz for receive.The Si24R2H operates in the frequency range of 2400MHz-2525MHz with 125 channels of 1MHz bandwidth,and receives in the frequency range of 15KHz-150KHz.

Si24R2H adopts GFSK/FSK digital modulation and demodulation technology.The data rate and PA output power can be adjusted to support three transmit data rates:2Mbps,1Mbps,and 250Kbps.Higher data rates allow the same amount of data to be sent and received in a shorter period of time,resulting in lower power consumption.

The Si24R2H has a built-in three-channel ASK receiver that detects data signals at LF carrier frequencies between 15KHz-150KHz and triggers 2.4GHz transmissions with configurable contents.The Si24R2H supports 16-bit or 32-bit Manchester wake-up mode and automatic entry/exit direction judgment,and supports internal NVM wireless programming through 125KHz receiver,which is very convenient for mass production.

Si24R2H built-in multiple temperature sensors and interfaces,internal integrated 10bit digital temperature sensor,can be connected to an external NTC resistor or SHT21 temperature and humidity sensor and MLX90615 infrared temperature sensor for human body temperature measurement.

The Si24R2H supports transmitting BLE4.2 standard packets and can easily transmit data to cell phones.

Si24R2H is specially optimized for low-power applications.Si24R2H turns on the auto-launch function,the internal Watchdog and internal RCOSC clock work,the internal Timer timer starts timing,the chip works in the sleep state,all the registers and FIFOs remain unchanged,the RTC and the Watchdog work,and the standby current is only 1uA.when the internal Timer timer or 125KHz trigger wake-up,the auto-launch controller automatically finishes loading and launching data from the NVM memory.When the internal timer or 125KHz trigger wakes up,the auto-transmit controller automatically completes the data loading and transmitting from the NVM memory,and the chip enters the sleep state immediately after the data transmitting is completed.The average power consumption of the Si24R2H is very low,which is especially suitable for coin cell battery-powered application systems.

Si24R2H is easy to operate,no need for external MCU,that is,it can automatically complete the data loading and transmitting,NVM memory can store register configuration and transmitting data content,will not be lost after power down,data can be maintained for more than 10 years.Under 3.3V supply voltage,without external high voltage,external MCU can complete NVM configuration and programming through the chip's four-wire SPI interface or 125KHZ wireless,the chip's maximum number of programmable times is 32,the chip supports NVM locking,preventing the NVM configuration data from being read back to ensure the safety of user data.

Si24R2H does not need 32.768KHz crystal,through the 125KHz receiver can also realize the high precision position location,suitable for various IOT applications and PKE keyless system,Si24R2H has a very low system cost,no external MCU,only a small number of peripheral passive components can be composed of an active RFID wireless data transceiver system.

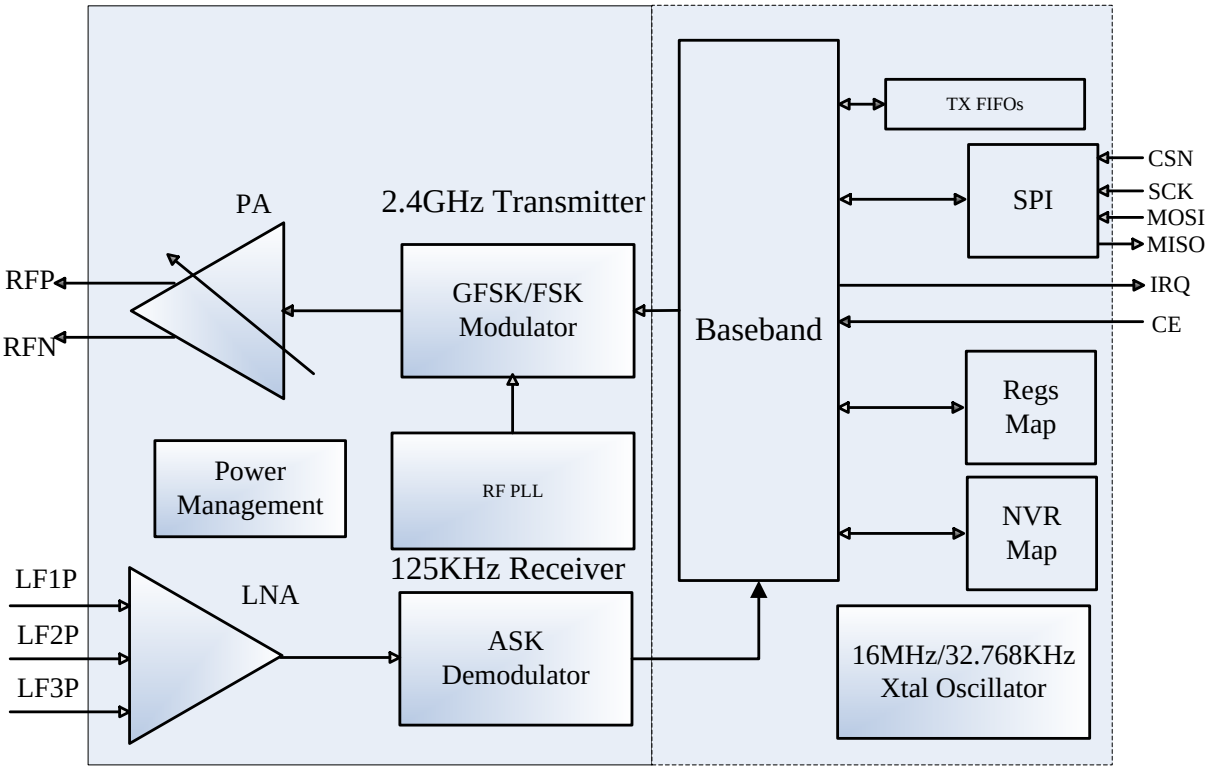


Figure 1-1 Chip structure diagram

2 Pinning information

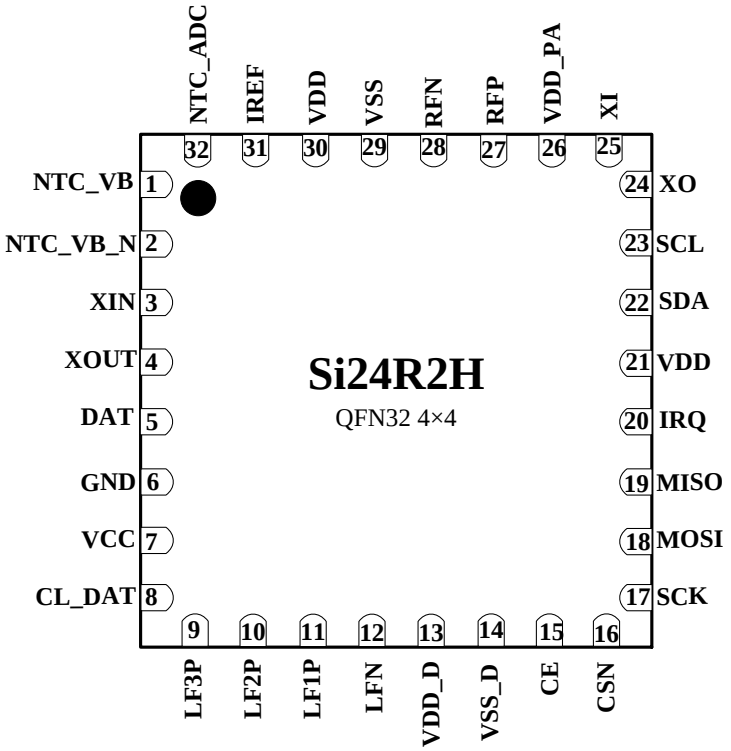


Figure2-Pinning information(QFN32 4×4 package)

Table 2-1 Pin description

Port	Pin name	Pin type	Description
1	NTC_VB	AO	NTC bias voltage
2	NTC_VB_N	A	NTC bias voltage
3	XIN	AI	32.768KHz crystal oscillator input pin(optional)
4	XOUT	AO	32.768KHz crystal oscillator output pin(optional)
5	DAT	DO	Data out
6	GND	Power	Ground(0V)
7	VCC	Power	Power supply
8	CL_DAT	DO	Manchester recovered clock
9	LF3P	AI	125KHz channel 3 input
10	LF2P	AI	125KHz channel 2 input
11	LF1P	AI	125KHz channel 1 input
12	LFN	AI	125KHz channel common ground

13	VDD_D	Power	Internal power supply
14	VSS_D	Power	Ground
15	CE	DI	Transmit enable signal,multiplexed as tamper control signal
16	CSN	DI	SPI chip select signal
17	SCK	DI	SPI clock signal,key transmit,replace transmit control signal
18	MOSI	DI	SPI input signal,key transmit,replace transmit control signal
19	MISO	DO	SPI output signal
20	IRQ	DO	Maskable interrupt signal,low active
21	VDD	Power	Power supply
22	SDA	DIO	I2C data，external temperature sensor
23	SCL	DO	I2C clock，external temperature sensor
24	XO	AO	16MHz crystal oscillator output pin
25	XI	AI	16MHz crystal oscillator input pin
26	VDD_PA	Power	Power supply pin to built-in PA(+1.8V)
27	RFP	RF	Antenna interface 1
28	RFN	RF	Antenna interface 2
29	VSS	Power	Ground(0V)
30	VDD	Power	Power supply
31	IREF	AI	Reference current
32	NTC_ADC	AI	NTC capture

3 Operating modes

3.1 Wireless transmitting mode

3.1.1 State control diagram

The Si24R2H chip has a built-in 2.4GHz transmitter with an internal state machine that controls the chip's transitions between different operating transmission modes.

The Si24R2H 2.4Ghz transmitter can be configured for Shutdown,Standby,Idle-TX,TX,and RX transmitter operating modes.The state transition diagram is shown in Figure 3-1.

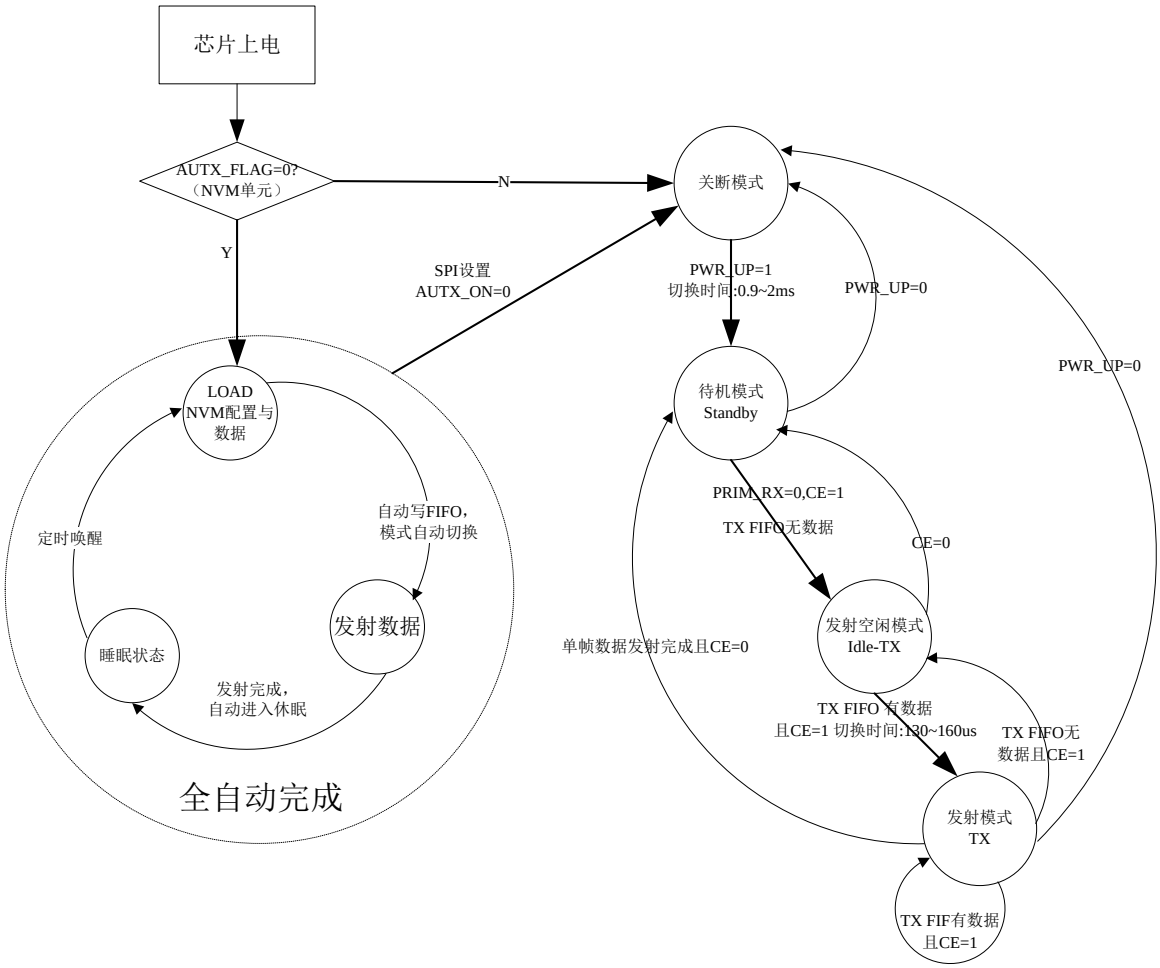


Figure3.1-Si24R2H transmitter operating mode switch diagram

3.1.2 Shutdown mode

When the chip NVM internal configuration ATR function is turned off,AUTX_FLAG is 1,the chip power on directly into the Shutdown mode.In Shutdown mode,Si24R2H all function modules off,the chip stops working,the consumption of current is minimal,but all the internal registers and FIFO values remain unchanged,can still be realized through the SPI to the registers of the read and write process.Read and write the registers through SPI.When the receiver is not working at all,the chip will work at about 1uA when the value of PWR_UP bit in CONFIG register is set to 0,and the chip will return to Shutdown mode immediately.

3.1.3 Standby mode

In Standby mode only part of the crystal oscillator is active.Standby mode is used to minimize average current consumption while maintaining short start-up times.Standby mode is entered after the crystal oscillator works stably by setting PWR_UP bit in the CONFIG register to 1.The crystal oscillator startup time is about 1.5~2ms,which is related to the performance of the crystal oscillator.The Si24R2H enters Idle-TX or RX mode by setting CE high.When CE pin is set low,Si24R2H returns to Standby mode from Idle-TX mode,TX or RX mode.

3.1.4 Idle-TX mode

In Idle-TX mode,the crystal oscillator and clock buffers are active and more current is used compared to Standby mode.Si24R2H enters Idle-TX mode if CE is held high on a PTX device with an empty on TX FIFO.If a new packet is uploaded to the TX FIFO,the internal circuits will be active immediately,Si24R2H enters TX mode and the packet is transmitted.

Both in Standby and Idle-TX mode all register and FIFO values are maintained and can be written or read by SPI.

3.1.5 TX mode

The TX mode is an active mode for transmitting packets.To enter this mode,Si24R2H must have PWR_UP bit set high,PRIM_RX bit set low,a payload in the TX FIFO and a high pulse on the CE pin for more than 10us.The transition time from Idle-TX mode to TX mode takes

130us~160us,but will not more than 130us.Si24R2H stays in TX mode until it finishes transmitting a packet.If CE=1,the status of TX FIFO determines the next action.If the TX FIFO is not empty the Si24R2H remains in TX mode and transmits the next packet.If the TX FIFO is empty the Si24R2H goes into Idle-TX mode.If CE=0,Si24R2H returns to Standby mode.The Si24R2H provides a TX interrupt after finishing transmitting a packet.

3.1.6 ATR mode

When the ATR function is turned on in the NVM of the chip,AUTX_FLAG is 0 and the CSN pin is high,the chip enters the ATR mode after power-on,the chip automatically loads the register configuration from the NVM,and automatically writes the data into the FIFO,and then transmits the data after the chip is stabilized,and then enters the sleep state after the data transmission is completed.In the sleep state,the internal hardware Watchdog,RCOSC and timer circuits work,the register state is maintained,in the case of the receiver does not work at all,the entire chip operating current is about 1u A.Since the chip transmits data for a short time,and most of the time works in the sleep state,the chip's average operating current is very low.

The retransmission interval of data can be configured in NVM,supports simple ALOHA protocol,supports automatic frequency hopping of four frequency points,and reduces the conflict probability of multiple chips transmitting data at the same time.

When the ATR function is activated and the external MCU writes the AUTX_ON command through the SPI interface,the ATR function will be turned off,the MCU can realize the internal register configuration and data transmission through the SPI interface,and then the ATR function will be turned on again by writing the same AUTX_ON command again,and the chip will re-enter into the ATR auto-transmit operation mode.The AUTX_ON command can also be disabled after the chip software reset command is executed or after the chip is re-powered up,so that the ATR function is turned off and the chip re-enters the ATR auto-transmit mode.The function is activated again.

When the ATR function is activated,before the external MCU writes the AUTX_ON command through the SPI interface,it must first pull the CSN pin of the SPI low and then pull it high(a low pulse),followed by CSN pulling it low to write the AUTX_ON command.

In ATR operation mode,the internal hardware Watchdog circuit(Watchdog)is automatically turned on,and the chip is automatically reset and restarted when three consecutive data transmissions are unsuccessful.

3.2 Wireless receiving mode

3.2.1 State control diagram

The Si24R2H chip features a 125kHz three-channel low-power ASK receiver for detecting digital signals at low-frequency carrier frequencies from 15kHz to 150kHz and generating wake-up signals.The integrated internal checker detects wake-up matches in 16-bit or 32-bit Manchester encoding and supports two repetitions of the match value check.

The receiver can operate with one,two or three channels,each with frequency detection and digital RSSI calculation.The sensitivity of the channels is adjustable,allowing longer communication distances and adaptation to noisy environments.

The state switch diagram is shown in Figure 3.2-1.

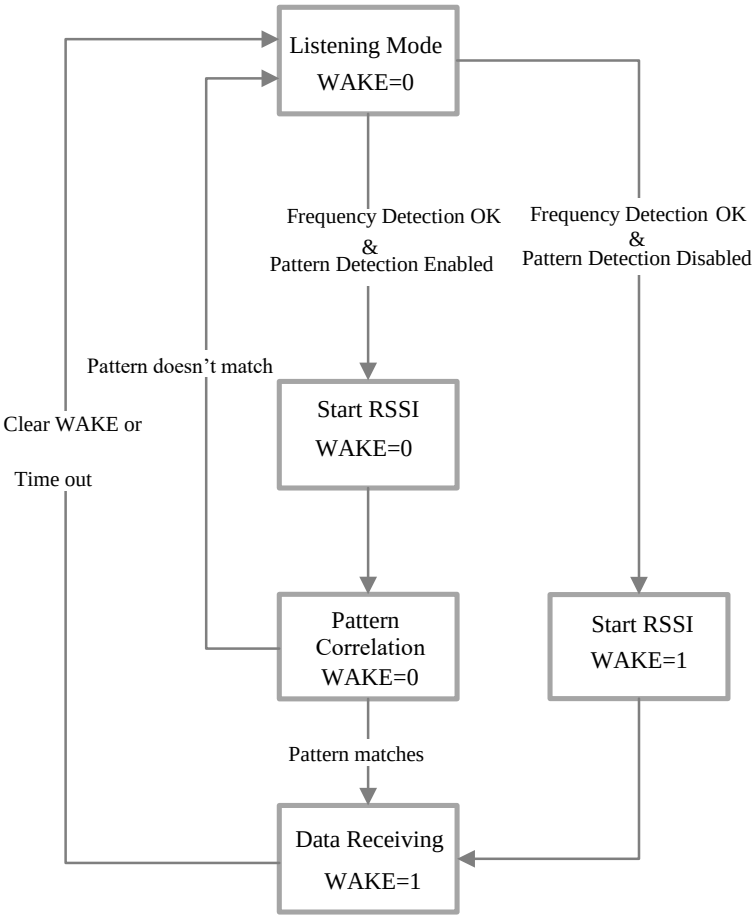


Figure3.2-125K operating mode flowchart

3.2.2 Listening mode

In listening mode,the chip is active and looks continuously for the presence of the carrier on the input of all active channels.In case the carrier is detected,then the RSSI measurements get started on all three channels and the result is stored in the memory.

If the three dimensional detection is not required,then it is possible to deactivate one or more channels.In case only two channels are required,then the deactivated channel must be the number two;while in case only one channel is needed,then the active channel must be the number one.

Inside the listening mode,it is possible to distinguish the following three modes：Standard listening mode,Scanning mode and ON/OFF mode.

3.2.2.1 Standard listening mode

All channels are active at the same time.

3.2.2.2 Scanning mode(Low Power mode 1)

A time slot T=1ms is defined and in each time slot only one channel can be active.As shown in Figure 3.2-2 when a certain time slot is over,the current active channel is switched OFF and the next channel becomes active and so on.If,for example all three channels are enabled,in the first time slot the only active channel is the number one.When the first time slot is over,the channel one is switched OFF and the channel three becomes active.During the third time slot,the channel two is active while the other two are OFF.This channel rotation starts back from the channel one and goes on until the presence of the carrier is detected by any channel.The Scanning mode(channel rotation)is managed internally by the 125K receiver and doesn’t need any activity from the host system(MCU).As soon as one channel detects the frequency,all three channels become immediately active at the same time.The 125K receiver can perform a simultaneous multidirectional evaluation(on all three channels)of the field and evaluate which channel has the strongest RSSI.The channel with the highest RSSI will be put through to the demodulator.In this way it is possible to perform multidirectional monitoring of the field with

a current consumption of a single channel,keeping the sensitivity as good as if all channels are active at the same time.

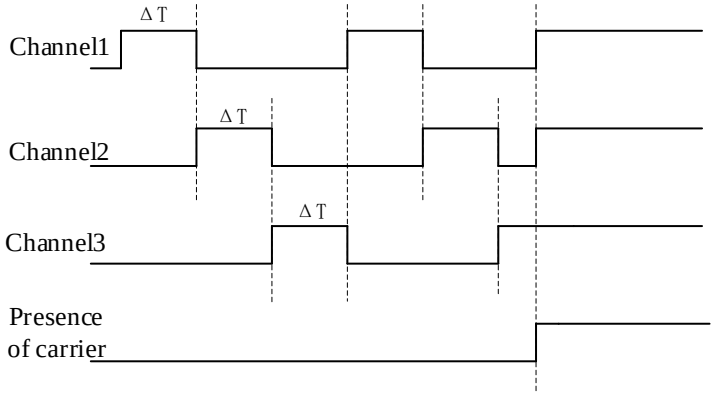


Figure3.2-Scanning mode

3.2.2.3 ON/OFF mode(Low Power mode 2)

In this low power sub-mode the chip sets the receiving channels in polling mode;all active channels are on at the same time only for a certain time T(where T is 1 ms).The OFF-time can be defined with the bits R4<7:6>.If,for example,R4<7:6>=11(see Figure 3.2-3)the active channels will be 1ms ON and 8ms OFF.

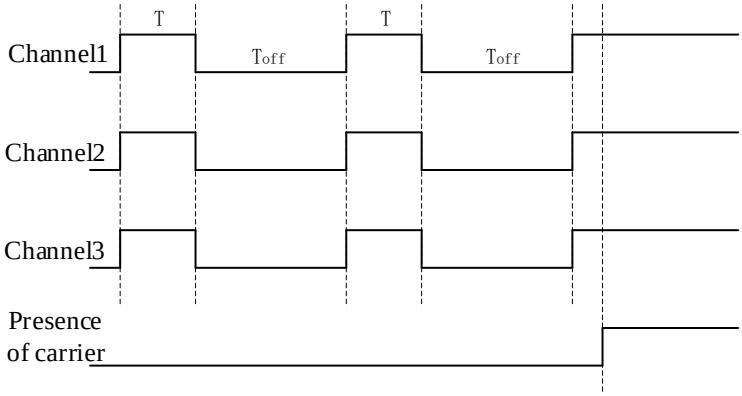


Figure3.2-ON/OFF mode

3.2.3 Artificial wake-up

Artificial wake-up can be turned on in listen mode,a counter based on a clock generation circuit.Register R8<2:0>defines a time window.If there is no action within this time window,the

wake-up interrupt signal WAKE is generated.

3.2.4 Preamble detection/pattern correlation

The chip can go in to this mode after detecting a LF carrier only if the data correlation is enabled(R1<1>=1).The correlator searches first for preamble bits and then for data pattern.Should the pattern correlation be disabled(R1<1>=0),the chip goes directly in Data receiving mode.

In this mode,if the received pattern matches,then the wake-up interrupt is displayed on the WAKE output(Wake goes high)and the chip goes in Data receiving mode.If the pattern fails,then the internal wake-up(on all active channels)is terminated and no interrupt is produced.

Having per default DAT_MASK disabled(R0<6>=0),the DAT pin shows the entire demodulated incoming signal(carrier burst+preamble+pattern+data).If DAT_MASK is enabled(R0<6>=1),the data will be displayed only after the generation of the WAKEUP interrupt.

3.2.5 Data receiving

After a successful wake-up the chip enters the data receiving mode.In this mode the chip can be retained a normal OOK receiver.The data is provided on the DAT pin and in case the Manchester decoder is enabled(see R1<3>=1),the recovered clock is present on the CL_DAT.It is possible to set the chip back to listening mode either with a direct command CLEAR_WAKE or by using the timeout feature.This feature automatically sets the chip back to listening mode after a certain time defined by the bits R7<7:5>.

4 SPI Interface

The SPI interface is a standard 4-wire SPI with a maximum data rate of 10Mbps.MCU can configure the chip through SPI interface,including R/W register,read and write FIFO,read the status of chip and clear the interrupts etc.

4.1 SPI Commands

See Table 4-1 and Table 4-2 for SPI commands.the CSN flips from high to low and the SPI interface begins operation.For each SPI operation,the first byte output from MISO is the value of the status register,and then the command is used to determine whether to output the value or not(no output is a high resistance state).Command words are entered in order from MSBit to LSBit in the command format,LSByte to MSByte in the data format,and MSBit to LSBit in each byte.For details,refer to SPI Timing,Figure 4-1 and Figure 4-2.

Table 4-1 2.4GHz module SPI commands

Command name	Command word(binary)	#Data bytes	Operations
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read register command,AAAAA represents register address(refer to the register table)
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write register command,AAAAA represents register address(refer to the register table),only allowed in Shutdown,Standby and Idle-TX mode
TESTREG_EN	01010000	1 Byte	Enter command 50,then data A5,which can enable NVM operation and r/w test register
NVMOP_EN	01011010	1 Byte	Enter command 5A,then data A5,which can enable NVM operation and read data from NVM
PROG_EN	01011011	1 Byte	Enter command 5B,then data A6,which can enable NVM programming
SW_PULL_CLR	01011101	1 Byte	Pull up CSN and enter command 5D,then data A8,represents force clearing the alarm state. Pull down CSN and enter command 5D,then data A8,represents the chip is in normal mode
AUTX_DISABLE	01011100	1 Byte	Enter the command 0x5C and immediately send the data 0xA7,indicating that

			Forces the ATR function to be turned off or on.When the ATR function is turned on,executing this command will turn off the ATR function and allow external MCU operates the internal register mapping.This command is disabled after hardware or software reset.AUTX_FLAG in NVM determines the switching of the ATR function.
SW_RST	01100011	0	The software reset command resets the entire chip.If NVM programmed and ATR function on,software reset will enter the automatic ATR mode.
W_NVM	10AA AAAA	1 Byte	Write NVM unit,AA_AAAA indicates the NVM address.Valid only under EN_NVMOP&PROG_EN.
R_NVM	11AA AAAA	1 to 32 LSByte first	Read NVM unit,AA_AAAA indicates NVM address.Valid only under EN_NVMOP.
FLUSH_TX	1110 0001	0	Clear TX FIFO for transmit mode.
REUSE_TX_PL	1110 0011	0	For sender,clear TX FIFO or write to FIFO. This command cannot be used with new data.
W_TX_PAYLOAD _NO ACK	1011 0000	1 to 32 LSByte first	For transmit mode,use this command to simultaneously set the AUTOACK bit to 1.
NOP	1111 1111	0	No operation.Can be used to return STATUS value.

Table 4-2 125kHz module SPI commands

Command name	Command word(binary)	#Data bytes	Operations
R_REG_125	100A AAAA	1 to 5 LSByte first	Read 125k registers. Mask this command when the EN_NVMOP command is in effect.
W_REG_125	110A AAAA	1 to 5 LSByte first	Write 125k registers. Mask this command when the EN_NVMOP

			command is in effect.
clear_wake	1010 0000	Clear wake-up	Only the single wake-up signal generated by 125kHz is cleared,not the 125k wake-up signal that wakes up the 2.4GHz transmitter module. Mask this command when the EN_NVMOP command is in effect.
reset_RSSI	1010 0001	Reset RSSI	Reset RSSI. Mask this command when the EN_NVMOP command is in effect.
trim_osc	1010 0010	Calibrate RC with scl	Calibrate RC with scl. Mask this command when the EN_NVMOP command is in effect.
clear_false	1010 0011	Clear error register	Clear error register. Mask this command when the EN_NVMOP command is in effect.
preset_default	1010 0100	Reset	Rsset. Mask this command when the EN_NVMOP command is in effect.
Calib_RCO_LC	1010 0101	Calibrate RC with LC	Calibrate RC with LC. Mask this command when the EN_NVMOP command is in effect.

4.2 SPI Timing

SPI operation includes basic Read/Write operation and other command operation.Figure 4.2-1 and Figure 4.2-2 show the SPI timing.

Note:The chip must be in Shutdown/Standby/Idle-Tx mode before writing to the configuration registers.

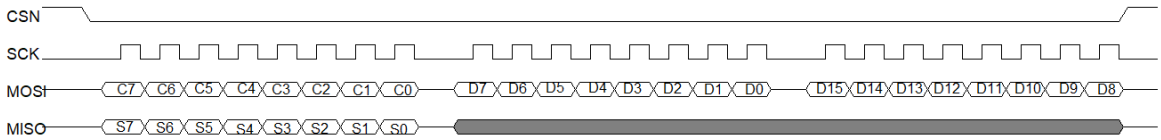


Figure 4.2-1 SPI write operation

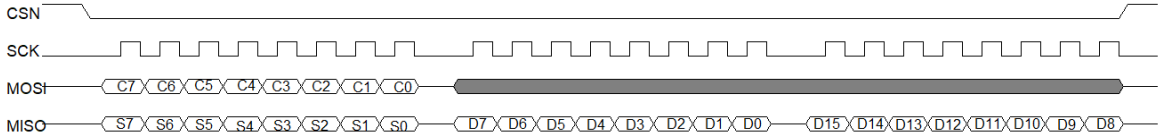


Figure 4.2-2 SPI read operation

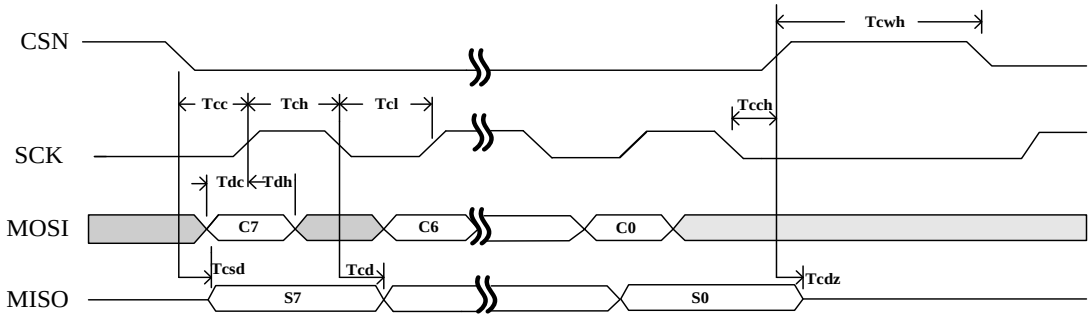


Figure 4-3 SPI typical timing

Table 4-3 SPI timing parameters

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

5 Register mapping

The chip has two sets of registers,the normal SPI registers and the NVM registers.The common SPI registers are the transmitter-related registers and the receiver-related registers.The transmitter related registers hold the control volume for 2.4GHz transmit function and the receiver related registers hold the control volume for 125kHz receive function.For details,see 5.1,5.2.NVM register information is shown in the NVM manual.

5.1 Transmit related registers

Table 5-1 2.4GHz module related registers

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration register
	WAKE_IRQ_EN	7	0	W/R	25k wake-up interrupt WAKE signal output enable 0:Disable 1:Enable
	Reserved	6	0	R	Reserved,0
	MASK_TX_DS	5	0	R/W	Transmit Interrupt Mask Control 0:Transmit interrupt enable,TX_DS interrupt flag generates an interrupt signal on the IRQ pin,active low 1:Transmit interrupt disable,TX_DS interrupt flag does not affect IRQ pin output
	Reserved	4	0	R/W	Reserved,0
	EN_CRC	3	1	R/W	Enable CRC.EN_CRC must be 1 if EN_AA is not all zeros. 0:Disable CRC 1:Enable CRC
	CRCO	2	0	R/W	CRC length configuration, 0:1byte 1:2 bytes

	PWR_UP	1	0	R/W	Off/On mode configuration 0:Shutdown mode 1:Start-up mode
	PRIM_RX	0	0	R/W	Fixed to 0
01	EN_AA				Enable auto-confirmation
	Reserved	7：6	00	R	Reserved,00
	EN_AA	5:0	111111	R/W	Set to all zeros for NOCRC Set to all zeros in compatibility mode,and set the ARC to 0
02	Reserved	7:0			
	Reserved	7:0	0	R/W	Reserved，0
03	SETUP_AW				Address width configuration
	Reserved	7:2	000000	R/W	Reserved,000000
	AW	1:0	11	R/W	Transmitter address width 00:error value 01:3bytes 10:4bytes 11:5bytes
04	Reserved				
	Reserved	7:0	0	R/W	Reserved，0
05	RF_CH				
	Reserved	7	0	R/W	Reserved，0
	RF_CH	6：0	0000010	R/W	Set the channel when the chip is working,corresponding to the 0th~125th channel respectively;the channel interval is 1MHz,default 0x02 which is 2402MHz
06	RF_SETUP				RF Configuration
	CONT_WAVE	7	0	R/W	1:Enable the constant carrier transmit mode to test transmit power
	Reserved	6	0	R/W	Reserved

	RF_DR_LOW	5	0	R/W	Set the RF data rate to 250kbps, 1Mbps or 2Mbps,with the RF_DR_HIGH common control
	PLL_LOCK	4	0	R/W	Reserved word,must be 0
	RF_DR_HIGH	3	1	R/W	Setting the RF data rate [RF_DR_LOW,RF_DR_HIGH]. 00：1Mbps 01：2Mbps 10：250kbps 11：Reserved
	RF_PWR	2:0	110	R/W	Setting TX transmit power 111:14dBm 110:13.5dBm 101:11dBm 100:10dBm 011:7dBm 010:4dBm 001:0dBm 000:-3dBm
07	STATUS				Status register(first byte of SPI operation,the status register value is passed through the MISO serial output).
	125k_wake	7	0	R	Wake-up signal at 125k
	Reserved	6	0	R	Reserved
	TX_DS	5	0	R	Transmitter transmit completion interrupt bit if in ACK mode,then ACK acknowledgement signal is received.After TX_DS sets to'1',write'1'to clear.
	CKF	4	-	R	Checksum flag,1:loaded correctly
	Reserved	3:1	111	R	Reserved,111
	TX_FULL	0	0	R	TX FIFO full flag bit.
08	Reserved				
	Reserved	7:0	-	NA	Reserved
09	Reserved				
	Reserved	7:0	-	NA	Reserved
0A	TMP				
	Reserved	39:8	-	NA	Reserved
	TMP	7:0	-	R	Temperature register

0B	Reserved	39:0		NA	Reserved
0C	Reserved	7:0	0	R/W	Reserved
0D	Reserved	7:0		NA	Reserved
0E	Reserved	7:0		NA	Reserved
0F	Reserved	7:0		NA	Reserved
10	TX_ADDR				
	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmitter's transmit address(LSByte is written first),if the transmit amplifier needs to receive the ACK acknowledgement signal,you need to configure the value of RX_ADDR_P0 to be equal to TX_ADDR,and enable the ARQ.
11	Reserved				
	Reserved	7	-	NA	Reserved
	Reserved	6:0	0	R/W	Reserved
12	Reserved				
	Reserved	7:6	-	NA	Reserved
	ADC_STATUS	5	-	R	Only when adc_status is 1,the temperature read is correct.
	Reserved	4:0	0	R/W	Reserved
13	Reserved				
	Reserved	7:0	0	R/W	Reserved
14	Reserved				
	Reserved	7:0	-	NA	Reserved
15	Reserved				
	Reserved	7:0	00000000	R	Reserved
16	Reserved				
	Reserved	7:0	00	NA	Reserved

17	FIFO_STATUS				FIFO state
	Reserved	7	0	R/W	Reserved，0
	TX_REUSE	6	0	R	Transmitter only,FIFO data reuse When the REUSE_TX_PL command is used,the data that has been successfully transmitted last time is emitted through the W_TX_PAYLOAD or FLUSH TX command disables the function
	TX_FULL	5	0	R	TX FIFO full flag 1:TX FIFO full 0:TX FIFO writable
	TX_EMPTY	4	1	R	TX FIFO empty flag 1:TX FIFO is empty 0:TX FIFO has data
	Reserved	3:0	0000	R/W	Reserved，0000
1C	DYNPD				Enable dynamic payload length
	Reserved	7:1	0		
	DPL_P0	0	0	R/W	1：Enable dynamic payload length
1D	FEATURE			R/W	Feture register
	Reserved	7:3	0	R/W	Reserved,00000
	EN_DPL	2	0	R/W	Enable dynamic payload length
	Reserved	1	0	NA	Reserved
	EN_DYN_ACK	0	1	NA	Enable command W_TX_PAYLOAD_NOACK

5.2 Receive related registers

Table 5-2 125kHz module related registers

Addr (Dec)	Mnemonic	Bit	Reset value	Type	Description
0	R0				
	PATT32	7	0	R/W	Match value extends to 32 bits(0 for

					16 bits,1 for 32 bits)
	DAT_MASK	6	0	R/W	Mask data on DAT pin before wake-up(0 unmask,1 mask)
	ON_OFF	5	0	R/W	ON/OFF mode enable
	MUX_123	4	0	R/W	Scanning mode enable
	EN_A2	3	1	R/W	Channel 2 enable
	EN_A3	2	1	R/W	Channel 3 enable
	EN_A1	1	1	R/W	Channel 1 enable
		0	0	R	Reserved
1	R1				
	ABS_HY	7	0	R/W	Enable absolute threshold for data slice comparator
	AGC_TLIM	6	0	R/W	AGC time-limited operation 1：Operate only within 256us of frequency detection 0：Always working after frequency detection(in the period of carrier triggered)
	AGC_UD	5	1	R/W	1:the AGC can increase or decrease the gain; 0:AGC reduces gain only
	ATT_ON	4	0	R/W	Antenna damper enable
	EN_MANCH	3	1	R/W	Manchester decode enable
	EN_PAT2	2	0	R/W	Double wake-up match value check
	EN_WPAT	1	1	R/W	Validator enable
	EN_XTAL	0	0	R/W	Crystal oscillator enable
2	R2				
	S_ABS	7	0	R/W	Absolute threshold reduction for data slice comparator
	EN_EXT_CLK	6	0	R/W	External clock enable
	G_BOOST	5	0	R/W	Amplifier gain increase
	VB3_D	4	0	R/W	Bias voltage vb3 decrease

	DISPLAY_CLK	3:2	00	R/W	11:The frequency of the clock generator is sent to the pin CL_DAT,also requires R16<7>=1
	S_WU1	1:0	00	R/W	Fault tolerance setting for frequency detection
3	R3				
	HY_20m	7	0	R/W	Hysteresis voltage of the data slice comparator（0:40mV，1:20mV）
	HY_POS	6	0	R/W	The hysteresis of the data slice comparator occurs at positive edge(0:positive and negative edge,1:positive edge)
	FS_SLC	5:3	100	R/W	Time constant of data slice comparator
	FS_ENV	2:0	000	R/W	Time constant of the demodulator
4	R4				
	T_OFF	7:6	00	R/W	Off time in ON/OFF mode 00：1ms；01：2ms； 10：4ms；11：8ms；
	D_RES	5:4	01	R/W	Antenna damper resistor
	GR	3:0	0000	R/W	Gain attenuation
5	R5				
	PATTA_2B	7:0	01101001	R/W	Wake-up match value A low byte
6	R6				
	PATTA_1B	7:0	10010110	R/W	Wake-up match value A high byte
7	R7				
	T_OUT	7:5	000	R/W	Automatic timeout time setting
	T_HBIT	4:0	01011	R/W	Bit duration definition
8	R8				
	BAND_SEL	7：5	000	R/W	Band selection
	T_AUTO	2：0	000	R/W	Artificial wake-up

					000：Disable； 001：1s； 010：5s； 011：20s； 100：2min； 101：15min； 110：1 hour； 111：2 hour；
9	R9				
	BLOCK_AGC	7	0	R/W	N.A.AGC
		6：0	0	R	Reserved
10	R10				
	RSSI1	4：0	0	R	RSSI value for channel 1
11	R11				
	RSSI2	4：0	0	R	RSSI value for channel 2
12	R12				
	RSSI3	4：0	0	R	RSSI value for channel 3
13	R13				
	F_WAKE	7：0	0	R	false wake-up register
14	R14				
	RC_CAL_OK	7	0	R	RC oscillator calibration success
	RC_CAL_KO	6	0	R	RC oscillator calibration fali
	RC_OSC_TAPS	5：0	0	R	RC oscillator calibration configuration
15	R15				
		7：5	0	R	Reserved
	LC_CAL_OK	4	0	R	LC oscillator working
	LC_CAL_KO	3	0	R	LC oscillator not working
		2：0	000	R	Reserved
16	R16				
	CLOCK_GEN_DIS	7	0	R/W	Display the output signal of the clock generator on pin CL_DAT,while it is

					necessary to set R2<3:2>=11
		6	0	R	Reserved
	RC_OSC_MIN	5	0	R/W	RC oscillator set to min frequency
	RC_OSC_MAX	4	0	R/W	RC oscillator set to max frequency
		3	0	R	Reserved
	LC_OSC_MUX3	2	0	R/W	Display the resonant frequency of the LF3P on the pin DAT
	LC_OSC_MUX2	1	0	R/W	Display the resonant frequency of the LF2P on the pin DAT
	LC_OSC_MUX1	0	0	R/W	Display the resonant frequency of the LF1P on the pin DAT
17	R17				
		7：5	0	R	Reserved
	CAP_CH1	4：0	00000	R/W	Tuning capacitor value setting for channel 1
18	R18				
		7：5	0	R	Reserved
	CAP_CH2	4：0	00000	R/W	Tuning capacitor value setting for channel 2
19	R19				
		7：5	0	R	Reserved
	CAP_CH3	4：0	00000	R/W	Tuning capacitor value setting for channel 3
20	R20				
	Reserved				
21	R21				
		7：5	0	R	Reserved
	GBOOST	4	0	R/W	1:Amplifier gain boost(R2<5>must be 1)
	START_I_XTAL	3	0	R/W	Setting the crystal oscillator starting

					current
	I_XTAL	2：0	000	R/W	Setting the crystal oscillator current loss
22	R22				
		7：4	0	R	Reserved
	RC_OSC_TAPS_EXTD	3：0	0000	R	Extend RC oscillator calibration control bits
23	R23				
	si_frame_en	7	1	R/W	si_frame_en 1：Single frame data 0：Double frame data
	si_source_en	6	1	R/W	si_source_en 1：Single emission source 0：Dual emission source
	in_out_en	5	1	R/W	in_out_en 1：Single side door 0：In and out direction judgment
	en_125k	4	0	R/W	en_125k 1:disable 125k wake up 2f 0:enable125k wake up 2f
		3：0	0	R	Reserved
24	R24				
	PATTB_2B	7：0	01011010	R/W	Wake-up match value B low byte
25	R25				
	PATTB_1B	7：0	10100101	R/W	Wake-up match value B high byte
26	R26				
		7：5	0	R	Reserved
	wl_rssi	4：0	0	R/W	Program signal strength threshold,larger than this value can program
27	R27				
	Blue_en	7	1	R/W	BLE bluetooth frame enable

					0：enable 1：disable
	Reserved	6	0		Reserved
	BLUE_INDEX	5:0	00000	R/W	Bluetooth channel

6 Wireless transmit packet processing protocol

The Si24R2H is based on packet communication and transmits packets in the same format as the Si24R1.The baseband processing engine is integrated inside the chip,which can realize the packet processing automatically without the intervention of external microcontroller.The baseband processing unit supports 1 to 32 byte dynamic data length;data length is in the packet.Fixed data length can also be used,which is specified through registers;the baseband processing unit accomplishes automatic unpacking and packing of data.The processing unit has a 3-stage FIFO and can transmit 3 packets of data at a time.

6.1.1 Packet format

A whole packet contains a preamble,address,packet control,payload and CRC field.Figure 6.1-1 shows the packet format with MSB to the left.

Preamble	Address	Packet control	Payload	CRC

Figure 6.1-1 A whole ARQ packet

The preamble is used to synchronize the receivers demodulator to the incoming bit stream.It is automatically attached when transmitting and added by transmitter and discarded by receiver,and shielded for users.

The address field stores the packet address values for the receiver.A packet will be received only when the address of the packet matches the address of the receiver.The address field width in the AW register can be configured to be 3,4 or 5 bytes.

Figure 6.1-2 shows the format of the 9 bit packet control field.

Payload length 6bit	PID 2bit	NO_ACK 1bit

Figure 6.1-2 Format of packet control field

The 6 bit payload length specifies the length of the payload in bytes.The length of the payload can be from 0 to 32 bytes.

For example：000000=0 byte(no payload)

100000=32 byte(32 bytes of payload)

The PID field is used to detect if the received packet is new or retransmitted.PID

prevents the PRX device from presenting the same payload more than once.The PID field is incremented at the TX side for each new packet received and write FIFO through the SPI.

When NO_ACK bit is 1,it indicates telling the receiver that the packet is not to be auto acknowledged.For the transmitter,to set NO_ACK bit high must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit,and set the NO_ACK flag bit in the packet control field with this command:W_TX_PAYLOAD_NOACK.The PRX does not transmit an ACK packet when it receives this packet,even if it is working in ACK mode.The payload is the user defined content of the transmitted packet.It can be up to 32 bytes.

The CRC field is the CRC value of the packet,CRC supports 8bit and 16bit.16bit can be 2bytes,2bytes_8005,2bytes_sp.The CRC field is the CRC value of the packet.8bit and 16bit CRC are supported.16bit CRC can be 2bytes,2bytes_8005,2bytes_sp.If you want to configure the number of 2H sends by MCU through SPI,the number of bytes of CRC can be configured directly through register CRCO,and the type of CRC needs to be configured through NVM.

6.1.2 Communication mode

In the TX mode the PTX device assembles the preamble,address,packet control field,payload and CRC to make a complete packet first and then transmits the packet with RF module.

6.1.2.1 NO ACK mode

On the PTX you can set the NO_ACK flag bit in the Packet Control Field with this command:W_TX_PAYLOAD_NOACK.After sending a packet of data,generates TX_DS interrupt immediately,and start to prepare transmitting next packet of data.After receiving data,the PRX checks if the NO_ACK flag is set and the data is valid,then generates RX_DR interrupt.It is means that a frame of data communication is finished and the PRX does not need to transmit an ACK packet.

6.1.2.2 Dynamic payload length(DPL)and static payload length

A PTX device with DPL enabled must have the EN_DPL bit in FEATURE register and the DPL_P0 bit in DYNPD register set.The first 6 bits in the control field of the packaged data are

the length of the data for sending.

The PRX set the EN_DPL bit in FEATURE register,and enable the pipe of DYNPD register.It will receive data according to the length control field.Thus,every time when receiving payload data,its length can be different.MCU can read out the payload length by using R_RX_PL_WID command.If it is static payload length by default,the payload length on the transmitter side must be the same every time,and must equal the value in the RX_PW_Px register on the receiver side.

6.1.3 Compatibility mode

The Si24R2H can provide an alternative packet format that is sent out as follows：

Figure 6.1-3 Compatibility mode packet format

In compatibility mode,you need to set register EN_AA=0,which does not support dynamic load length mode,and set DPL_Px=0 and EN_DPL=0.In compatibility mode,the receiver needs to set RX_PW_Px to the value of packet length sent by the sender,and set DPL_Px=0 and EN_DPL=0.In addition,the data rate can only be set to 1 Mbps or 250 kbps.In addition,the data rate can only be set to 1Mbps or 250kbps.

6.1.4 BLE Bluetooth packet format

The Si24R2H can send BLE Bluetooth packets(Txpayload),Bluetooth packets are only available in compatibility mode,the packet includes the leading code,address,load data,and CRC,and is compatible with BLE4.2.The broadcast address is fixed to 0x6B7D9171.the packet has a minimum length of 10 bytes and a maximum length of 40 bytes.

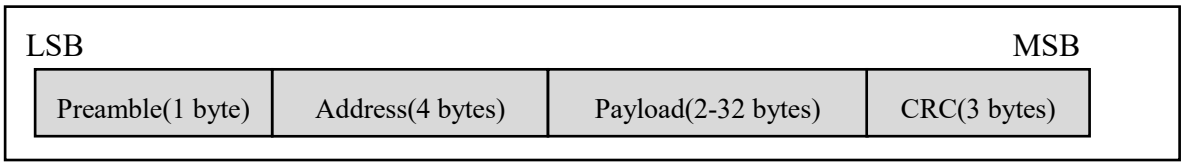


Figure 6.1-4 BLE-Bluetooth packet format

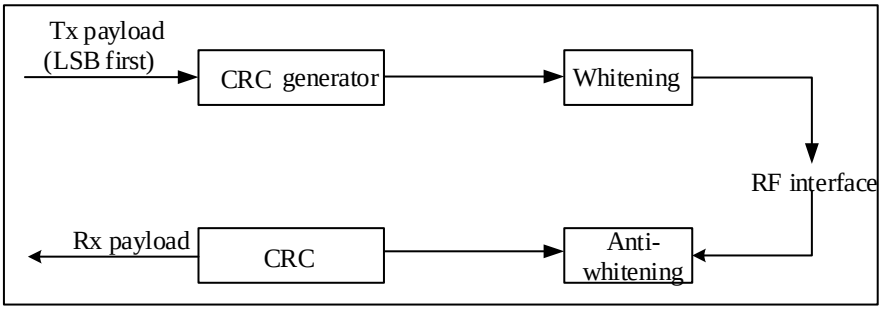


Figure 6.1-5 BLE Bluetooth packet data flow

Write register BLUE_EN=1 Enable Bluetooth function,BLE Bluetooth channel can be passed through register BLUE_INDEX to config options.The mapping of data channels,broadcast channels,and RF channels for BLE Bluetooth is shown in Table 6-1.

Table 6-1 BLE Bluetooth channel and RF channel mapping

RF channel	RF center frequency	Channel Type	Data channel index	Broadcast channel index
0	2402 MHz	broadcast channel		37
1	2404 MHz	data channel	0	
2	2406 MHz	data channel	1	
.....	.....	data channel		
11	2424 MHz	data channel	10	
12	2426 MHz	broadcast channel		38
13	2428 MHz	data channel	11	
14	2430 MHz	data channel	12	
.....	.....	data channel	.....	
38	2478 MHz	data channel	36	
39	2480 MHz	broadcast channel		39

7 Wireless wake-up and receiving

A three-channel,low-power ASK receiver for detecting digital signals at low-frequency carrier frequencies of 15kHz-150kHz and generating wake-up signals.An integrated internal checker detects wake-up matches in 16-bit or 32-bit Manchester encoding and supports two repetitions of the match check.

The receiver can operate with one,two or three channels,each with frequency detection and digital RSSI calculation.The sensitivity of the channels is adjustable,allowing longer communication distances and adaptation to noisy environments.

The receiver has an internal clock generator and can optionally use a crystal oscillator or an RC oscillator.The user can also choose to use an external clock.

The receiver supports programmable data rates and Manchester decoding with clock recovery.The auto-tuning feature ensures a perfect match between the chip and the desired carrier frequency,greatly simplifying antenna tuning.

7.1 Channel amplifier

Each of the 3 channels consists of a variable gain amplifier(VGA)with automatic gain control(AGC)and a frequency detector.When in listening mode(waiting for RF signal),the gain of all channel amplifiers is set to maximum.The frequency detector counts the zero crossing of the amplified RF signal to detect the presence of the wanted carrier.After the frequency detection is complete,the AGC starts working.The RSSI(Received Signal Strength Indicator)represents how strong the input signal is and it is the inverse representation of the gain of the VGA.In fact,if for example the input signal is very strong the AGC will reduce the gain of the VGA and the RSSI will be larger.

The receiver can work between 15 kHz and 150 kHz.Once the carrier frequency has been chosen the user must set the amplifier working in the appropriate frequency band using the bits R8<7:5>,as described in the table 7-1.

It is possible to boost the gain of the amplifiers,as R2<5>=1.In case the lowest frequency band is used(15kHz-40 kHz)the gain boost is automatically enabled from the logic.

The amplifier gain continues to increase when R21<4>=1（The premise is R2<5>must be 1）.

It is possible to enable/disable individual channels,in case not all three channels are needed.This enables to reduce the current consumption by 1.5uA(typical)per channel.

7.1.1 Frequency detector

The frequency detection is based on a zero crossing counter and uses the Clock Generator as time base.The Clock Generator generates time windows equal to N times its period.The frequency detection is successful if in two consecutive time windows the zero threshold counter detects M zero crossing(Because the frequency of the clock is determined by the carrier frequency,the number of the zero threshold in a time window is certain).N depends on the operating frequency band,as shown in the Table 7-1.M depends also on the operating frequency range,the frequency detection criteria can be tighter or more relaxed according to the setup described in R2<1:0>(see Table 7-2,7-3).

Table 7-1 Operating frequency and N value

R8<7>	R8<6>	R8<5>	N	Operating frequency range/kHz
0	0	0	4	95-150
0	0	1	6	65-95
0	1	0	10	40-65
0	1	1	18	23-40
1	1	1	14	15-23

Table 7-2 M value for for frequency detection in the bands 23 kHz-150kHz

R2<1>	R2<0>	M
0	0	16±6
0	1	16±4
1	0	16±2
1	1	N.A.

Table 7-3 M value for frequency detection in the bands 15-23 kHz

R2<1>	R2<0>	M
0	0	8±3

0	1	8±2
1	0	8±1
1	1	N.A.

7.1.2 RSSI calculation

The AGC starts working after the frequency detection.At the beginning the gain in the VGA is set to maximum and the AGC reduce it according to the received signal input level.The AGC needs maximum 35 carrier periods to settle,getting a stable RSSI.

The AGC can operate in two modes:AGC down only(R1<5>=0),AGC up and down(R1<5>=1).If the AGC down only mode is selected,the AGC can only decrease the gain for the whole duration of the data reception.In this mode the system holds the RSSI peak.When the AGC up and down mode is selected,the RSSI can dynamically follow the input signal strength variation in both directions.

The RSSI is available for all 3 channels at the same time and it is stored in 3 registers(R10<4:0>、R11<4:0>、R12<4:0>).Once the RSSI gets stable,the channel selector compares which channel receives the strongest RSSI and freezes the channels which have the smaller RSSI.From this time on the AGC is active only on the selected channel.

Both AGC modes(only down or down and up)can also operate with time limitation.This option allows AGC operation only in time slot of 256 μ s after the frequency detection(during carrier burst),then the RSSI is frozen till the wake-up or RSSI reset occurs(direct command clear_wakeup or reset_RSSI).

The RSSI is reset either with the direct command'clear_wakeup'or'reset_RSSI'.The'reset_RSSI'command resets only the VGA setting but does not terminate wake-up frequency detection condition.This means that if the signal is still present the new AGC setting(RSSI)will appear not later than 35 LF carrier periods after the command was received.The AGC setting is reset during data receiving if for duration of 3 Manchester half symbols no carrier is detected.

In case the maximum amplification at the beginning is a drawback(e.g.in noisy environment)it is possible to set a smaller starting gain on the amplifier,according to the Table 7-4.In this way it is possible to reduce the false frequency detection.

Table 7-4 Attenuation of initial gain

R4<3>	R4<2>	R4<1>	R4<0>	Gain attenuation
0	0	0	0	0
0	0	0	1	N.A.
0	0	1	0 or 1	N.A.
0	1	0	0 or 1	-4dB
0	1	1	0 or 1	-8dB
1	0	0	0 or 1	-12dB
1	0	1	0 or 1	-16dB
1	1	0	0 or 1	-20dB
1	1	1	0 or 1	-24dB

In case the chip needs to deal with higher field strengths the antenna damper can be enabled(R1<4>=1).The antenna damper consists of internal resistors which can be connected in parallel to the external resonator as shown in Figure 7-1.The value of the resistor can be adjusted with the bits R4<5:4>as shown in Table 7-5.The shunt resistors degrade the quality factor of the external resonator by reducing the signal at the input of the amplifier.In this way the resonator sees a smaller parallel resistance(in the band of interest)which degrades its quality factor in order to increase the linear range of the channel amplifier(the amplifier doesn't saturate in presence of bigger signals).

Table 7-5 Antenna damper resistance setting

R4<5>	R4<4>	Shunt resistor
0	0	1 kΩ
0	1	3 kΩ
1	0	9 kΩ
1	1	27 kΩ

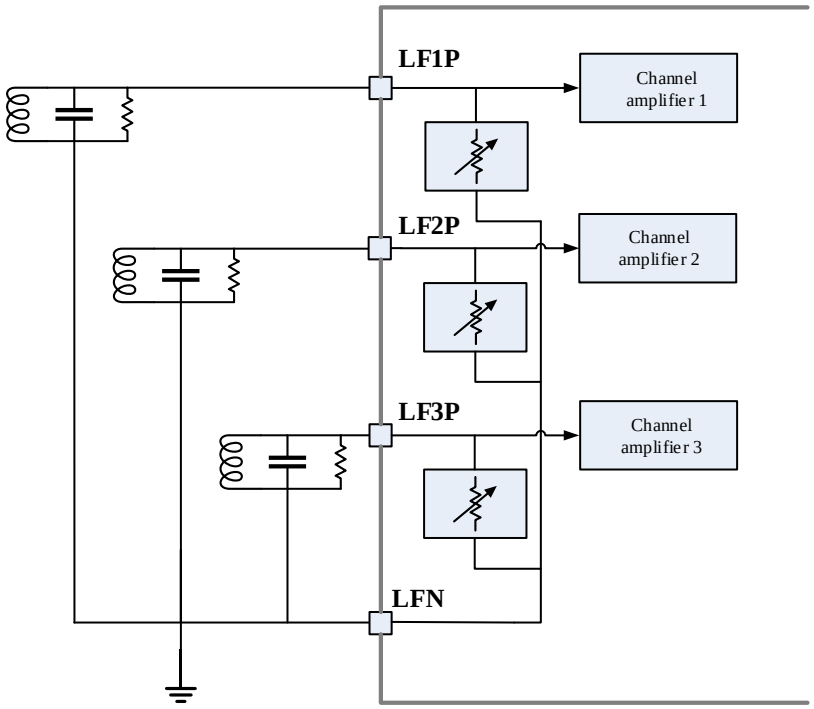


Figure 7.1-1 Antenna damper

7.2 Demodulator/data slicer

As soon as the 125K frequency detects successfully the frequency and the RSSI has got stable(not later than 35 LF carrier periods)the channel selector compares the RSSI on all active channels and connects the channel amplifier which has the biggest RSSI to the demodulator.The channel selector needs 32 RF carrier periods to take this decision.The output signal(amplified LF carrier)of selected channel is connected to the input of the demodulator.

A concept block diagram is shown in the Figure 7.2-1.The demodulator takes the signal to base-band and recovers two signals from the amplified RF signal;a fast and a slow envelop.Those two signals are fed to the data slicer,which is a comparator with programmable hysteresis.At the output of the data slicer are streamed the digital received bits as shown in Figure 7.2-2.

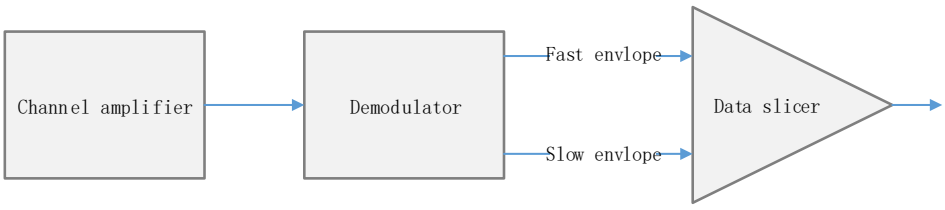


Figure 7.2-1 Demodulator and data slicer

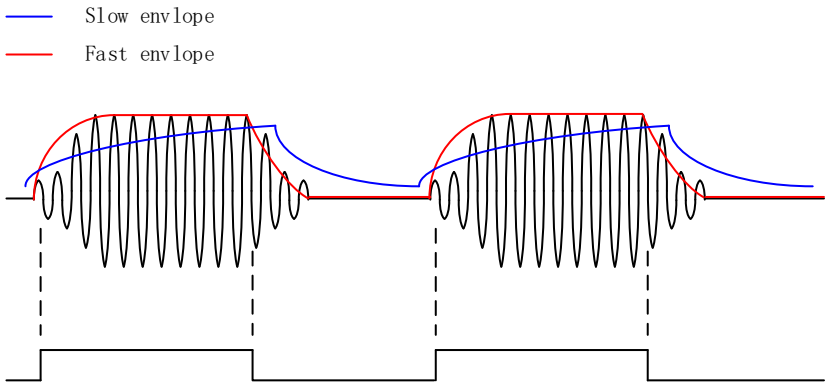


Figure 7.2-2 Envlope detector signals-dynamic threshold

The performance of the demodulator can be optimized according to bit rate and preamble length.On one hand the fast envelope's time constant(R3<2:0>)needs to be adjusted to the desired symbol rate as shown in Table 8-1.However,decreasing the fast envelope's time constant also means that more noise will be injected due to the wider band.On the other hand,the slow envelop signal acts as an average of the incoming data.Therefore,the bigger its time constant is,the better will be the noise rejection.Yet,a bigger time constant of the slow envelop(R3<5:3>)requires a longer preamble in order to settle to the correct value.The minimum preamble length as a function of the slow envelope's settings is given in Table 7-7.

Table 7-6 Bit setup of the fast envelope for different symbol rates

R3<2>	R3<1>	R3<0>	Symbol rate（Manchester Symbols/s）
0	0	0	4096
0	0	1	2184
0	1	0	1490
0	1	1	1130
1	0	0	910
1	0	1	762
1	1	0	655
1	1	1	512

Table 7-7 Minimum required preamble lengths as function of slow envelop settings

R3<5>	R3<4>	R3<3>	Minimum preamble length

			（ms）
0	0	0	0.8
0	0	1	1.15
0	1	0	1.55
0	1	1	1.9
1	0	0	2.3
1	0	1	2.65
1	1	0	3
1	1	1	3.5

With the bits R3<7:6>it is possible to change the hysteresis on the data slicer comparator.If R3<7>=0,then the comparator hysteresis is 40mV else comparator hysteresis is 20mV.If R3<6>=0,then data slicer hysteresis on both edges else data slicer hysteresis only on positive edges.

The slow envelop signal(blue signal in Figure 7.2-2)represents the average of the demodulated signal,therefore acts as a reference signal for the data slicer.In case the chosen protocol has a duty cycle far away from 50%(for example in the NRZ protocol there can be several consecutive ones or zeros)the slow envelop signal would not be a stable reference signal for the data slicer.In this case the data slicer can also work with an absolute threshold R1<7>=1),as shown in the Figure 7.2-3.It is even possible to reduce the absolute threshold in case the environment is not particularly noisy(R2<7>=1).

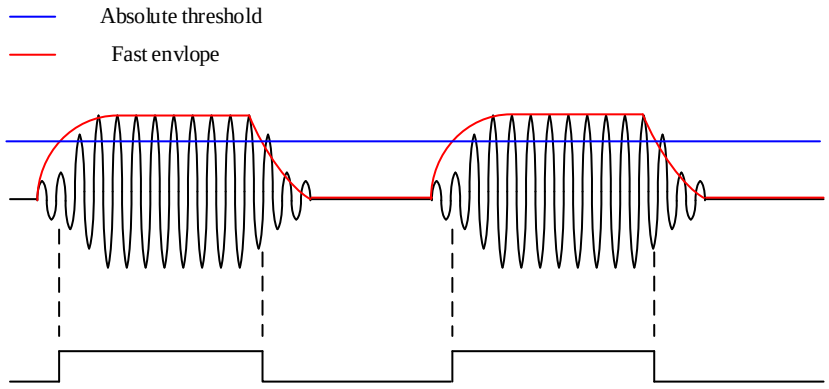


Figure 7.2-3 Envelop detector signals-absolute threshold

As the input signal may be damped due to physical influences of the transmitter environment,the symbol rate needs to be adapted(lowered)if absolute threshold is enabled to

ensure a proper detection of the wake-up signal.The peak level of the signal should be reached within 1/3 of the symbol duration which is defined as two times the bit duration.The bit duration is defined in register R7<4:0>as a function of the Clock Generator periods,as shown in the Table 7-8.

Table 7-8 Bit setup of bit duration and clock period

R7<4>	R7<3>	R7<2>	R7<1>	R7<0>	Bit duration in clock periods
0	0	0	1	1	4
0	0	1	0	0	5
0	0	1	0	1	6
0	0	1	1	0	7
0	0	1	1	1	8
0	1	0	0	0	9
0	1	0	0	1	10
0	1	0	1	0	11
0	1	0	1	1	12
0	1	1	0	0	13
0	1	1	0	1	14
0	1	1	1	0	15
0	1	1	1	1	16
1	0	0	0	0	17
1	0	0	0	1	18
1	0	0	1	0	19
1	0	0	1	1	20
1	0	1	0	0	21
1	0	1	0	1	22
1	0	1	1	0	23
1	0	1	1	1	24
1	1	0	0	0	25
1	1	0	0	1	26
1	1	0	1	0	27
1	1	0	1	1	28
1	1	1	0	0	29

1	1	1	0	1	30
1	1	1	1	0	31
1	1	1	1	1	32

7.3 Wake-up protocol and manchester decoder

7.3.1 Wake-up protocol

125K receiver can support protocols below：

1、Single pattern detection,include 16-bit pattern and 32-bits pattern；

2、Double pattern detection(repeat once),include 16-bit pattern and 32-bits pattern.

The wake-up state can be terminated either by the host system(MCU)with the direct command‘clear_wake’sent over SPI or with a time-out option.In case the latter is used the host system(MCU)does not need to take any action to terminate the wake-up state and the chip is set back to listening mode automatically after a predefined time.It is possible to set the duration of the time-out with the register R7<7:5>,as shown in the Table 7-9.

Table 7-9 Timeout setting

R7<7>	R7<6>	R7<5>	Time out
0	0	0	Disabled
0	0	1	50ms
0	1	0	100ms
0	1	1	150ms
1	0	0	200ms
1	0	1	250ms
1	1	0	300ms
1	1	1	350ms

In case the pattern correlation is disabled(R1<1>=0)the 125k receiver wakes up upon detection of the carrier frequency only as shown in Figure 7.3-1.The minimum duration of the carrier burst in order to ensure that 125k wakes up and the RSSI is settled is specified in the Table 7.3-2.In addition the carrier burst does not have to be longer than 155 periods of the

Clock Generator(Crystal oscillator or RCO or External Clock).As shown in the Figure 3.2-1,the 125k after the detection of the carrier goes directly from the Listening mode to Data receiving mode after settling the RSSI.

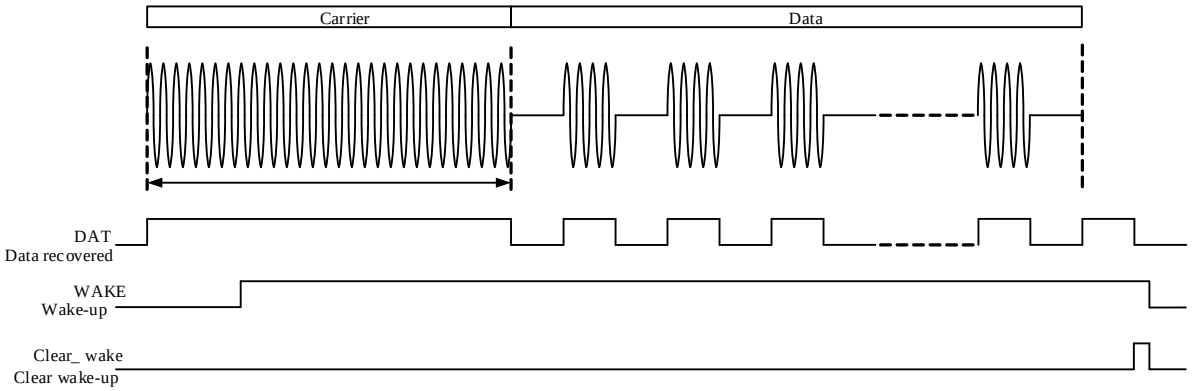


Figure 7.3-1 Wake-up process with frequency detection only

Table 7-10 Minimum duration of the carrier burst

Operating frequency range（kHz）	Minimum duration of the carrier burst
95-150	16Tclk+16Tcarr
65-95	28Tclk+16Tcarr
40-65	52Tclk+16Tcarr
23-40	96Tclk+16Tcarr
15-23	92Tclk+8Tcarr

Note：Tclk is the period that clock generator generated，Tcarr is the period of carrier

In case the pattern correlation is enabled(R1<1>=1)the 125k receiver generates a wake-up interrupt if the wake-up protocol is fulfilled,as shown in the Figure 7.3-2.The communication protocol consists of a carrier burst,a preamble(0101010…)and the 16-bit pattern.In case the double pattern option is enabled(R1<2>=1)the 16-bit pattern has to be repeated 2 times consequentially(2 times the same pattern).The signal on the WAKE pin goes high one bit after the end of the pattern and the data transmission can get started.

The minimum length for the carrier burst depends on the operating frequency range and is described in the Table 7-11.If the carrier burst is shorter than what has been specified in the Table 7-11,then the frequency detection is not guaranteed.In order to fulfill the protocol the carrier burst must be shorter than 155 periods of the clock generator(crystal oscillator or RCO

or external clock).The carrier burst must be followed by a separation bit and at least 6 bits preamble(101010).The separation bit must last as half Manchester symbol.The preamble and the pattern cannot be longer than 30 symbols in sum in case 16-bit pattern detection is enabled and 46 symbols if the 32-bit pattern detection is enabled.

In case the ON/OFF option is enabled(R0<5>=1)the minimum duration of the carrier burst must be prolonged by the OFF time defined in the R4<7:6>.

Should the carrier burst be longer than what is defined in the Table 7-11 or the number of preamble bits longer than what has been specified above a false wake-up event might be recorded in the register R13<7:0>.

If the Scanning Mode be enabled(R0<4>=1)the minimum duration of the carrier burst is defined in the Table 7-11.

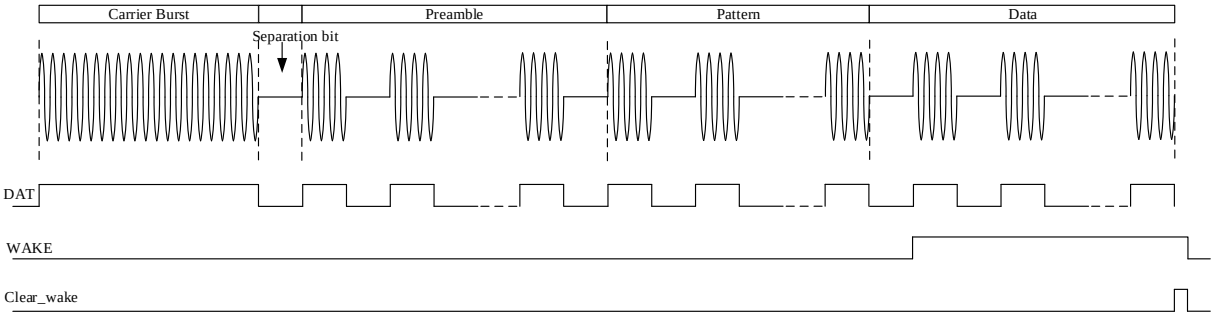


Figure 7.3-2 Wake-up protocol overview if pattern detection is enabled

Table 7-11 Minimum duration of the carrier burst in scanning mode

Operating frequency range （kHz）	Minimum duration of the carrier burst
95-150	80Tclk+16Tcarr
65-95	92Tclk+16Tcarr
40-65	180Tclk+16Tcarr
23-40	224Tclk+16Tcarr
15-23	220Tclk+8Tcarr

Note：Tclk is the period that clock generator generated，Tcarr is the period of carrier

7.3.2 Correlator

In order to prevent the 125K from falsely waking up the 2.4G due to noise and

interference,an internal verifier checks whether the bit sequence coming from the data splitter corresponds to the stored match value.r1<1>=1 is the verifier enable signal,and the verification is performed only after the frequency detection.The match check is only successful(generates a WAKE signal)if both the bit sequence(match value)and its timing(duration of individual bits)match.The chip stores two Pattern match values,the desired PatternA in R5<7:0>(low byte)and R6<7:0>(high byte)and the desired PatternB in R24<7:0>(low byte)and R25<7:0>(high byte).Either PatternA or PatternB can wake up.

125K is able to check the input match value.The match value must be in Manchester code form.In Manchester code,each"symbol"consists of two"bits"(bit 1-0 for symbol 1 and bit 0-1 for symbol 0).Figure 7.3-3 shows Manchester encoding process of 3 symbols(101).In a Manchester-encoded bit stream,three consecutive 0s or 1s are not possible,which helps to recover the clock signal.

The bit duration is a function of the clock generator period,defined by R7<4:0>,see Table 7-8.

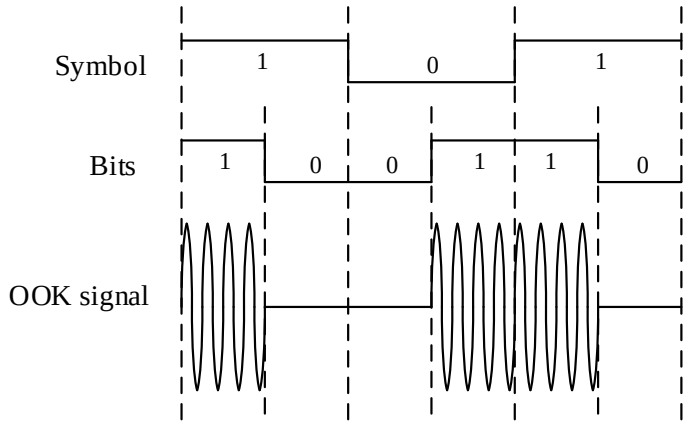


Figure 7.3-3 Manchester encoding

The user can define the pattern to correlate in the registers R5<7:0>and R6<7:0>and can decide whether the stored pattern is a bit representation(16 Manchester bits corresponds to 8 Symbols)if R0<7>=0 or the symbol representation(16 symbols corresponds to 32 bits)of the pattern if R0<7>=1.The number of different pattern is 2^SYM,where SYM is the number of Manchester symbols.In case the R5 and R6 represent the bit sequence of the pattern there are 256 different possible combinations,while in case they are the symbol representation there are 65536 different patterns.

7.3.3 False wake-up register

The wake-up strategy in the 125K is based on 2 steps:

1. Frequency Detection:In this phase the frequency of the received signal is checked.

2. Pattern Correlation:Here the pattern is demodulated and checked whether it corresponds to the valid one.

If there is a disturber or noise capable to overcome the first step(frequency detection)without producing a valid pattern,then a false wake-up call happens.Each time this event is recognized a counter is incremented by one and the respective counter value is stored in a memory cell(false wake-up register).Thus,the microcontroller can periodically look at the false wake-up register,to get a feeling how noisy the surrounding environment is and can then react accordingly(e.g.reducing the gain of the LNA during frequency detection,set the 125K temporarily to power down etc.),as shown in the Figure 7.3-4.The false wake-up counter is a useful tool to quickly adapt the system to any changes in the noise environment and thus avoid false wake-up events..

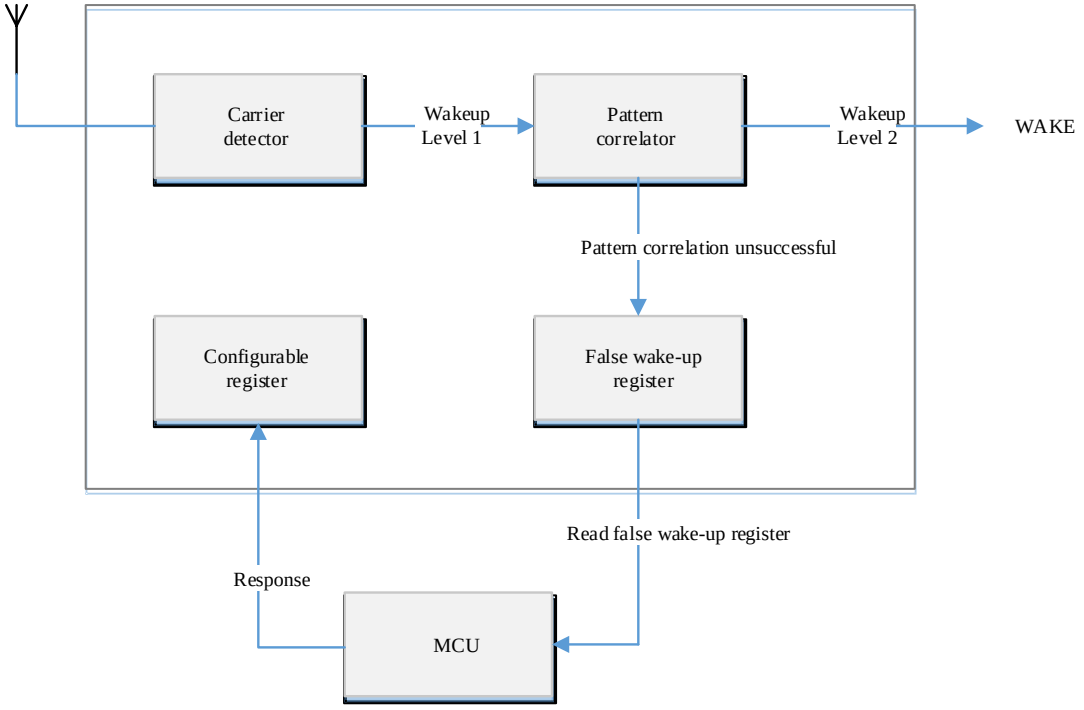


Figure 7.3-4 false wake-up register

7.3.4 Manchester decoder and clock recovery

In case the Manchester decoder is enabled(R1<3>=1)the 125k decodes the incoming Manchester bits automatically and the Manchester decoded data are displayed on the DAT pin and the Manchester recovered clock on the CL_DAT.The data coming out from the DAT pin are stable on the rising edge of the CL_DAT clock,as shown in Figure 7.3-5.

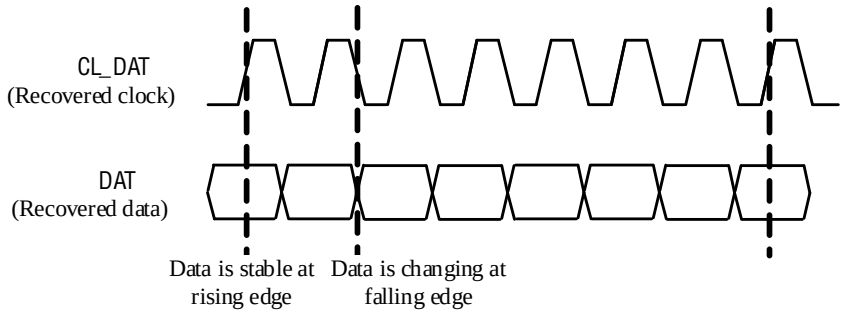


Figure 7.3-5 Manchester encoding with clock recovery

In case a Manchester timing violation happens,the signal on SPO goes high for a duration of 4 periods of internal clock(either crystal oscillator or RCO or external clock).

7.4 Clock generator

7.4.1 Overview

The Clock generator can be based on a crystal oscillator(R1<0>=1),the internal RC-oscillator(R1<0>=0),or an external clock source(R1<0>=1).The crystal oscillator has higher precision of the frequency with higher current consumption and needs three external components(crystal plus two capacitors).The RC-oscillator is completely integrated and can be calibrated to increase its precision.Should a digital clock already be available it can be applied directly to the XOUT pin(XIN to VCC).

Regardless which clock generator is chosen,the frequency of the Clock generator must be set according to the carrier frequency.Table 7-12 shows the dependency of the Clock generator frequency from the carrier frequency and operating frequency band.

Table 7-12 Clock generator frequency versus frequency band

Carrier frequency（kHz）	Clock frequency
95-150	$f = f_{carrier} \cdot \frac{1}{4}$
65-95	$f = f_{carrier} \cdot \frac{3}{8}$
40-65	$f = f_{carrier} \cdot \frac{5}{8}$
23-40	$f = f_{carrier} \cdot \frac{9}{8}$
15-23	$f = f_{carrier} \cdot \frac{14}{8}$

It is possible to display the frequency of the clock generator on the CL_DAT pin writing R2<3:2>=11 and R16<7>=1.

7.4.2 Crystal oscillator

In case the user decides to use the crystal oscillator as reference clock a 32.768kHz quartz can be used in case the tolerance setting for the frequency detection is relaxed(R2<1:0>=00).Should this not be the case,then Table 7-13 shows how the frequency of the quartz has to be chosen.

If working in the bandwidth 23-40kHz,then it is recommended not to use the XTAL oscillator to avoid any coupling between the input antennas and the quartz.

Table 7-13 Parameter of XTAL

Parameter	Conditions	Min	Typ	Max	Unit
Crystal motional resistance		-	-	60	KΩ
Minimum frequency	For 32.768kHz crystal	-	25	-	kHz
Typical frequency		-	32.768	-	kHz
Maximum frequency		-	45	-	kHz
Start-up time	Crystal dependent	-	1	-	s
Calibration time		45	50	55	%

Current consumption		-	300	-	nA

7.4.3 RC oscillator and RC calibration

7.4.3.1 RCOSC overview

Table 7-14 Parameters of RC oscillator

Parameter	Condition	Min	Typ	Max	Unit
Calibration time	Periods of reference clock	65	-	-	cycles
Current consumption		-	730	-	nA

In case the pattern detection and the Manchester decoder are not enabled(R1<1>=0 and R1<3>=0)the calibration on the RC-oscillator is not needed.If using pattern detection and the Mancheter decoder,then the RC oscillator has to be calibrated.

If RC oscillator turns off or the power-up reset happens(such as changing the battery)，then RC configuration maybe changed and must re-calibrate the RC oscillator.

The calibration of the RC-oscillator can be done in two different ways：

（1） Over SPI,the host system(MCU)has to be able to provide 65 clock pulses of a reference clock.In this case the host has to have a precise reference clock(quartz,resonator etc.).

（2） Using the internal calibration procedure based on the antenna resonator.Using this calibration method the RC-oscillator is automatically trimmed to the proper frequency,according to the operating frequency band.The precision of the calibration depends on the tolerances of the resonator of the first channel(LC connected to LF1P).

7.4.3.2 RCOSC calibration

A. Calibration via SPI

Calibration starts when 125K receives the direct command Calib_RCosc(trim_osc).

To calibrate the RC oscillator via SPI SCLK,the chip select pin(CSN)needs to be set low,and then the direct command TRIM_OSC must be sent via SPI.65 digital clocks(e.g.,125kHz/4=31.25kHz)of the reference clock must then be sent on the clock bus(SCLK),see Figure 7.4-1.After this,the chip select pin(CSN)must be pulled up.

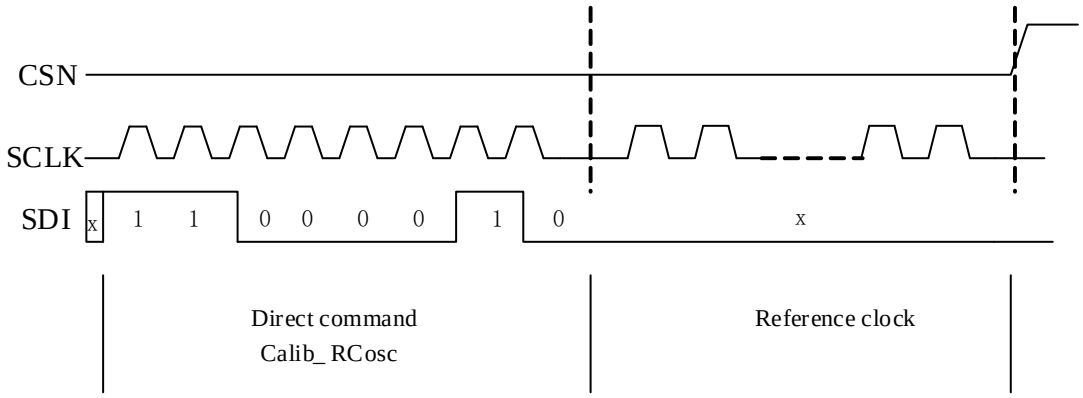


Figure 7.4-1 RC oscillator calibration via SPI

B. Calibration by LC

This procedure uses an LC circuit connected to channel 1(LF1P),which is not used as an antenna but as a resonator for an oscillator.The internal LC oscillator is connected to the external LC circuit via a multiplexer.

The LC oscillator generates a clock that coincides with the resonant frequency of the LC circuit.In a typical application,the user designs the external resonator so that the resonant frequency of the external LC circuit is as close as possible to the carrier frequency.The mathematical relationship between the oscillation frequency and the LC time constant is：

$$F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$

The RC oscillator starts to calibrate by sending the direct command Calib_RCO_LC via SPI.According to Table 7.4-1,the calibrated frequency of the RC oscillator depends on the carrier frequency and is automatically set to perform better frequency detection.

LC calibration procedure：

A. Calibrating with an LC requires ensuring that the LC is operational during calibration and that the LC oscillator is operating at flags R15<4>=1 and R15<3>=0.

B. Send the direct command Calib_RCO_LC via SPI,when R14<7>=1,the RC oscillation calibration is finished.

C. RC power-up self-calibration

0.8m(s)after turning on the RCOSC of the 125kHz receiver(31 clocks),which activates the 125kHz receiver RCOSC self-calibration,using the 2.4GHz transmitter's OSC clock to calibrate the 125kHz receiver's RCOSC.After a certain period of time,the calibration result was approximately 31.25khz.

If you do not want to use the RCOSC self-calibration function of the 125kHz receiver,you need to send a calibration command using SPI within 0.8ms(in this case,self-calibration will not be performed after the calibration command).It is also possible to re-calibrate after the self-calibration is completed by sending a calibration command using SPI.

125kHz receiver whose clock source is not RCOSC will not self-calibrate.

7.4.4 External clock source

Using an external signal as a clock for 125K requires enabling the external clock generator(R2<6>=1)and crystal oscillator(R1<0>=1).The external clock can be used directly via pin XOUT,in which case pin XIN must be connected to VCC.

Table 7-15 Parameters of extenal clock

Parameter	Min	Typ	Max	Unit
Low level	0	-	0.1*V_{CC}	V
High level	0.9*V_{CC}	-	V_{CC}	V
Rise-time	-	-	3	μs
Fall-time	-	-	3	μs

7.5 Antenna tuning

The 125K integrates a fine antenna tuning function internally.As shown in Figure 7.5-1,the 125K inplements the tuning function with the help of the host computer(MCU).

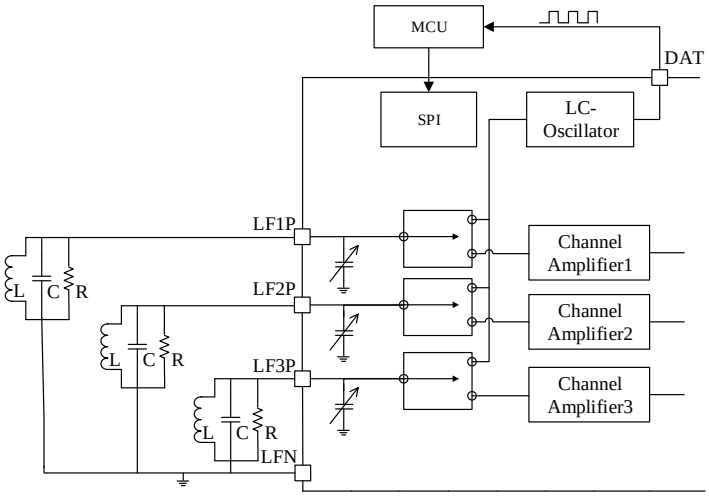


Figure 7.5-1 Tuning implementation

Each of the three antennas can be tuned with the internal capacitor banks.The capacitor can be connected or disconnected(adding or subtracting parallel capacitance to the external resonator)through registers R17<4:0>,R18<4:0>and R19<4:0>.The capacitance tuning range is 0~31pF and step into 1pF.

Table 7-16 Parallel tuning capacitance on LF1P

R17	Capacitance on LF1P
R17<0>=1	Add 1pF
R17<1>=1	Add 2pF
R17<2>=1	Add 4pF
R17<3>=1	Add 8pF
R17<4>=1	Add 16pF

Table 7-17 Parallel tuning capacitance on LF2P

R18	Capacitance on LF2P
R18<0>=1	Add 1pF
R18<1>=1	Add 2pF
R18<2>=1	Add 4pF
R18<3>=1	Add 8pF
R18<4>=1	Add 16pF

Table 7-18 Parallel tuning capacitance on LF3P

R19	Capacitance on LF3P
R19<0>=1	Add 1pF
R19<1>=1	Add 2pF
R19<2>=1	Add 4pF
R19<3>=1	Add 8pF
R19<4>=1	Add 16pF

The three channels can be tuned separately.The host system(MCU)has to connect the LC-oscillator to the antenna to measure the resonance frequency on the pin DAT.The host should measure the frequency on this pin and just changing register setting fine tune it to get it as close as possible to the nominal value of the carrier frequency.With the bits R16<2:0>it is possible to connect the LC-oscillator to the three different antennas.

Table 7-19 LC display channel select

Register bit	Parameter	Read-write type	Default	Description
R16<2>	LC_OSC_MUX3	R/W	1'b0	Output LF3P resonance frequency at the DAT pin
R16<1>	LC_OSC_MUX2	R/W	1'b0	Output LF3P resonance frequency at the DAT pin
R16<0>	LC_OSC_MUX1	R/W	1'b0	Output LF3P resonance frequency at the DAT pin

8 Wireless wake-up and transmit(entry and exit mode)

In addition to generating a single wake-up signal and receiving data,the 125kHz receiver can also be configured to generate wake-up signals to wake up the 2.4GHz transmitter to transmit different data under different circumstances.

Turn on wake-up 2.4G Transmit function(enableen_125k),125kHz receiver can wake up 2.4GHz transmit data after receiving a valid frame,and exit wake-up if no valid frame is received within the defined time(for wake-up timeout,auto timeout timeout expires).

8.1 Transmit substitution value

The 125k receiver can wake up the 2.4GHz transmitter to transmit the substitution value.You can use the following modes to define different wake-up methods for transmitting substitution packets.

1. **Single-frame data mode**

Single frame data mode is single transmitter source only(125k base station).Wake up 2.4G hz transmitter when received frame PATTA or PATTB match passes and RSSI strength meets RSSI setting range(can set RSSI max.min.)PATTA match wake up transmit wake up A substitution value PATTB match wake-up transmit wake-up B substitution value.

2. **Dual-frame data,single emitter source mode**

When the received frame PATTA or PATTB matches and the strength of the RSSI meets the RSSI setting range(the RSSI maximum minimum and difference can be set),close to the 125KHz transmitter source,the wake-up transmitter transmits the Wake-Up A substitution value.

Wake-up transmitter transmits a Wake-up B substitution value when the received frame PATTA or PATTB matches and the strength of the RSSI meets the RSSI setting range(RSSI Max Min and Difference can be set)away from the 125KHz transmitter source.

3. **Dual frame data,dual transmitter sources,single side gate mode**

his mode requires two transmitter sources(125k base stations).Both sources transmit frames containing a PATT that matches the chip memory PATT.One source transmits the frame containing the PATTA and the other source transmits the frame containing the PATTB.The two sources are placed on each side of the door,and the substitution values can be used to determine

which side of the door the tag is on.

When the strength of the RSSI meets the RSSI setting range and the tag is on the A side,the wake-up transmitter transmits the wake-up A substitution value.When the strength of the RSSI meets the RSSI setting range and the tag is on the B side,the wake-up transmitter transmits the wake-up B substitution value.

4. Dual frame data,dual transmitter sources,in/out direction judgment mode

This mode requires two transmitter sources(125k base stations).Both sources transmit frames containing a PATT that matches the chip memory PATT.One source transmits the frame containing the PATTA and the other source transmits the frame containing the PATTB. The two transmitting sources are placed on both sides of the door,so that the direction of the tags can be determined by the substitution of the transmitted values.

When the strength of RSSI meets the RSSI setting range,move from A side to B side,wake-up transmitter transmits wake-up A substitution value.

When the strength of the RSSI meets the RSSI setting range,move from the B side to the A side to wake up the transmitter to transmit wake-up B substitution value.

Note:PATTA is the wake-up A reference and PATTB is the wake-up B reference.

8.2 Transmit receive data

The 125K receiver can also wake up the 2.4G transmitter to transmit the received data,and can transmit the received valid data by satisfying any of the wake-up methods.Maximum support for transmitting 4 bytes of data.Dynamic and static modes can be selected.

a) Static mode:static length can be set,according to the number of bytes m(0<m<=4)set by the static length,the first m bytes of the received data will be transmitted as valid data,and the replacement position is optional.

b) Dynamic mode:Judge the number of valid data bytes to be transmitted by the low three bits of the first byte of the received data as the length of the received data(0<n<=4),and then transmit the next n bytes of data by substitution,and the position of substitution is optional.

Note:Replacement priority is lower than alarm replacement priority

8.3 Standby substitution

Using the wireless wake-up and transmit function,if the received data format does not conform to the Manchester encoding protocol after a single wake-up of the 125kHz,the chip will automatically use the CLEAR_WAKE command,the receiver register R7<7:5>defines the automatic timeout time to be invalidated,and the 125kHz will return to the listening mode to receive a new frame automatically.At this time,the wakeup timeout time is used as the timeout time for the wireless wakeup and transmit function.After exceeding the wake-up timeout time,125kHz does not have a valid receive frame,exits the wake-up transmitter,and the transmitter enters the standby mode.

The chip supports standby substitution and can set the standby transmit interval(standby transmit interval is N times of the transmit interval).When no valid frame is received,the 125k receiver does not wake up the 2.4G transmitter,and a packet of standby data frames will be sent at every time interval of the standby transmit interval,and you can choose whether to transmit the preset packet or the substitution packet through the configuration.

8.4 Transmit RSSI value

The chip can transmit the RSSI value detected by the receiver when the receiver wakes up the transmitter to send the number.

Select the Wake on 125k 2.4G Transmit function,select the RSSI replacement location,select transmit RSSI,and each time Wake on 125k 2.4G transmits,the 2.4G transmits the RSSI value at the RSSI Replacement Location at the time it was currently woken up by 125k.Without enabling Transmit RSSI,no RSSI value will be sent.

Replacement position priority:RSSI Replacement Position has the lowest priority.

For an rssi replacement value to be successfully emitted,the rssi replacement position needs to be before the receive data/receive replacement position,or the rssi replacement position must have an offset greater than 4 relative to the receive data/receive replacement position(receive data/receive replacement position before the rssi replacement position),but less than the transmitting payload length.

9 Sensor

Si24R2H has a built-in temperature sensor and multiple temperature sensor interfaces.Internal integrated 10bit digital temperature sensor,can measure the internal temperature of the chip,can be connected to an external NTC resistor to measure the external temperature of the chip,can also be plugged into the SHT21 temperature and humidity sensor and MLX90615 infrared temperature sensor,can realize the human body temperature measurement.

Temperature transmit function or temperature alarm function can be selected.Temperature Alarm Function:Transmits an alarm value at the 2.4G transmitter replacement location only if the temperature threshold is exceeded,and transmits a normal packet if the temperature threshold is not exceeded.Temperature transmit function:the temperature value measured by the corresponding sensor is transmitted at the 2.4G transmit replacement position.The measured value can be selected with or without alarm bit.

9.1 External SHT21 temperature and humidity measurement

9.1.1 Communication with SHT21

By plugging the Si24R2H chip into the SHT21 sensor via I2C and selecting SHT21 as the reference temperature and humidity for the temperature and humidity transmitter and temperature and humidity alarm functions,the Si24R2H will automatically read the temperature and humidity value measured by the SHT21 via I2C to realize the function of transmitting the temperature and humidity value of the SHT21 or the alarm value.

The SHT21 measures both temperature and humidity.Temperature alone,humidity alone,and humidity alternately can be selected.

The sensor sampling interval can be set up to be N times the hair count interval.

9.1.2 Transmit temperature and humidity values or alarm values

The temperature and humidity measured by the SHT21 read by the Si24R2H are all 14 bits.The transmit packet has temperature and humidity indication bits.The following shows the

relationship of the configuration to the transmit temperature/humidity/alarm values：

A. Selects the temperature transmit function and selects the transmit alarm bit

Transmit the low byte of the measured temperature/humidity first.

Then transmit{alarm bit 0/1,temperature and humidity indication bit,temperature/humidity high 6 bits}

(Alarm bits:1'b1 for exceeding temperature threshold range;1'b0 for within temperature threshold range)

(Temperature and humidity bits:1'b1 for humidity,1'b0 for temperature)

B. Select the temperature transmit function and select the do not transmit alarm bit

Transmit the measured temperature/humidity low byte first

Then transmit temperature/humidity high byte{0,temperature/humidity indicator bit,temperature/humidity high 6 bit}

(No alarm bit highest bit is 0)

C. Select temperature alarm function

If the temperature threshold is exceeded,the temperature alarm will be sent to replace the value;if the humidity threshold is exceeded,the humidity alarm will be sent to replace the value.

Note：

The actual temperature is calculated as:$T = -46.85 + 175.72 \times \frac{S_t}{2^{14}}$

The actual humidity is calculated as:$RH = -6 + 125 \times \frac{S_{RH}}{2^{14}}$

$S_t$is the temperature of transmission，$S_{RH}$is the humidity of transmission.

9.2 External MLX90615 temperature and humidity measurement

9.2.1 Communication with MLX90615

By putting the Si24R2H chip through an external MLX90615 sensor and selecting to use the MLX90615 as the reference temperature for the temperature transmitter function and the temperature alarm function,the Si24R2H will automatically read the temperature value measured by the MLX90615 through the I2C to realize the function of transmitting the MLX90615 temperature or alarm value.

Optional MLX90615 Measurement of target temperature/measurement of ambient temperature.

It is possible to set the sensor sampling interval to be N times the transmitter interval.To enable the MLX90615,the sampling interval needs to be greater than 0.35ms.

9.2.2 Transmit temperature value or alarm value

The temperature measured by the MLX90615 read by the Si24R2H is typically 15 bits.The following configuration and launch temperature/humidity/alarm value relationship：

A. Selects the temperature transmit function and selects the transmit alarm bit

Transmit the low byte of the measured temperature first

Then transmit{alarm bit 0/1,temperature high 7 bits}

(Alarm bits:1'b1 for exceeding temperature threshold range;1'b0 for within temperature threshold range)

B. Select the temperature transmit function and select the do not transmit alarm bit

Transmit the measured temperature low byte first

Then transmit the measured temperature high byte

C. Select temperature alarm function

If the upper and lower temperature thresholds are exceeded,temperature alarm substitution value will be tramsmitted.

Note：

If the measured temperature is 16 bits,it is not possible to enable the transmit alarm bit,and if the measured temperature is 15 bits,it is possible to enable the transmit alarm bit.

Actual temperature calculation formula:

$T[℃] = 0.02 * T_{send} - 273.15$

$T_{send}$is the temperature transmitted

9.3 Temperature measurement using internal temperature sensor

9.3.1 Internal temperature sensor configuration

The Si24R2H has an integrated 10bit digital temperature sensor,which can measure the internal temperature of the chip and can be connected to an external NTC resistor to measure

the external temperature of the chip.The internal temperature sensor is selected as the reference temperature for the temperature transmitter and temperature alarm functions,and the transmitter can transmit either its measured value or the associated alarm value,where the measured value can be selected with or without the alarm bit.

9.3.2 Transmit temperature value or alarm value

Operating procedure of transmitting chip internal temperature：

1. Select internal temperature sensor to measure temperature,type chooses the internal temperature
2. If the temperature emission function is selected,the emitted temperature can be observed

Transmission temperature value(10 bits)=Measured value+Temperature calibration value

A. Select the temperature emission function and select the emitted alarm bit

Transmit the temperature low byte first

Then transmit the temperature high byte{alarm bit 0/1,5'h0,transmit temperature value highest two bits}

(Alarm bits:1'b1 for exceeding temperature threshold range;1'b0 for within temperature threshold range)

B. Select the temperature transmit function and select the no transmit alarm bit

Transmit the temperature low byte first

Then transmit the temperature high byte{0,5'h0,highest two digits of emitted temperature value}

No alarm bit,the highest bit is 0

C. Select temperature alarm function

If the upper and lower temperature thresholds are exceeded,temperature alarm substitution value will be tramsmitted.

9.4 External NTC temperature measurement

9.4.1 NTC configuration

The Si24R2H can be externally connected to an NTC resistor to measure the external temperature of the chip.Choose to use the internal temperature sensor as the reference

temperature for the temperature transmitter function and the temperature alarm function,and choose the external NTC for the type,the transmitter can transmit its measured value or the related alarm value,where the measured value can be chosen with or without alarm bit.

Table 9-1 External signal connection via pad required for ntc measurement

Port	Port name	Port type	Functional description
1	NTC_VB	AO	Measurement of NTC reference voltage VREFP
2	NTC_VB_N	A	Measuring the NTC reference voltage VREFN
32	NTC_ADC	AI	NTC Capture Thermistor temperature signal(voltage)

9.4.2 Transmit temperature value or alarm value

Operating procedure：

1. Select internal temperature sensor for temperature measurement,external NTC for type selection
2. Configure options as needed
3. If you select the temperature emission function,you can observe the temperature of the emission

Transmission temperature value（10 bits）=ADC measurement value+Temperature calibration value

A. Select the temperature emission function and select the emitted alarm bit

Transmit the temperature low byte first

Then transmit the temperature high byte{alarm bit 0/1,5'h0,transmit temperature value highest two bits}

B. Select the temperature transmit function and select the no transmit alarm bit

Transmit the temperature low byte first

Then transmit the temperature high byte{0,5'h0,highest two digits of emitted temperature value}

No alarm bit,the highest bit is 0

C. Select temperature alarm function

If the upper and lower temperature thresholds are exceeded,temperature alarm substitution

value will be tramsmitted.

Note:Actual temperature calculation formula

The relationship between the NTC thermometry transmission temperature and the actual temperature is determined by the R-T curve of the NTC resistor

10 Electrical specification

10.1 Transmission part

10.1.1 Limitation parameter

Operating condition	Minimum	Maximum	Unit
Supply voltage			
VDD	-0.3	3.6	V
VSS		0	V
Input voltage			
VI	-0.3	5.25	V
Output voltage			
VO	VSS to VDD	VSS to VDD	V
Total power consumption			
		100	mW
Temperature			
Operating temperature	-40	+85	℃
Storage temperature	-40	+125	℃
ESD performance	HBM(Human Body Model):Class 1C		

10.1.2 Electrical specification

Condition：VDD=3V,VSS=0V TA=27℃,Crystal oscillator CL=12pF

Symbol	Parameter	Min	Typ	Max	Unit	Remark
OP parameters						
VDD	Supply voltage	2.1		3.6	V	ADC operation with voltage requires larger than 2.4V

I_{SHD}	Supply current in Shutdown mode		1		μA	
Isleep	Supply current in Sleep mode		1		μA	RCOSC,Watchdog ATR Timer still working
I_{STB}	Supply current in Standby mode		19		μA	
I_{IDLE}	Supply current in Idle-Tx mode		350		μA	
I_{TX}@14dBm	Current in TX mode@14dBm		48		mA	
I_{TX}@10dBm	Current in TX mode@10dBm		31		mA	
I_{TX}@4dBm	Current in TX mode@4dBm		20		mA	
I_{TX}@0dBm	Current in TX mode@0dBm		18		mA	
I_{TX}@-3dBm	Current in TX mode@-3dBm		14		mA	
RF parameters						
F_{OP}	RF frequency range	2400		2525	MHz	
F_{CH}	RF channel interval	1			MHz	At least 2MHz when 2Mpbs
ΔF_{MOD}(2Mbps)	Modulation frequency offset		±330		KHz	
ΔF_{MOD}(1M/250Kbps)	Modulation frequency offset		±175		KHz	
R_{GFSK}	Data rate	250		2000	Kbps	
TX parameters						
P_{RF}	RF output power	-3		14	dBm	
P_{BW}@2Mbps	Modulation bandwidth		2.1		MHz	
P_{BW}@1Mbps	Modulation bandwidth		1.1		MHz	

P_{BW}@250Kbps	Modulation bandwidth		0.9		MHz	
P_{RF1}	1st adjacent channel power 2MHz			-20	dBm	
P_{RF2}	2nd adjacent channel power 4MHz			-46	dBm	
Crystal oscillator parameter						
F_{XO}	Crystal frequency		16		MHz	
ΔF	Frequency offset		±20		ppm	
ESR	Equivalent loss resistance		100		Ω	

10.2 Receiving part

10.2.1 Limitation parameter

Exceeding one or more of the limit parameters listed in Table 10.2-1 may result in permanent damage to the device.

Table 10.2-1 125K limit parameter

Symbol	Description	Min	Max	Unit	Remark
VCC	Dc supply voltage	-0.5	3.6	V	
V_{IN}	Input pin voltage	-0.5	3.6	V	
I_{SOURCE}	Input current(latch immunity)	-100	100	mA	
ESD	Electrostatic discharge	±2		kV	HBM
P_t	Total power consumption(all inputs and outputs)		0.07	mW	
T_{strg}	Storage temperature	-65	150	℃	
T_{body}	Package temperature		260	℃	
RH_{NC}	Relative humidity(non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			

10.2.2 Operating condition

Table 10.2-2 125K operating condition

Symbol	Description	Min	Typ	Max	Unit
VCC	Supply voltage positive	2.4	3	3.6	V
VSS	Negative supply voltage	0		0	V
T_{AMB}	Environmental temperature	-40		85	℃

10.2.3 DC/AC parameter

Table 10.2-3 125K DC/AC parameter

Symbol	Description	Condition	Min	Typ	Max	Unit
CMOS input						
V_{IH}	High level input voltage		0.6VCC	0.7VCC	0.8VCC	V
V_{IL}	Low level input voltage		0.12VCC	0.2VCC	0.3VCC	V
I_{LAEK}	Input leakage current				100	nA
CMOS output						
V_{OH}	High level output voltage	1mA load	VCC-0.4			V
V_{OL}	Low level output voltage	1mA load			VSS+0.4	V
C_L	Capacitive load	1MHz clock			400	pF
Tri-state CMOS output						
V_{OH}	High level output voltage	1mA load	VCC-0.4			V
V_{OL}	Low level output voltage	1mA load			VSS+0.4	V
I_{OZ}	Tri-state leakage current	To VCC and VSS			100	nA

10.2.4 Electrical parameter

Table 10.2-4 125K electrical parameter

Symbol	Description	Condition	Min	Typ	Max	Unit
Input characteristics						
R_{IN}	Ac input impedance at 125khz	Antenna damper doesn't working (R1<4>=0）		2		MΩ
F1MAX	Band 1 maximum input frequency			150		kHz
F1MIN	Band 1 minimum input frequency			95		kHz
F2MAX	Band 2 maximum input frequency			95		kHz
F2MIN	Band 2 minimum input frequency			65		kHz
F3MAX	Band 3 maximum input frequency			65		kHz
F3MIN	Band 3 minimum input frequency			40		kHz
F4MAX	Band 4 maximum input frequency			40		kHz
F4MIN	Band 4 minimum input frequency			23		kHz
F5MAX	Band 5 maximum input frequency			23		kHz
F5MIN	Band 5 minimum input frequency			15		kHz
Current consumption						
I1CHRC	Current consumption when only one channel operates and the RC oscillator is used as a clock in the			4.6		uA

	standard listening mode					
I2CHRC	Current consumption when two channels operate and the RC oscillator is used as a clock in the standard listening mode			6.6		uA
I3CHRC	Current consumption when three channels operate and the RC oscillator is used as a clock in the standard listening mode			8.3		uA
I3CHSCRC	Current consumption when three channels operate and the RC oscillator is used as a clock in the scanning mode			4.5		uA
I3CHOORC	Current consumption when three channels operate and the RC oscillator is used as a clock in the ON/OFF mode	11% duty cycle		3.3		uA
		50% duty cycle		5.7		
I3CHXT	Current consumption when three channels operate and the crystal oscillator is used as a clock in the standard listening mode			7.9		uA
IDATA	Current Consumption in Preamble detection / Pattern correlation / Data receiving mode (RC-oscillator)	With 125 kHz carrier frequency and 1 kbps data-rate. No load on the output pins.		9.2		uA
IBOOST	Additional current			150		nA

	consumption per channel if gain boost enabled					
Input sensitivity						
SENS1	Input Sensitivity on all channels in the Band1	With 125 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
SENS1B	Input Sensitivity on all channels in the Band1 with 3dB gain boost	With 125 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		60		uVrms
SENS2	Input Sensitivity on all channels in the Band2	With 90 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
SENS2B	Input Sensitivity on all channels in the Band2 with 3dB gain boost	With 90 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		60		uVrms
SENS3	Input Sensitivity on all channels in the Band3	With 60 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single		80		uVrms

		preamble detection				
SENS3B	Input Sensitivity on all channels in the Band3 with 3dB gain boost	With 60 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		60		uVrms
SENS4B	Input Sensitivity on all channels in the Band4 with 3dB gain boost	With 30 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		60		uVrms
SENS5B	Input Sensitivity on all channels in the Band5 with 3dB gain boost	With 18 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		60		uVrms
Channel setup time						
TSAMP	Amplifier setup time			250		us
Crystal oscillator						
FXTAL	Frequency	Crystal dependent	25	32.768	45	kHz
TXTAL	Start-up time				1	s
IXTAL	Current consumption			300		nA
External clock source						
IEXTCL	Current consumption			0.8		uA
FEXTCL	Frequency		25		45	kHz
RC oscillator						
FRCNCAL	Frequency	If no calibration is performed	25	32.768	45	kHz
FRCCAL32		If calibration with	31	32.768	34.5	

		32.768 kHz reference signal is performed				
FRCCALMAX		Maximum achievable frequency after calibration		45		
FRCCALMIN		Minimum achievable frequency after calibration		23.75		
TRC	Start-up time	From RC enable (R1<1> = 0)			1	s
TCALRC	Calibration time		65			Periods of reference clock
IRC	Current consumption			650		nA
LC oscillator						
$FLCO_{MIN}$	Minimum frequency	L=47mH，C=2.3nF		15		kHz
$FLCO_{MAX}$	Maximum frequency	L=7.2mH，C=150pF		150		kHz
$RPAR_{MIN}$	Minimum eq. Parallel			10		kΩ
Tuning capacitance						
LF1Ptuning	Capacitance	Maximum internal capacitance (in step of 1pF) on LF1P		31		pF
LF2Ptuning		Maximum internal capacitance (in step of 1pF) on LF2P		31		pF
LF3Ptuning		Maximum internal capacitance (in step of 1pF) on LF3P		31		pF

11 Package

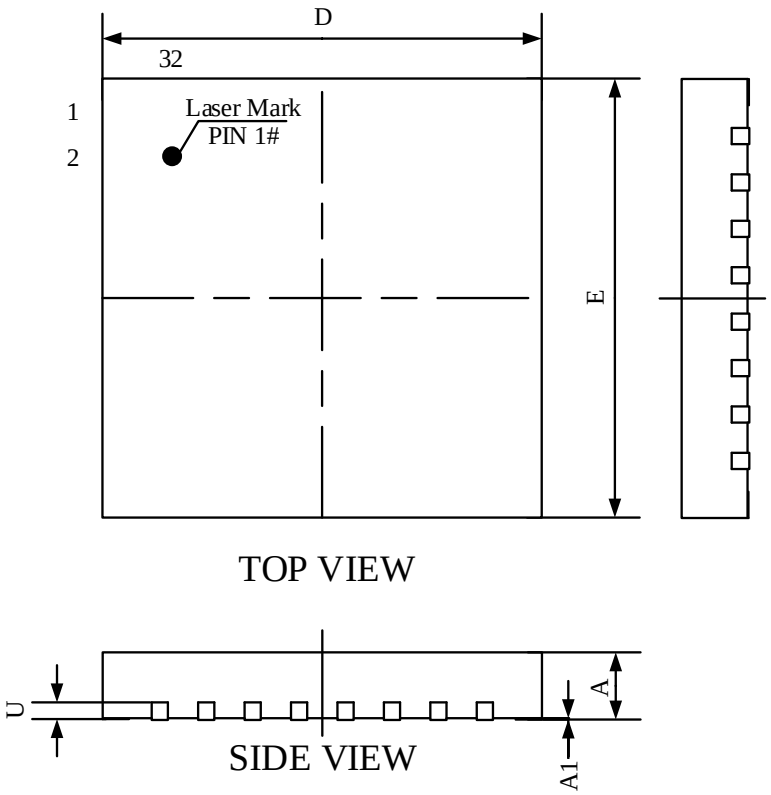


Figure 11-1 Package(QFN32L)

Table 11-1 Package size

SYMBOL	MILLIMETER(mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.2	0.05
b	0.155	0.18	0.205
D	3.9	4	4.1
D2	2.55	2.65	2.75
f	0.375	0.4	0.425
e	0.4BSC		
Nd	2.8BSC		
Ne	2.8BSC		
E	3.9	4	4.1
E2	2.55	2.65	2.75

12 Application schematic

12.1 Application schematic

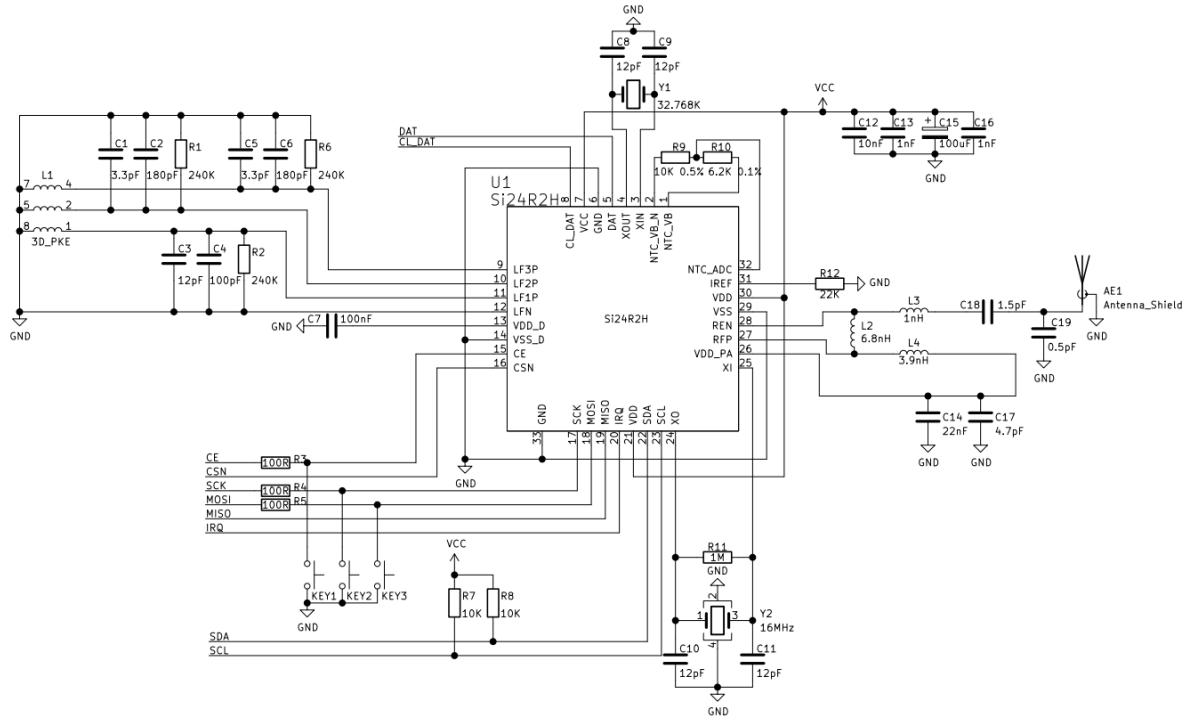


Figure 12.1-1 Multi-function application schematic

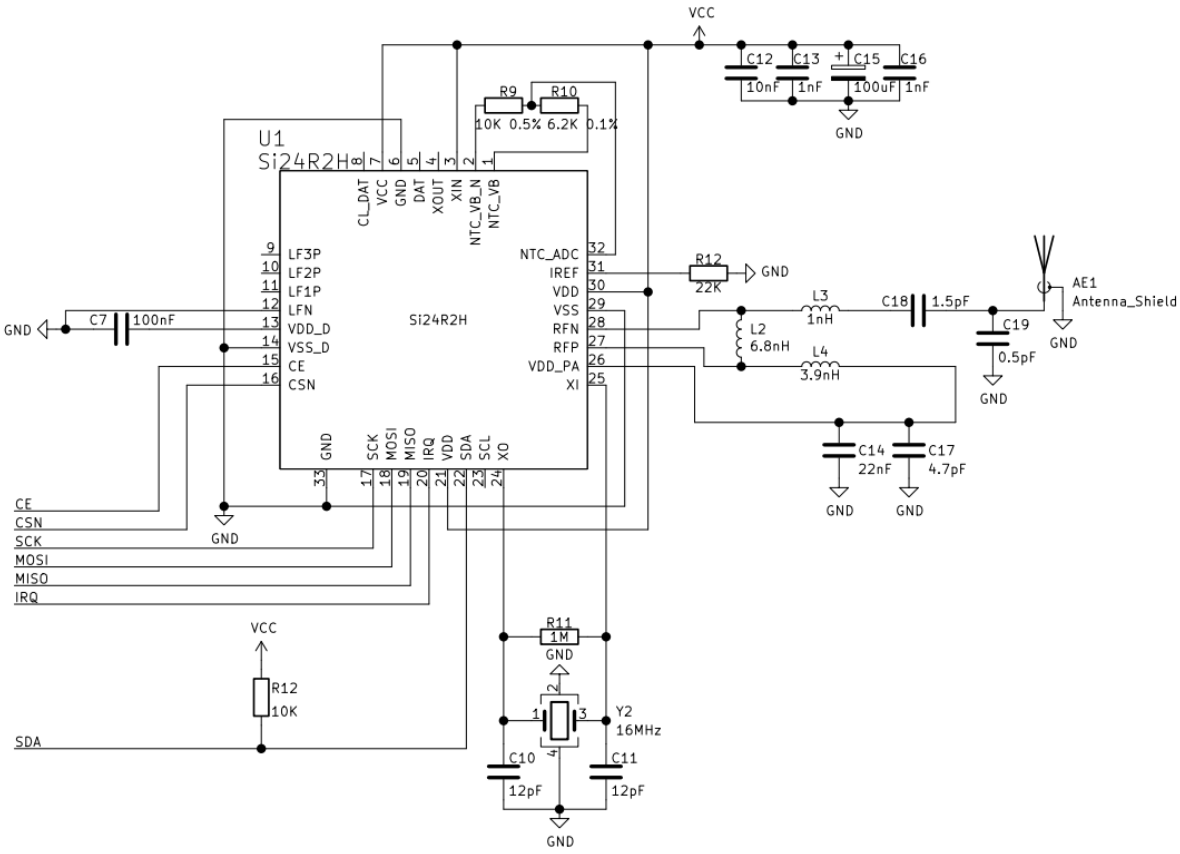


Figure 12.1-2 NTC temperature measurement 2.4G(BLE)transmission application schematic

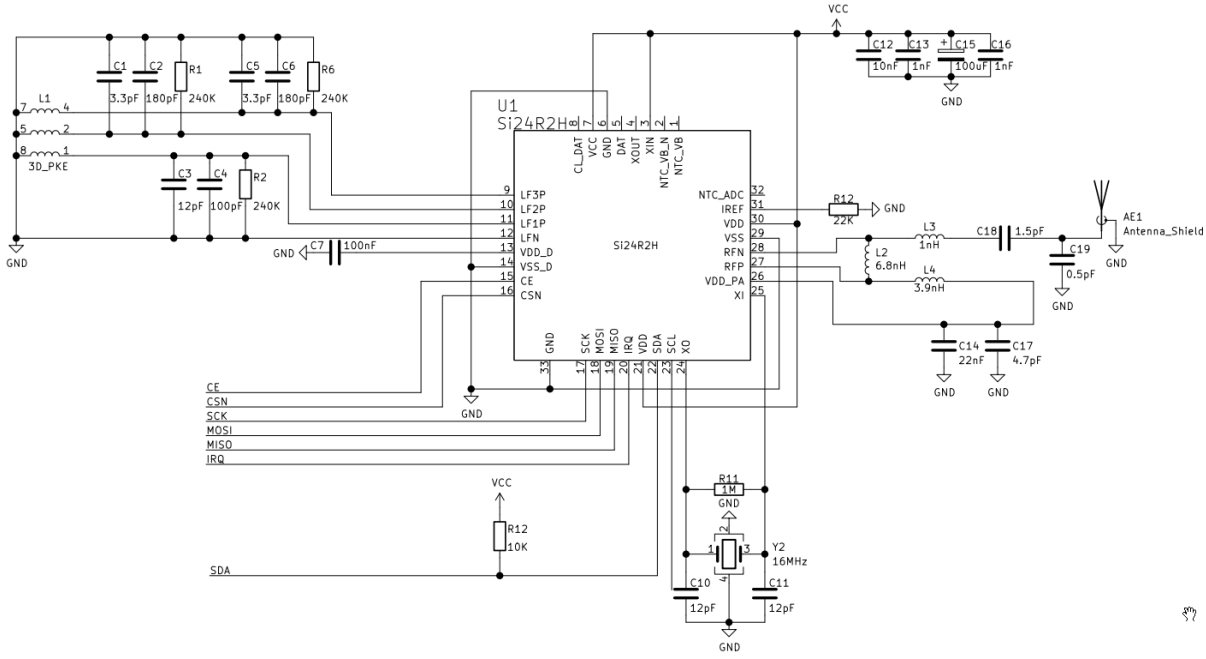


Figure 12.1-3 2.4G+125K application schematic

Note：

1. Grounding is required at the bottom of the chip.
2. SDA pin also requires a pull-up resistor to the power supply when an external temperature sensor is not used.
3. Important update: update the 2.4G partial RF matching circuit, modify the inductance value of L4 from 1nH to 3.9nH and the capacitance value of C14 from 10nF to 22nF. The modification reason is optimize the frequency deviation and optimize interference of the 125KHz signal to the 2.4GHz signal.
4. Modify the capacitance value of C7 from 2.2uF to 100nF.

Table 12-1 Component BOM table

Name	Value	Package	Description
C8,C9（optional）	12pF	0402	NPO，±2%
C10,C11	12pF	0402	NPO，±2%
C12	10nF	0402	X7R，±10%
C13,C16	1nF	0402	X7R，±10%
C15[a]	100uF	1210	±20%
C2,C4（optional）	150pF	0603	NPO，±5%
C1,C3（optional）	18pF	0603	NPO，±5%
C5（optional）	3pF	0603	C0G，±0.25pF
C6（optional）	180pF	0603	NPO，±5%
C18	1.5pF	0402	NPO，±0.1pF
C19	0.5pF	0402	NPO，±0.1pF
C7	100nF	0402	X7R，±10%
C14	22nF	0402	X7R，±10%
C17	4.7pF	0402	C0G，±0.25pF
L1（optional）	L(3D)	3D_PKE	125KHz antenna
L2	6.8nH	0402	Chip inductor，±5%
L3	1nH	0402	Chip inductor，±5%
L4	3.9nH	0402	Chip inductor，±5%
R1,R2,R6（optional）	240K	0603	±5%
R10（optional）	6.2K	0603	±0.1%

R9-NTC[b]（optional）	10K	0603	±1%(±0.5%)
R12	22K	0402	±1%
R11（optional）	1M	0402	±10%
U1	Si24R2H	QFN32 4x4	
Y1[c]（optional）	32.768KHz	3215	±20ppm,CL=12pF
Y2	16MHz	3225	±20ppm,CL=9Pf~15pF

a. Capacitor leakage for low power applications must be as small as possible.

b. NTC accuracy±0.5%or±1%for general temperature measurements and±0.1%for body temperature measurements.

c. Y1 32.768KHZ crystal is optional,without this crystal does not affect the reception performance.

12.2 PCB layout

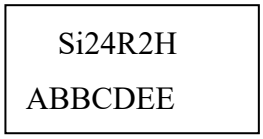
This section is the notes for PCB layout of the typical application schematic above.A double-sided FR-4 board is used.There is a copper clad surface on the top and bottom layers respectively,the copper clad surfaces of the top and bottom layers are connected by a large number of vias,and there is no copper clad surface under the antenna.The bottom layer of PCB is the ground plane.To ensure better RF performance,die exposed at the bottom of the IC is recommended to connect to PCB ground plane.It is strongly recommended to keep it connected.The RF matching component pads are at least 0.5mm from the surrounding ground.

13 Revision history

Version	Modified date	Modified content
V1.0	2023/11/24	First draft
V1.1	2024/2/29	Update application schematic and the Component BOM table: update the 2.4G partial RF matching circuit, modify the inductance value of L4 from 1nH to 3.9nH and the capacitance value of C14 from 10nF to 22nF. The modification reason is optimize the frequency deviation and optimize interference of the 125KHz signal to the 2.4GHz signal.
V1.2	2024/05/09	Update application schematic and modify the capacitance value of C7 from 2.2uF to 100nF.

14 Order information

Package marking



Si24R2H:chip code

A:package date code,5 represents year 2020

BB:week of sending out processing,42 represents in the year A the 42th week

C:package factory code,A、HT、NJ or WA,can also abbreviated as A、H、N or W

D:test factory code,A、Z or H

EE:production batch code

Table 14-1 Order information

Order code	Package	Container	Min unit
Si24R2H-Sample	4×4mm 32-pin QFN	Box/Tube	5
Si24R2H	4×4mm 32-pin QFN	Tape and reel	4K

15 Technical Support and Contact Information

Nanjing Zhongke Microelectronic Industry Technology Research Institute Co.,Ltd
Technical Support Center
Phone:025-68517780
Address:Room 201,Building B,Research Zone 3,Xuzhuang Software Park,Xuanwu District,Nanjing, Jiangsu,China
Website:http://www.csm-ic.com

Sales and Marketing
Phone:13645157034,13645157035
Email:sales@csmic.ac.cn

Technical Support
Phone:13645157034
Email:supports@csmic.ac.cn