

FURUNO GNSS Receiver

GT-100

Hardware Specifications

(Document No. SE22-410-003-07)



FURUNO ELECTRIC CO., LTD.

www.furuno.com

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Revision History

Version	Changed contents	Date
0	Initial release	2022.06.22
1	Change the figure in section 4.1 Correct items in Table 4.2 Add items in Table 5.1 Add items in Table 5.2 Add section 5.4 Change the contents in section 5.5 Add items in Table 5.6.2 Change the figures in section 7.1 Add a note in section 7.1 Correct the weight in section 7.2 Add the storage conditions in section 8.3 Change the figure in section 8.4 Change the figure in section 8.5 Change the figure in section 8.6 Add the marking specifications in chapter 9	2022.12.19
2	IMPORTANT NOTICE Change the figure in section 3 Change the contents in Table 4.2 Change the contents in Table 5.6.1 Change the contents in Table 5.6.2	2023.05.12
3	Add items in Table 5.2 Change the contents in section 5.6.2	2023.07.13
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5	Correct chapter 9	2024.03.18
6	Add section 5.6 Change a note in section 7.1	2024.06.20
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1 Outline

This document contains the specification pertinent to the GNSS module.

2 Features

2.1 Product Overview

GT-100 is Dual band, multi constellation GNSS receivers.

- ◆ GT-100 support L1 Band and L5 Band.
- ◆ GT-100 support GPS, GLONASS, BeiDou, Galileo, NavIC, SBAS and QZSS as multi constellation.

GT-100 output accurate time information.

- ◆ GT-100 support PPS (Pulse per Second) output synchronized with UTC time or GPS time and frequency output that can be set arbitrarily.

The products support the debug feature for GNSS application.

- ◆ Internal Antenna Diagnostic function.

The products include an embedded NVM for firmware updates.

- ◆ Size: 16Mbit
- ◆ Memory Structure: STT-MRAM

The products have an UART interface. And the following message format is supported.

- ◆ NMEA Message

Table 2.1 General Specifications¹⁾

Items	Description	Notes
GNSS reception capability	GPS L1C/A	L1
	GLONASS L1OF	L1
	Galileo E1	L1
	Beidou B1I	L1
	Beidou B1C	L1
	QZSS L1C/A	L1
	SBAS L1	L1
	NavIC L5	L5
	GPS L5	L5
	Galileo E5a	L5
	Beidou B2a	L5
	QZSS L5	L5
	Anti-Jamming	● -
	Anti-Spoofing	● -
Environment Robustness	Multipath mitigation	● -
	T-RAIM	● -
	Antenna current detection	● -
	Serial data format	NMEA ²⁾ ● Default 115200bps
Antenna	Active antenna	●
	Passive antenna	● External LNA required.
Operational limits	Altitude	18,300m
	Velocity	515 m/s

Notes:

1) See the function specifications for details.

2) See the protocol specifications for details.

3 Functional Overview

The internal key device for GT-100 is *eRide*OPUS 9. The latest Furuno monolithic GNSS receiver chip with an ARM-Cortex processor (for signal tracking and processing), PLL synthesizer, Down-converter, ADC, DSP and STT-MRAM (for firmware and data storage).

GT-100 also include a TCXO (for reference clock), RTC (for real-time clock) 32 kHz crystal, SAW filter, and antenna current detection circuit. The block diagram is shown in Figure 3.1.

GT-100 have a built-in function (FGEN) for generating high-precision clock pulses in the GNSS receiver chip. GT-100 output a PPS signal or a clock pulse of any frequency from its OCLK0, OCLK1 and OCLK2. The GT-100 have an input pin, ICLK, to allow time synchronization with an external PPS or clock. Refer to the function specifications and protocol specifications for usage.

RF_IN is the signal line on which the GNSS signal input and the bias voltage for antenna power supply are superimposed. By applying a voltage to VCC_ANT, the bias voltage is superimposed on RF_IN. The antenna current detection circuit detects whether the current flowing from VCC_ANT to RF_IN is insufficient or excessive. This status can be known by serial communication.

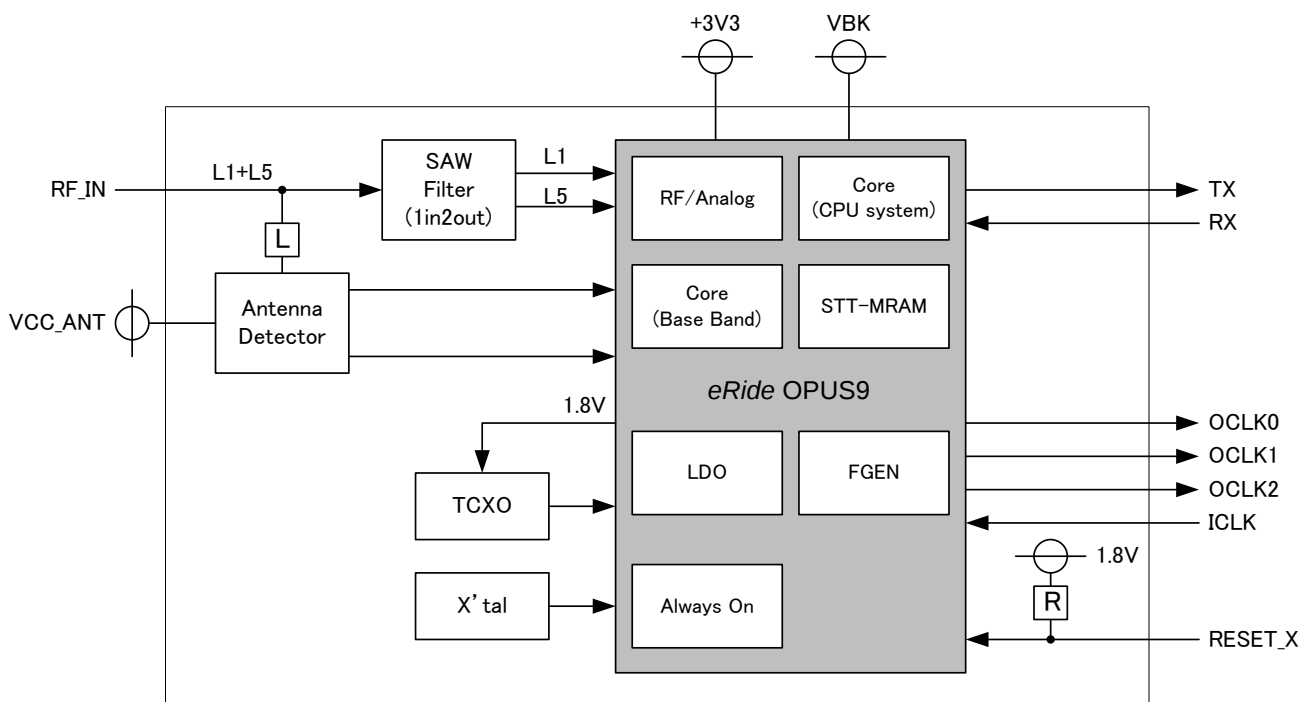
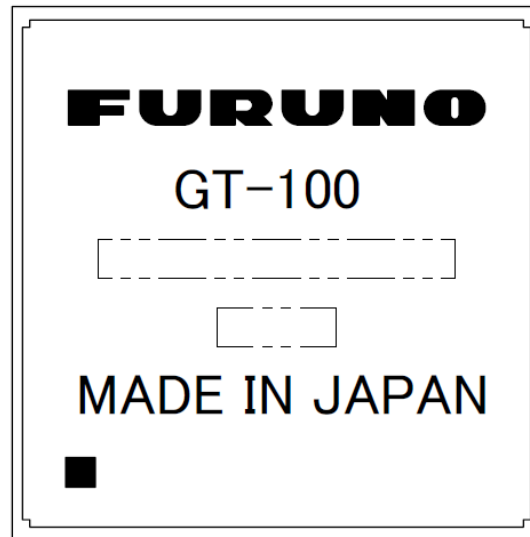


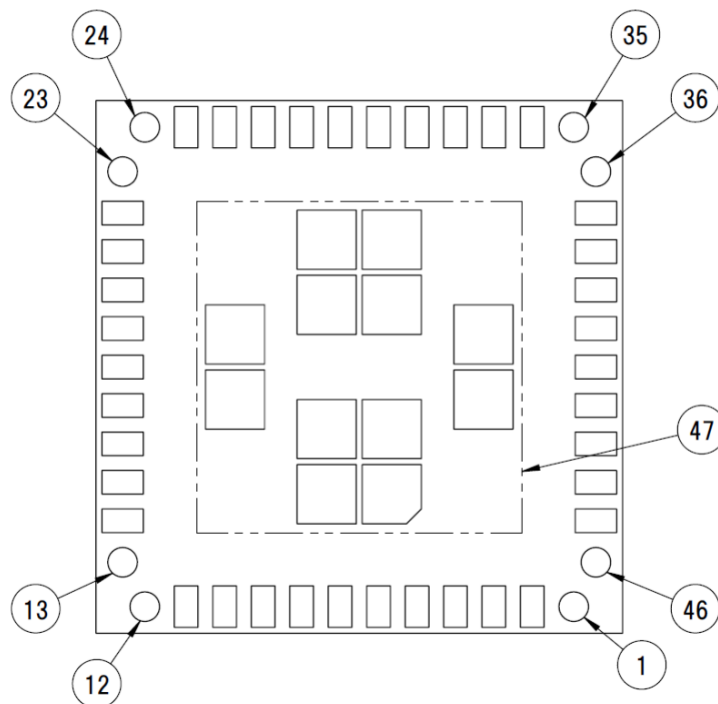
Figure 3.1 Block Diagram

4 I/O Signal Description

4.1 Pin Layout



TOP View



BOTTOM View

Note: GND pads of the center are put together as Pin No.47.

4.2 GT-100 Signal Description

Table 4.2 I/O Signal Description

#	GT-100 Pin Name	I/O	I/O Voltage	Built-in PU/PD ¹⁾	Reset State	Unused	Description
1	NC	-	-	-	-	OPEN	-
2	GND	-	-	-	-	-	-
3	RESERVE	-	-	-	-	OPEN	Don't connect to GND.
4	RESERVE	-	-	-	-	OPEN	-
5	RESERVE	-	-	-	-	OPEN	-
6	GND	-	-	-	-	-	-
7	GND	-	-	-	-	-	-
8	GND	-	-	-	-	-	-
9	GND	-	-	-	-	-	-
10	RF_IN	INPUT	-	-	-	OPEN	L1 & L5 band RF signal input pin
11	GND	-	-	-	-	-	-
12	NC	-	-	-	-	OPEN	-
13	NC	-	-	-	-	OPEN	-
14	VCC_ANT	Power Input	-	-	-	OPEN	Antenna Detector power supply / Antenna power supply input pin
15	GPIO2	OUTPUT ²⁾	3.3V	-	Hi-Z	OPEN	Refer to Protocol Specifications
16	OCLK1	OUTPUT	3.3V	-	Hi-Z	OPEN	PPS/clock output pin
17	GND	-	-	-	-	-	-
18	NC	-	-	-	-	OPEN	Don't connect to GND.
19	GND	-	-	-	-	-	-
20	VBK	Power Input	-	-	-	OPEN	Backup power supply input pin
21	GND	-	-	-	-	-	-
22	GND	-	-	-	-	-	-
23	NC	-	-	-	-	OPEN	-
24	NC	-	-	-	-	OPEN	-
25	GND	-	-	-	-	-	-
26	GND	-	-	-	-	-	-
27	RESERVE	-	-	-	Hi-Z	OPEN	-
28	RESERVE	-	-	-	Hi-Z	OPEN	-
29	RX	INPUT	3.3V	PU	Hi-Z	OPEN or PU	UART reception input pin
30	TX	OUTPUT	3.3V	-	Hi-Z	OPEN	UART transmission output pin
31	GND	-	-	-	-	-	-
32	ICLK	INPUT	3.3V	PD	Hi-Z	GND or PD	PPS/clock input pin
33	OCLK2	OUTPUT	3.3V	-	Hi-Z	OPEN	PPS/clock output pin
34	GND	-	-	-	-	-	-
35	NC	-	-	-	-	OPEN	-
36	NC	-	-	-	-	OPEN	-
37	GND	-	-	-	-	-	-
38	OCLK0	OUTPUT	3.3V	-	Hi-Z	OPEN	PPS/clock output pin
39	GPIO0	OUTPUT ²⁾	3.3V	-	Hi-Z	OPEN	Refer to Protocol Specifications
40	GPIO1	OUTPUT ²⁾	3.3V	-	Hi-Z	OPEN	Refer to Protocol Specifications
41	RESERVE	-	-	-	-	OPEN	-
42	GND	-	-	-	-	-	-
43	VCC	Power Input	-	-	-	-	Main power supply input pin External reset signal input pin
44	Reset_X	INPUT	1.8V	PU	-	OPEN or PU	Logic L: Reset Logic H: Normal operation
45	GND	-	-	-	-	-	-
46	NC	-	-	-	-	OPEN	-
47	GND	-	-	-	-	-	-

Notes:

1) Pull-up and pull-down resistor values are shown in Table 5.3.

2) Hi-Z when command is not set.

5 Electrical Characteristics

5.1 Absolute Maximum Rating

The lists of absolute maximum ratings are specified over operating case temperature shown in Table 6.1. Stresses beyond those listed under those ranges may cause permanent damage to the module.

Table 5.1 Absolute Maximum Rating

Items	Symbol	Min.	Max.	Unit	Notes
Supply voltage to VCC	V _{CC_ABS}	-0.3	4.0	V	-
Supply voltage to VBK	V _{BK_ABS}	-0.3	2.5	V	-
Supply voltage to VCC_ANT	V _{ANT_ABS}	-	7.0	V	-
Digital input (DI) voltage	-	-0.3	3.7	V	-
Digital input (DI) voltage	-	-0.3	2.2	V	Apply to Reset_X pin.
RF_IN input power	P _{RF_ABS}	-	0	dBm	-
Magnetic field strength	T _{MFS_ABS}	-	1000	mT	-

5.2 Power Supply

Table 5.2 Power Supply Characteristics

T_A=25°C, unless otherwise stated

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage to VCC	V _{CC0}	3.0	3.3	3.60	V	-
Supply voltage to VBK	V _{BK}	1.40	1.80	1.98	V	-
Supply voltage to VCC_ANT	V _{ANT}	3.0		5.0	V	-
VCC rising slew rate	V _{CC_RS}	0.2	-	20	ms	Figure 5.4.1
VCC current consumption	I _{CCAL}	-	55	200	mA	Full search @T _A =85°C
	I _{CCTL}	-	50	-	mA	Tracking satellite outdoor @T _A =85°C
VBK current consumption at back up	I _{BKN}	-	40	-	μA	V _{CC} =0V
		-	-	1.5	mA	V _{CC} =0V @T _A =85°C
VBK current consumption at normal operation)	I _{BKB}	-	-	0.1	μA	V _{CC} =3.3V
VCC_ANT current consumption	I _{CC_ANT}	-	13	21	mA	The current of the active antenna is not included.

5.3 Digital Interface Signal

Table 5.3 Interface Signal

$T_A=25^{\circ}\text{C}$, unless otherwise stated

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Logic L input voltage for 3.3V power domain Inputs	V_{IL}	0	-	$0.3 \times V_{CC}$	V	-
Logic H input voltage for 3.3V power domain Inputs	V_{IH}	$0.7 \times V_{CC}$	-	V_{CC}	V	-
Logic L input voltage for 1.8V power domain Input (Reset_X)	V_{IL_RST}	0	-	0.5	V	Apply to Reset_X pin
Logic H input voltage for 1.8V power domain Input (Reset_X)	V_{IH_RST}	1.36	1.8	-	V	Apply to Reset_X pin
Logic L output voltage	V_{OL}	0	-	$0.2 \times V_{CC}$	V	@ $ I_{OL} = 2\text{mA}$
Logic H output voltage	V_{OH}	$0.8 \times V_{CC}$	-	V_{CC}	V	@ $ I_{OH} = 2\text{mA}$
Pull-up resistor for 3.3V power domain I/O	R_{PU}	33	-	330	$k\Omega$	-
Pull-up resistor for 1.8V power domain Input (Reset_X)	R_{PU_RST}	-	10	-	$k\Omega$	Apply to Reset_X pin
Pull-down resistor	R_{PD}	33	-	330	$k\Omega$	-

5.4 Operation Sequence

5.4.1 Rise Time for Power Supply

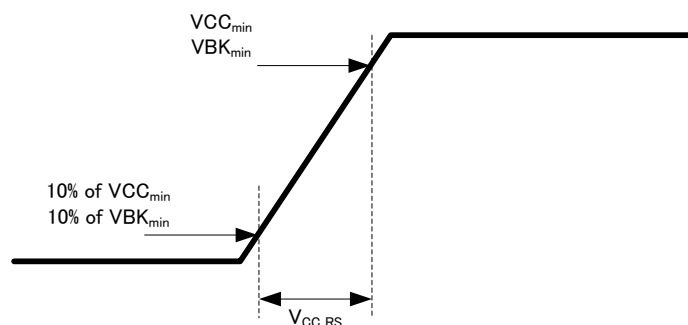


Figure 5.4.1 Rise Time for Power Supply Sequence

5.4.2 Power-up / Power-down timing of VBK and VCC

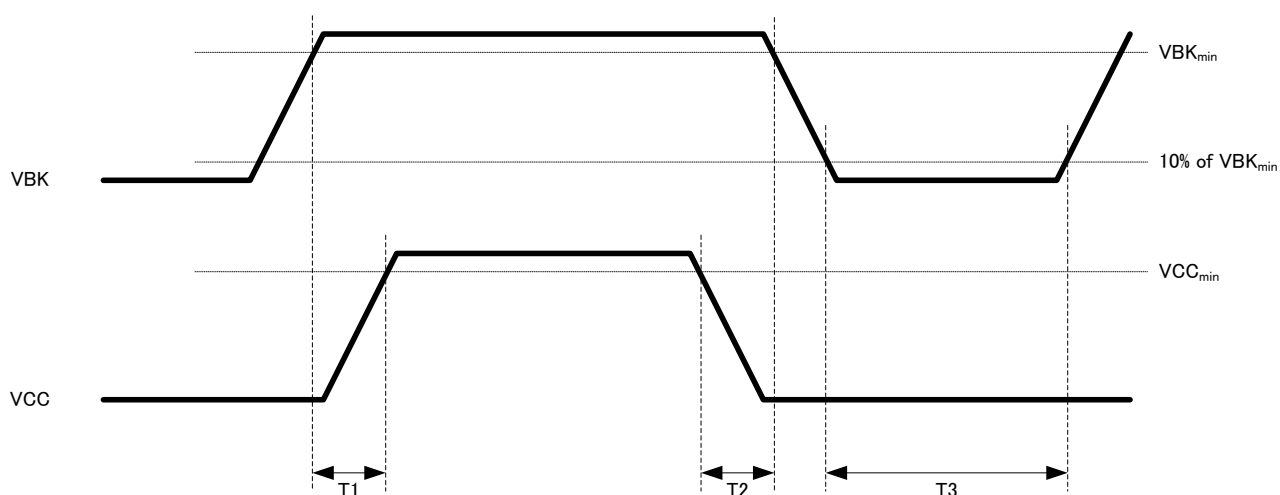


Figure 5.4.2 Power-up / Power-down timing of VBK and VCC Sequence

Table 5.4.2 Power-up / Power-down timing of VBK and VCC Sequence

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
VBK rise to VCC rise time	T1	0	-	-	ms	The VBK should rise at earlier than or VCC rising.
VCC fall to VBK fall time	T2	0	-	-	ms	The VCC should fall earlier than or same timing as the VBK falling.
Minimum VBK inactive time	T3	500	-	-	ms	The VBK should be kept low more than 500ms.

5.5 Reset

5.5.1 External Reset

In most cases, it is not required to drive external reset input (Reset_X) pin. However, if it is needed to force the reset state externally for e.g. synchronizing the reset state with the application circuitry, Reset_X can be used for this purpose. The H voltage level of the Reset_X signal should be 1.8V. The Reset_X has an internal pull-up. (Pull-up resistor is 10kΩ.) An open-drain or open-collectors is recommended to prevent collisions with internal pull-up voltages.

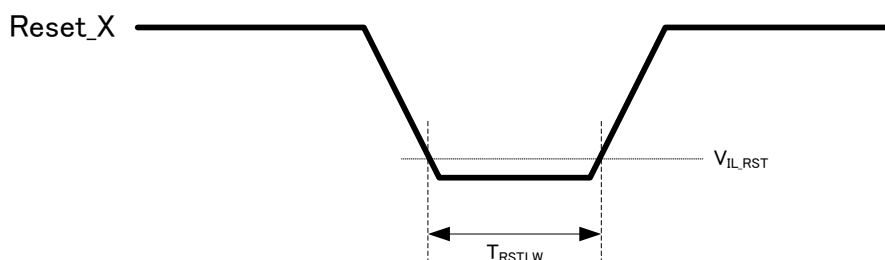


Figure 5.5.1 Reset Sequence

Table 5.5.1 Reset Sequence

Items	Symbol	Min.	Max.	Unit	Notes
Minimum reset activate time	T_{RSTLW}	500	-	ms	The Reset_X should be kept low more than 500ms.

5.5.2 UART Wake-up Timing after Reset

5.5.2.1 Without External Reset

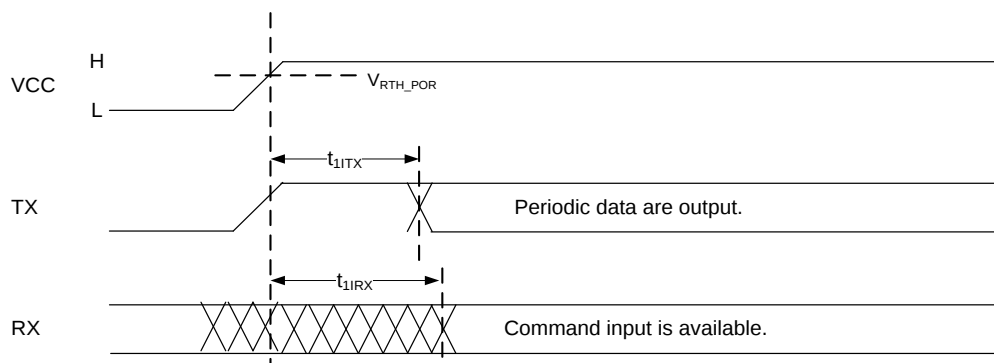


Figure 5.5.2.1 UART Wake-up Timing after V_{RTH_POR}

Table 5.4.2.1 UART Wake-up Timing after V_{RTH_POR}

Items	Symbol	Min.	Max.	Unit	Notes
Time delay from VCC reaches V_{RTH_POR} to TX valid	t_{1ITX}	-	6	s	
Time delay from VCC reaches V_{RTH_POR} to RX ready	t_{1IRX}	-	6	s	

5.5.2.2 With External Reset

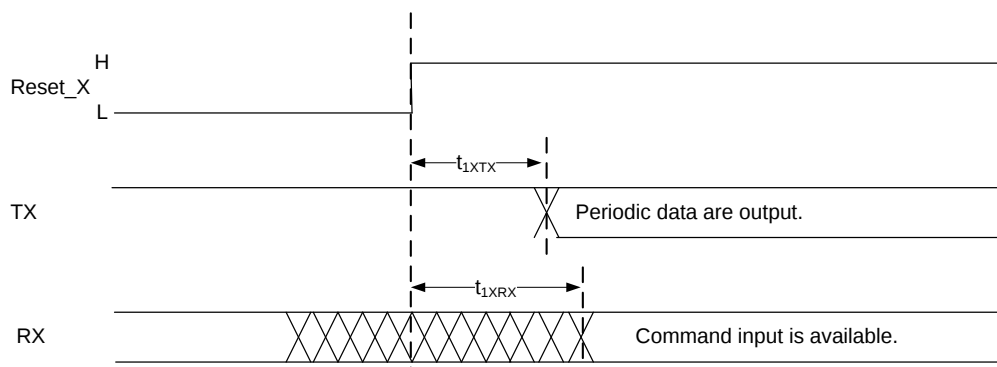
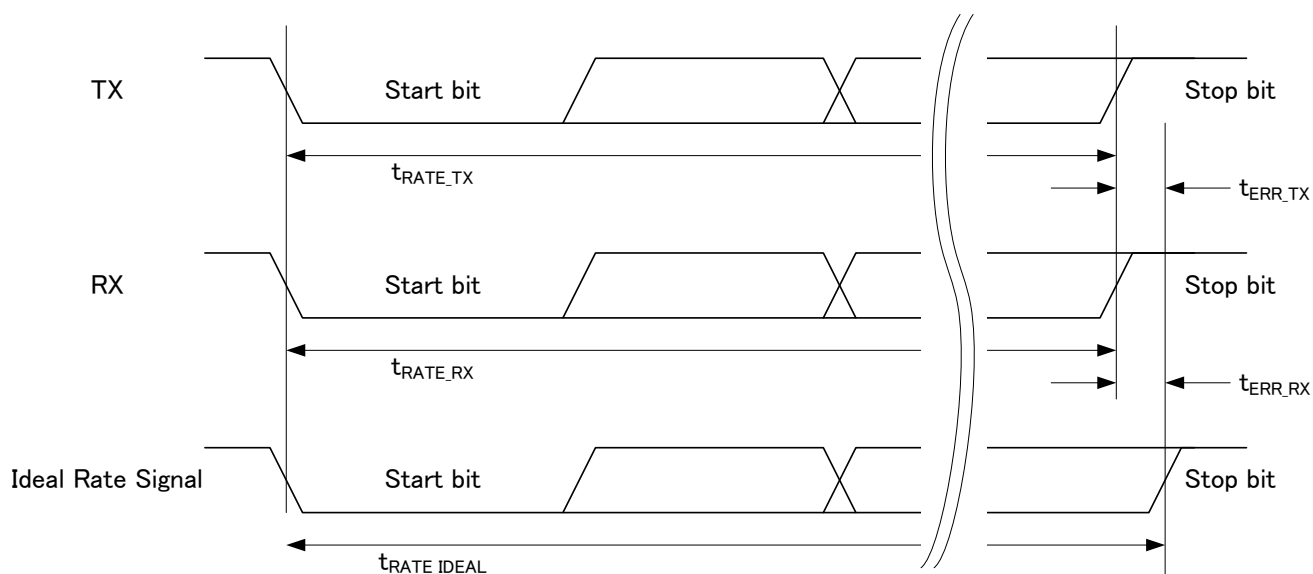


Figure 5.1.2.2 UART Wake-up Timing after Reset_X

Table 5.5.2.2 UART Wake-up Timing after Reset_X

Items	Symbol	Min.	Max.	Unit	Notes
Time delay from Reset_X set to H to TX valid	t_{1XTX}	-	6	s	
Time delay from Reset_X set to H to RX ready	t_{1XRX}	-	6	s	

5.6 UART



Items	Symbol	Min.	Max.	Unit	Notes
Baud Rate	R_{BRT_RATE}	9600	460800	bps	
UART Error Rate	R_{BRT_ERR}	-2	2	%	$t_{ERR_TX} / t_{RATE_IDEAL}$ $t_{ERR_RX} / t_{RATE_IDEAL}$

5.7 Antenna

5.7.1 Recommended Antenna

Table 5.6.1 Recommended Active Antenna

Item	Min.	Typ.	Max.	Unit	Remarks
L1 Bandwidth	1559	-	1606	MHz	
L5 Bandwidth	1166	-	1187	MHz	
Antenna element gain	0	-	-	dBi	
Amplifier gain	15	-	40	dB	Including cable loss. 15 dB to 25 dB is recommended for noise robustness
Amplifier NF	-	-	3	dB	Including cable loss
Impedance	-	50	-	Ω	

5.7.2 Antenna Amplifier Power

Power for antenna pre-amplifier input on pin #14 (VCC_ANT) is superimposed (biased) on pin #10 (RF_IN).

GT-100 have the function of supplying voltage to the active antenna and diagnosing the connection state (open, short) of the antenna. The diagnostic results are output by the proprietary NMEA message. In addition, it also has a protection function (OFF Mode) when the antenna is shorted. When the antenna output voltage is 0.5V(TYP) or less, it enters OFF Mode. To return to Normal Mode from OFF Mode, please solve the short-circuit problem first. After that, it will work as Normal Mode when the antenna output voltage is 1.0V(TYP) or higher. The diagnostic result is SHORT during OFF Mode.

Table 5.6.2 Recommended Antenna Power

$T_A=25^{\circ}\text{C}$, VCC_ANT=5V unless otherwise stated

Items	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_{APO}	$V_{ANT}-0.5$	-	-	V	@ $I_{APO}=50\text{mA}$
Output current	I_{APO}	-	-	55	mA	-
Open Detect Threshold Current	I_{AOD}	-	1.3	2.5	mA	-
Short Detect Threshold Current	I_{ASD}	60	82	-	mA	-
Short Protection	I_{ASP}	68	-	130	mA	-
Load Capacity	C_{ALC}	-	-	50	μF	

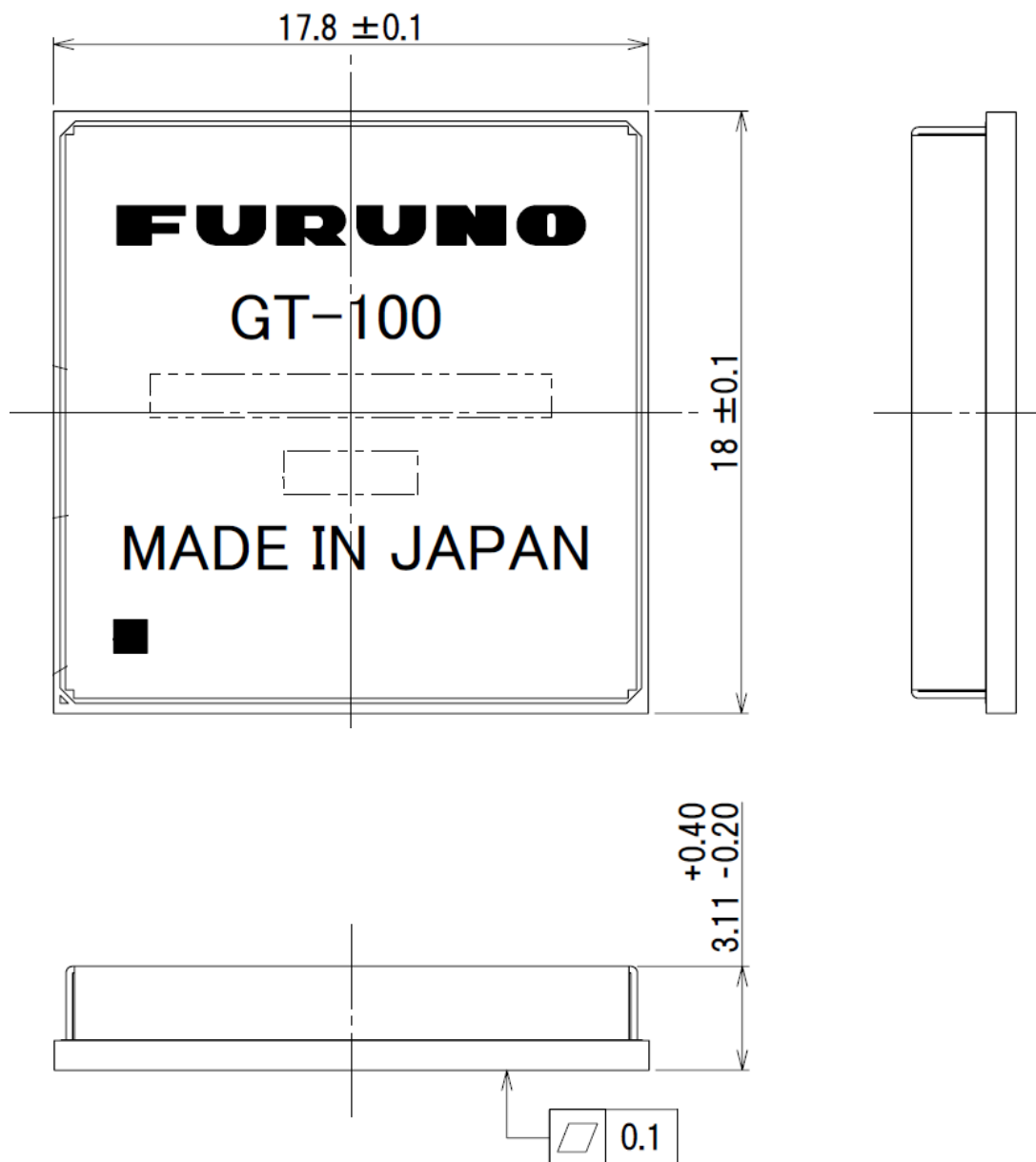
6 Environmental Specifications

Table 6.1 Environmental Specifications

Items	Specification	Unit	Notes
Operating temperature	-40 to +85	$^{\circ}\text{C}$	-
Storage temperature	-40 to +105	$^{\circ}\text{C}$	-
Magnetic field immunity	10-year data retention	Max 100	mT @25 $^{\circ}\text{C}$
		Max 90	mT @55 $^{\circ}\text{C}$
		Max 55	mT @85 $^{\circ}\text{C}$
	Active Read / Write	Max 25	mT -

7 Mechanical Specifications

7.1 Mechanical Description



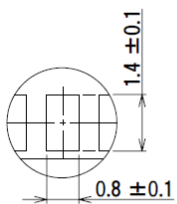
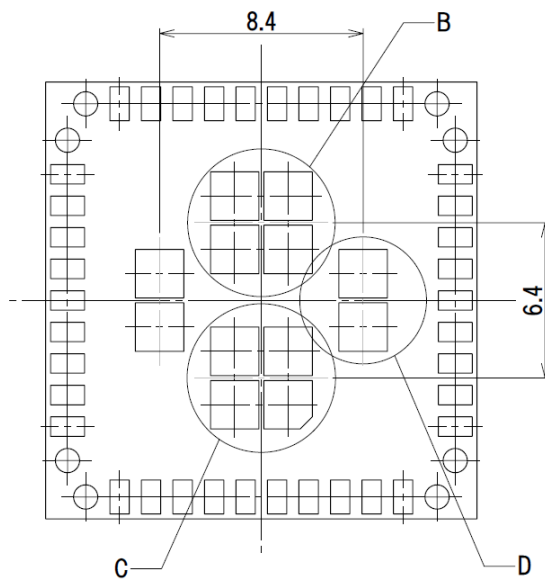
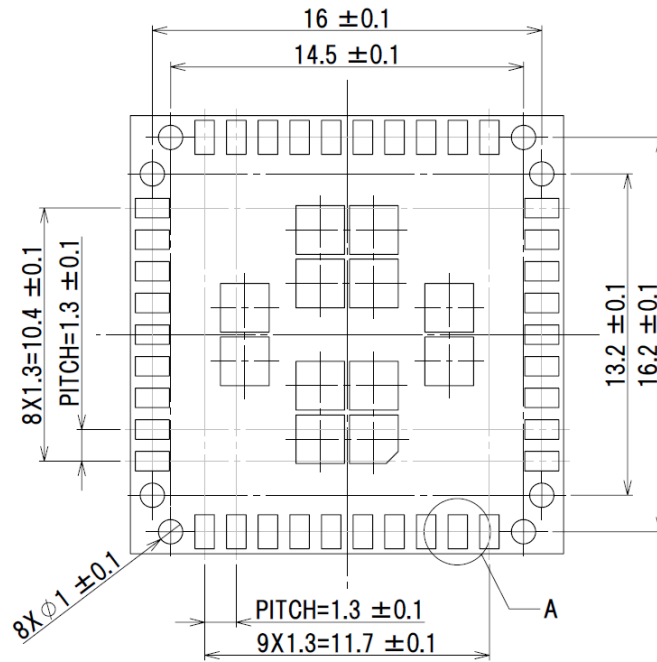
units: [mm]

Note: Tolerances are ± 0.3 mm, unless otherwise specified.

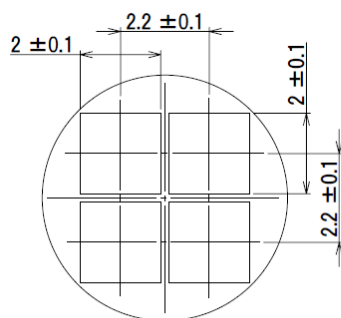
Dimensions in (): It is reference dimension.

The terminal coplanarity of product assumes the state of room temperature.

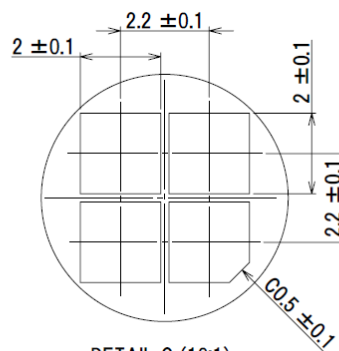
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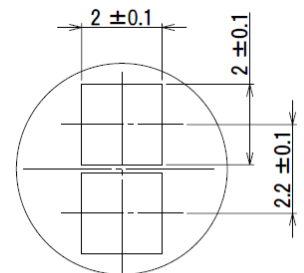
DETAIL A (10:1)
 (38 parts)



DETAIL B (10:1)



DETAIL C (10:1)



DETAIL D (10:1)
 (2 parts)

Note: Tolerances are $\pm 0.3\text{mm}$, unless otherwise specified.
Dimensions in (): It is reference dimension.
The terminal coplanarity of product assumes the state of room temperature.
Surface treatment specifications for module bottom terminal.
Material : Cu
Surface finish : Ni-Au
Ni $3\mu\text{m}$ - $8\mu\text{m}$
Au $0.05\mu\text{m}$ – $0.15\mu\text{m}$

7.2 Weight

1.7g (TYP)

8 MECHANICAL DESIGN INFORMATION

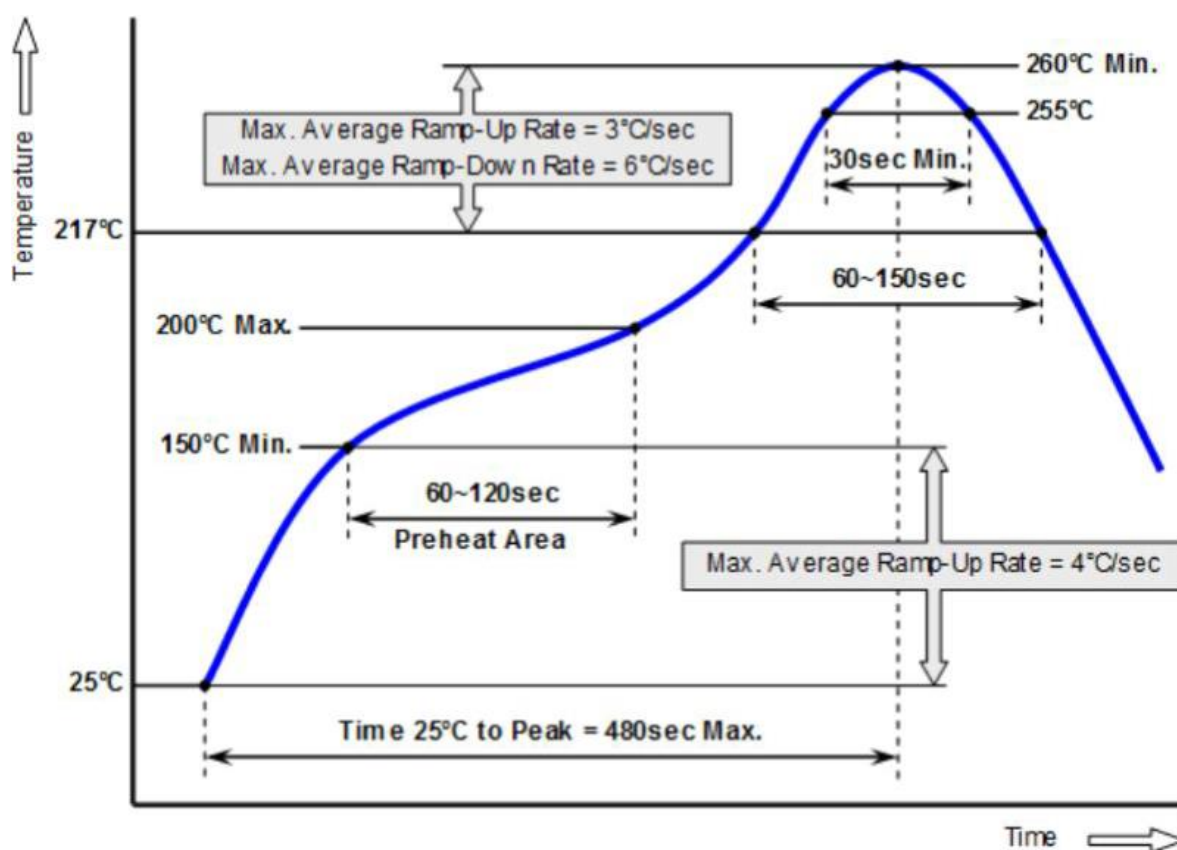
Recommended Copper Land and Solder Stop Mask (Resist) on Customer's Mother Board and Solder Print Mask (Metal Mask) Dimensions for better soldering with GT-100. The following drawings have been verified based on FURUNO recommended reflow soldering conditions and reference PCB. The reflow solderability should vary in accordance to the thickness of the PCB, reflow condition and pattern layout etc. If the customer will apply these conditions (Copper Land, Solder Stop Mask, Solder Print Mask, etc.), further verification or modification of these parameters may be necessary. Please solder the NC pins to NC footprint patterns of the Main Board.

8.1 Reflow times

1 time

Note: This Module is exclusive use of reflow

8.2 Reflow Heat Resistance



Allowable reflow number of times: 1 time Max.

Note:

1. The measurement point is at the center of the upper surface of the module.
2. Please execute the reflow soldering on the following conditions according to JEDEC J-STD-020D.
 Peak Temperature: Max. 260[°C]
 Peak Time ($\geq 255[°C]$): Max. 30[s]

8.3 Storage Conditions

The following conditions shall be kept for soldering and keeping in storage this product.

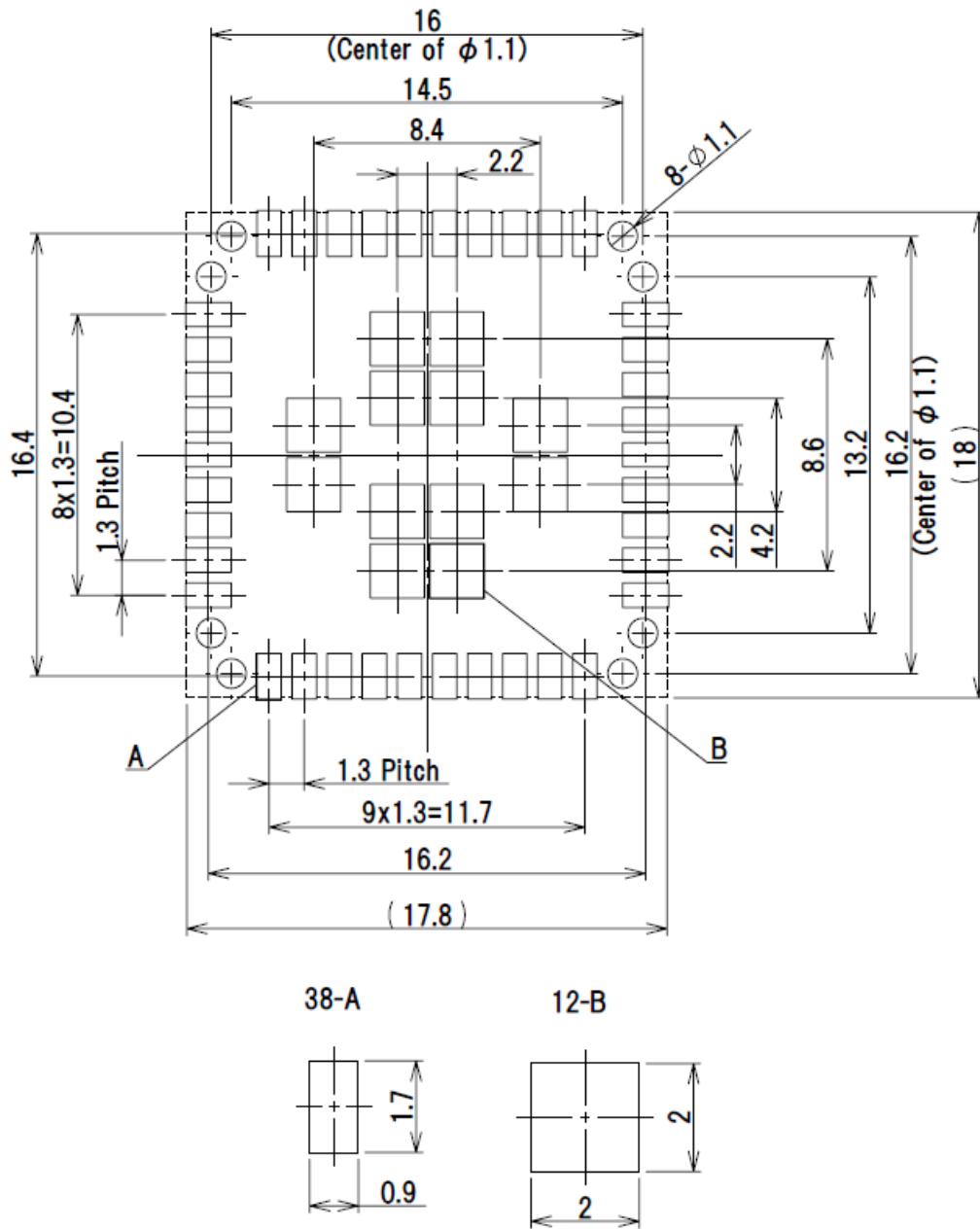
1. Shelf life in dry bag: 12 months at 5 ~ 40 °C and < 85 % RH.
2. After dry bag is opened, module that will be subjected to soldering reflow or equivalent processing must be:
 - a) Mounted within 168 hours at factory condition of < 30 °C / 60 % RH, or
 - b) Stored at < 30 °C / 10 % RH.
3. Modules require baking, before mounting, if:
 - a) Humidity Indicator Card is >10 % when read at 23 °C ± 5 °C, or
 - b) Item 2.a) or 2.b) are not met.
4. If baking is required, device may be baked for 216 hours at 40 ~ 45 °C and < 5 % RH for low-temperature device containers.
 - a) Allowable baking number of times: 1time.

Technical drawing of a square plate with dimensions and labels. The overall dimensions are 16.4 (width) and 16.2 (height, center of $\phi 1$). The plate features a central square area with dimensions 14.5 (width, center of $\phi 1$) and 13.2 (height). The central area is divided into four quadrants by a vertical line (1.3 Pitch) and a horizontal line (1.3 Pitch). The central square has a width of 8.4 and a height of 6.4. The plate is labeled with 38-A, 2-B, and 2-C. The plate is made of 8- $\phi 1$ material. The plate is labeled with 38-A, 2-B, and 2-C. The plate is made of 8- $\phi 1$ material.

Note

1. All are Top View.
2. Recommended Pattern and Solder stop mask on Customer's board and Metal mask dimensions for better soldering with GT-100.
3. Tolerances are $\pm 0.1\text{mm}$, unless otherwise specified.

8.5 Solder Stop Mask Design



units: [mm]

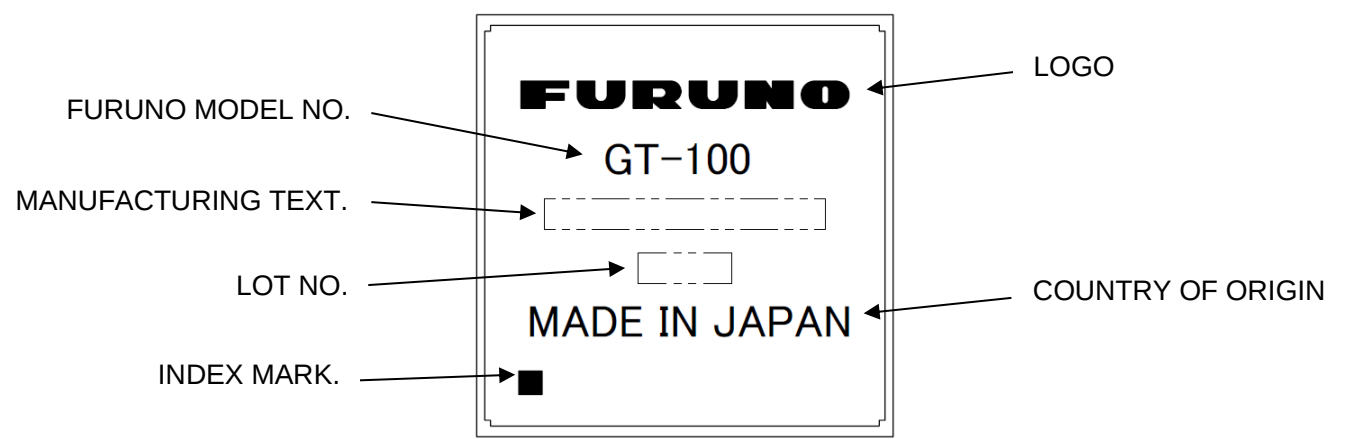
Note

1. All are Top View.
2. Recommended Pattern and Solder stop mask on Customer's board and Metal mask dimensions for better soldering with GT-100.
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1. All are Top View.
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9 Marking



Items	Description																								
LOGO	FURUNO																								
FURUNO MODEL NO	GT-100																								
MANUFACTURING TEXT	The twelve digits max “UMSZ6□□□□□□																								
LOT NO	The three digits “□□□”																								
	Time Bucket(A~E)																								
	Month Code <table><tr><td>Jan</td><td>Feb</td><td>Mar</td><td>Apr</td><td>May</td><td>Jun</td></tr><tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr><tr><td>Jul</td><td>Aug</td><td>Sep</td><td>Oct</td><td>Nov</td><td>Dec</td></tr><tr><td>7</td><td>8</td><td>9</td><td>O</td><td>N</td><td>D</td></tr></table>	Jan	Feb	Mar	Apr	May	Jun	1	2	3	4	5	6	Jul	Aug	Sep	Oct	Nov	Dec	7	8	9	O	N	D
	Jan	Feb	Mar	Apr	May	Jun																			
	1	2	3	4	5	6																			
Jul	Aug	Sep	Oct	Nov	Dec																				
7	8	9	O	N	D																				
Year Code <table><tr><td>CY2022</td><td>CY2023</td><td>CY2024</td></tr><tr><td>2</td><td>3</td><td>4</td></tr></table>	CY2022	CY2023	CY2024	2	3	4																			
CY2022	CY2023	CY2024																							
2	3	4																							
	Note: Last number of Christian years.																								
COUNTRY OF ORIGIN	MADE IN JAPAN																								

10 Special Instruction

10.1 Electronic Component

Components in GT-100 module such as chip resistors, capacitors and TCXO's are planned to be purchased from multiple manufacturers/vendors according to FURUNO's procurement policy. So it is possible that multiple components from multiple manufacturers/vendors could be used even in the same production lot.

10.2 RoHS

GT-100 comply with RoHS directives.

11 Reference Documents

- FURUNO SE22-600-013 GT-100 Function Specifications
- FURUNO SE22-600-007 GT-100 PFEC Protocol Specifications

Supplement: White Paper

If you would like to understand the specifications in depth, please check the technical white paper from the URL below.

Our engineers specializing in time synchronization provide explanations with test results of our anti-jamming and multipath technologies.

- Dual Band GNSS Receivers: Safeguarding Critical Infrastructure

<https://pages.furuno.com/en-gt100-dualband-robustness-downloadform.html>

- White Papers (GNSS Receivers for Time Synchronization)

<https://pages.furuno.com/en-gnsstiming-whitepaper-downloadform.html>