5.0kV$_{RMS}$ Reinforced Isolated Amplifier

Features

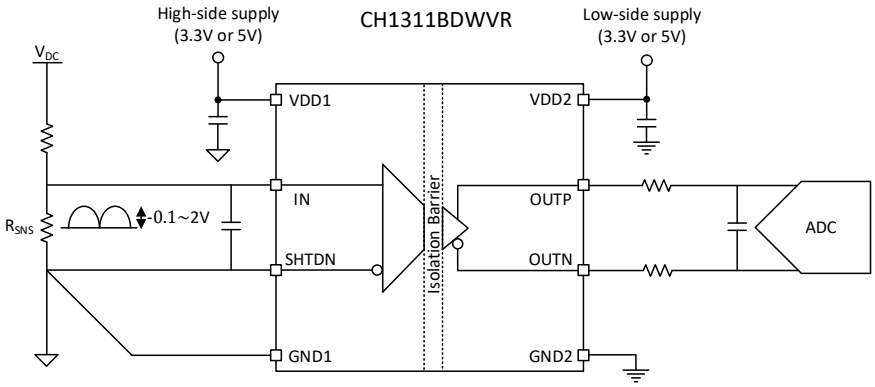
- -0.1V to 2V, high-impedance input voltage range optimized for voltage measurement
- Low offset error and drift:
  ±2.5mV (max), ±10µV/°C (max)
- Fixed gain: 1
- Low gain error and drift:
  ±0.3% (max), ±30ppm/°C (max)
- Low nonlinearity and drift:
  0.04%, ±1ppm/°C (typical)
- 3.3V to 5V operation on high side
- Missing high-side supply indication
- Safety-related certifications:
  7071V$_{PK}$ reinforced isolation per DIN VDE V 0884-17: 2021-10
  5.0kV$_{RMS}$ isolation for 1 minute per UL1577
- High CMTI: 150 kV/µs (typical)

Applications

- Isolated voltage sensing in:
  – Motor drives
  – Frequency inverters
  – Uninterruptible power supplies

PART NUMBER	PACKAGE	BODY SIZE
CH1311BDWVR	WB SOIC-8	5.85mm*7.5mm

Simplified Schematic



1 Pin Configurations and Functions

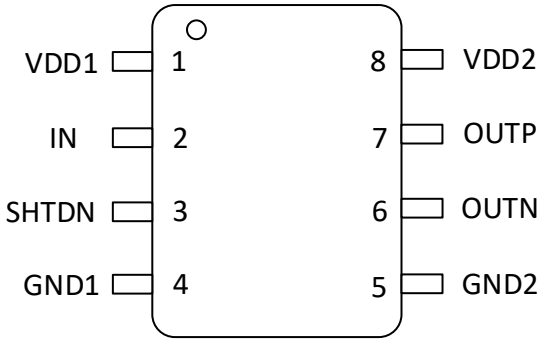


Figure 1. Pin Configuration, Top View

Pin Functions and Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	VDD1	High-side power	High-side power supply, 3.0 V to 5.5 V relative to GND1.
2	IN	Analog input	Analog input.
3	SHTDN	Digital input	Shutdown input, active high, with internal pullup resistor.
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply, 3.0V to 5.5V relative to GND2.

2 Specifications

2.1 Absolute Maximum Ratings (1)

Parameter	Description	MIN	MAX	UNIT
Power supply	VDD1 to GND1	-0.3	6.5	V
	VDD2 to GND2	-0.3	6.5	V
Input voltage	IN	GND1-6	VDD1+0.5	V
	SHTDN	GND1-0.5	VDD1+0.5	
Output voltage	OUTP, OUTN	GND2-0.5	VDD2+0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Junction temperature, T_J	T_J	-40	150	°C
Storage temperature, T_{stg}	T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 ESD Ratings

Parameter		VALUE	UNIT
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

2.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	MIN	MAX	UNIT
High side power supply	VDD1 to GND1	3.0	5.5	V
Low side power supply	VDD2 to GND2	3.0	5.5	V
Specified linear full-scale voltage	IN-GND1	-0.1	2	V
Capacitive load	On OUTP or OUTN to GND2		500	pF
	OUTP to OUTN		250	
Resistive load	On OUTP or OUTN to GND2		1	kΩ
Input voltage	SHTDN to GND1	0	VDD1	
T_A	Ambient Temperature	-40	125	°C

2.4 Thermal Information

Parameter	Description	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43	°C/W

2.5 Insulation Specifications

Parameter	Description	Test Condition	VALUE	UNIT
CLR	External clearance	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
Material group		According to IEC 60664-1	I	
Overvoltage category		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	

DIN V VDE V 0884-17 (VDE V 0884-17): 2021-10(2)

Parameter	Description	Test Condition	VALUE	UNIT
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	1.2/50 µs waveform per IEC 62368-1 $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
$V_{pd(m)}$	Method a, after Input-Output safety test subgroup 2/3	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	2545	V_{PK}
	Method a, after Input-Output safety test subgroup 1	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	3394	V_{PK}
	Method b1, at routine test (100% production) and preconditioning (type test) (4)	Method b1: $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s partial discharge ≤ 5pC	3977	V_{PK}
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4*sin(2πft), f =1MHz	~1.2	pF
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500V at T_S =150°C	> 10^9	Ω
Pollution degree			2	
Climatic category			40/125/21	

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.

(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier are tied together, creating a two-pin device.

UL 1577

Parameter	Description	Test Condition	VALUE	UNIT
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1s (100% production)	5000	V_{RMS}

2.7 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon circuit failure.

Parameter	Description	Test Condition	MIN	TYP	MAX	UNIT
I_S	Safety input, output or supply current	$R_{\theta JA}$=85°C/W, T_J=150°C, T_A =25°C, VDD1=VDD2=5.5V			294	mA
		$R_{\theta JA}$=85°C/W, T_J=150°C, T_A=25°C, VDD1=VDD2=3.3V			445	mA
P_S	Safety input, output or supply power	$R_{\theta JA}$=85°C/W, T_J=150°C, T_A=25°C			1470	mW
T_S	Maximum Safety temperature				150	°C

2.8 Electrical Characteristics

Minimum and maximum specifications of the CH1311B apply from T_A=-40°C to +125°C, VDD1=3.0V to 5.5V, VDD2 =3.0V to 5.5V, IN=0V to 2V, and SHTDN=GND1=0V, typical specifications are at T_A=25°C, VDD1=5V, and VDD2=3.3V (unless otherwise noted).

Parameter		Test Condition	MIN	TYP	MAX	UNIT
INPUT and OUTPUT						
V_{OS}	Input offset voltage (1)	T_A = 25°C	-2.5	±0.5	2.5	mV
TCV_{OS}	Input offset drift (1)		-10	±3	10	µV/°C
R_{IN}	Input resistance			1		GΩ
I_{IB}	Input bias current	T_A = 25°C	-15		15	nA
C_{IN}	Input capacitance	f_{IN} = 275 kHz		25		pF
GAIN	Normal gain			1		V/V
E_G	Gain error (1)	T_A = 25°C	-0.3%	±0.05%	0.3%	
TCE_G	Gain error drift (1)		-30	±5	30	ppm/°C
NL	Nonlinearity (1)		-0.04%	±0.01%	0.04%	
TC_{NL}	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion	V_{IN} = 2V, f_{IN} = 10 kHz, BW = 100 kHz		-83		dB
SNR	Signal to noise ratio	V_{IN} = 2V, f_{IN} = 1 kHz, BW = 10 kHz		81		dB
		V_{IN} = 2V, f_{IN} = 10 kHz, BW = 100 kHz		71		dB
$NOISE_{OUT}$	Output noise	V_{IN}= GND1, BW =100kHz		250		uV_{RMS}
PSRR	Power-supply rejection ratio	PSRR vs VDD1, at DC		-95		dB
		PSRR vs VDD1, 100mV and 10kHz ripple		-85		
		PSRR vs VDD2, at DC		-95		
		PSRR vs VDD2, 100mV and 10kHz ripple		-85		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{Clipping}$	Input Voltage before clipping output	IN to GND1		2.516		V
$V_{CLIPout}$	Clipping differential output voltage	V_{IN} > $V_{Clipping}$		2.5		V
$V_{FAILSAFE}$	Failsafe differential output voltage			-2.6	-2.5	V
BW	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	OUTP or OUTN		0.2		Ω
I_{SC}	Output short-circuit current	VDD2 or GND2		±13		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV	100	150		kV/us
I_{IN}	SHTDN pin, GND1 ≤ SHTDN ≤ VDD1		-70		1	uA
V_{IH}	High level of input voltage		0.77* VDD1			V

Parameter		Test Condition	MIN	TYP	MAX	UNIT
V_{IL}	Low level of input volage				0.28* VDD1	V
POWER SUPPLY						
$VDD1_{UVLO}$	VDD1 undervoltage detection threshold	VDD1 Rising	2.3	2.5	2.7	V
	VDD1 undervoltage hysteresis	Hysteresis		0.15		V
$VDD2_{UVLO}$	VDD2 undervoltage detection threshold	VDD2 Rising	2.2	2.4	2.6	V
	VDD2 undervoltage hysteresis	Hysteresis		0.35		V
IDD1	High-side supply current	3.0V ≤ VDD1 ≤ 5.5V		4	6	mA
IDD2	Low-side supply current	3.0V ≤ VDD2 ≤ 5.5V		3	5	mA

(1) The typical value includes one sigma statistical variation.
(2) This parameter is output referred.

2.9 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN			1.0		us
t_f	Fall time of OUTP, OUTN			1.0		us
t_{PD}	IN to OUTP, OUTN (50% – 10%)	Unfiltered output, see Fig2		0.7	1	us
	IN to OUTP, OUTN (50% – 50%)	Unfiltered output, see Fig2		1.2	1.5	us
	IN to OUTP, OUTN (50% – 90%)	Unfiltered output, see Fig2		1.7	2	us
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0V, to OUTP, OUTN valid, 0.1% settling		350		us
t_{EN}	Device enable time	SHTDN high to low		350		us
t_{SHTDN}	Device shut down time	SHTDN low to high		3	10	us

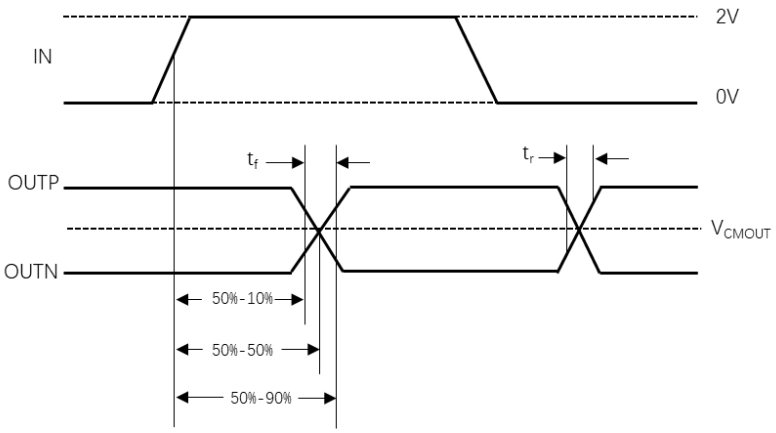


Figure 2. Rise, Fall, and Delay Time Waveforms

2.10 Typical Characteristics

VDD1 = 5V, VDD2 = 3.3V, V_{IN} = 2V, SHTDN = 0V, f_{IN} = 10kHz, and BW = 100kHz (unless otherwise noted)

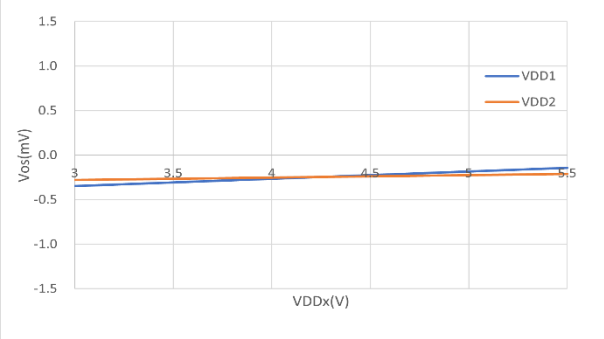


Figure 3. Input Offset Voltage vs Supply Voltage

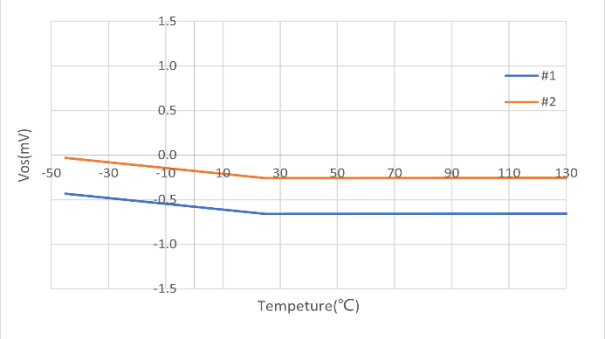


Figure 4. Input Offset Voltage vs Temperature

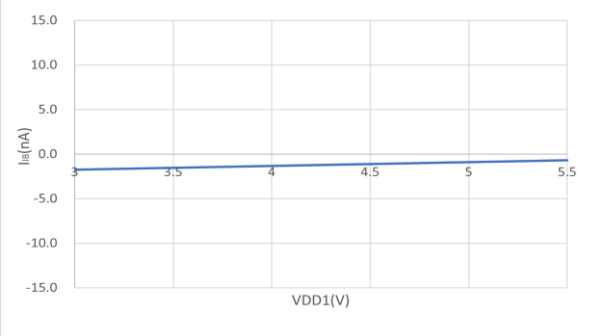


Figure 5. Input Bias Current vs High-Side Supply Voltage

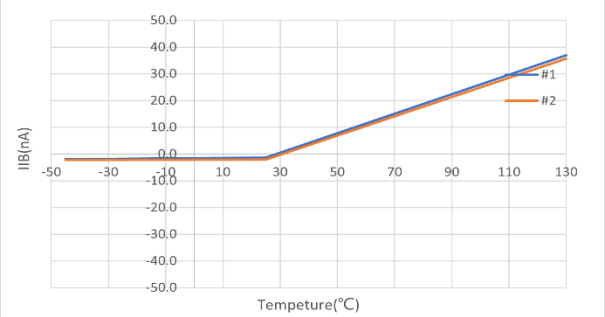


Figure 6. Input Bias Current vs Temperature

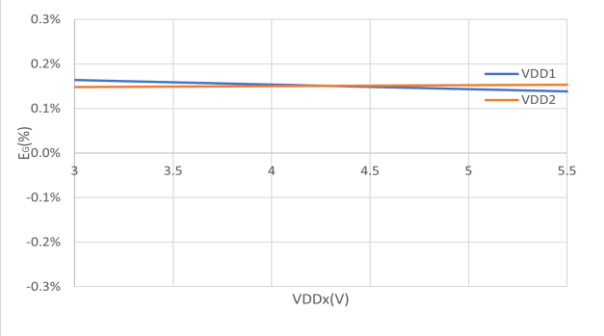


Figure 7. Gain Error vs Supply Voltage

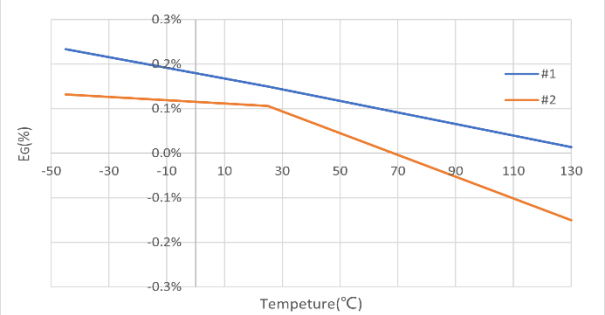


Figure 8. Gain Error vs Temperature

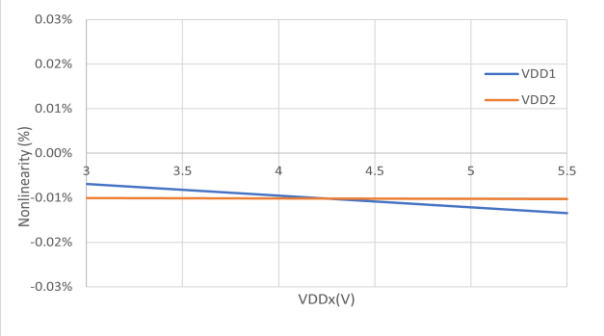


Figure 9. Nonlinearity vs Supply Voltage

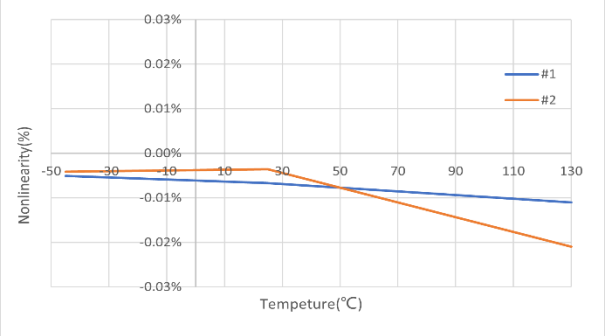


Figure 10. Nonlinearity vs Temperature

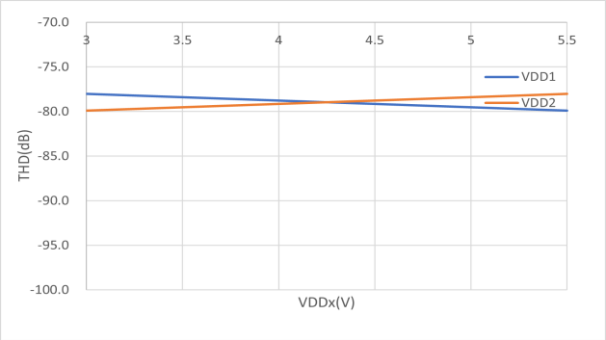


Figure 11. Total Harmonic Distortion vs Supply Voltage

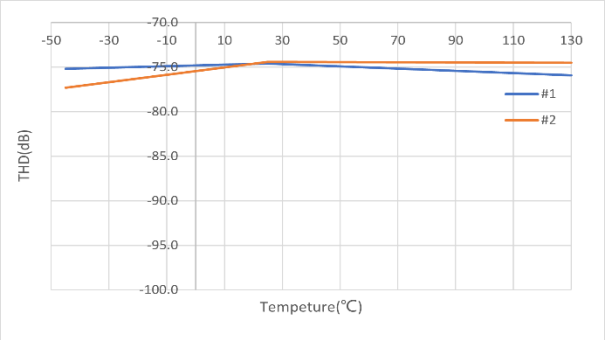


Figure 12. Total Harmonic Distortion vs Temperature

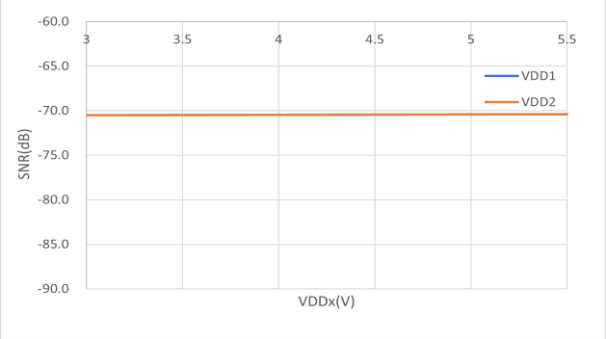


Figure 13. Signal-to-Noise Ratio vs Supply Voltage

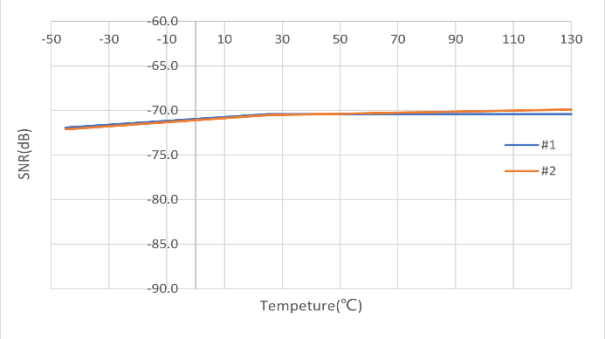


Figure 14. Signal-to-Noise Ratio vs Temperature

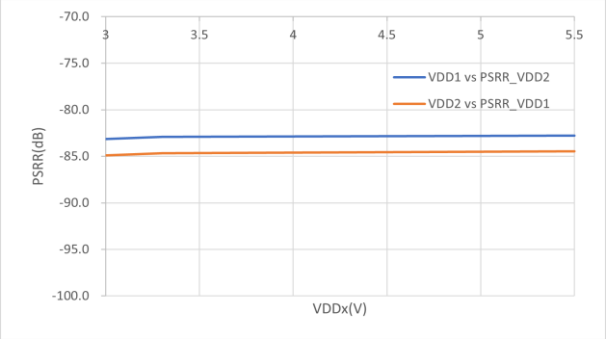


Figure 15. Power-Supply Rejection Ratio vs Supply Voltage

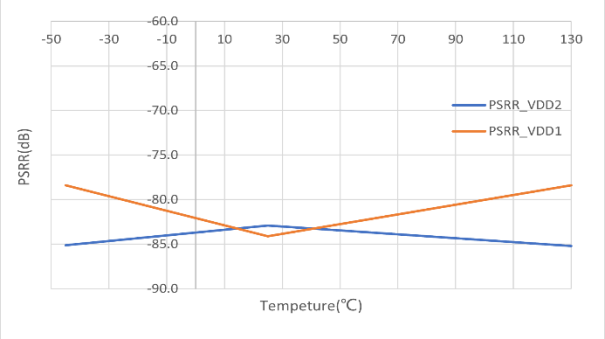


Figure 16. Power-Supply Rejection Ratio vs Temperature

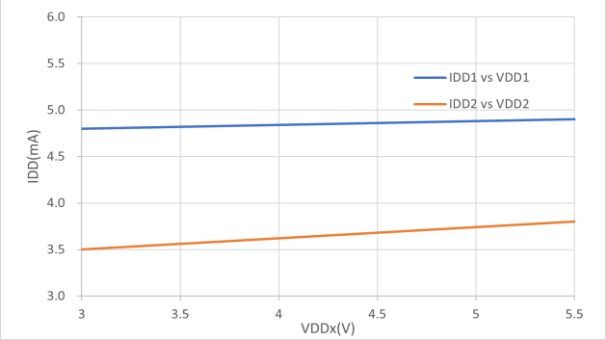


Figure 17. Supply Current vs Supply Voltage

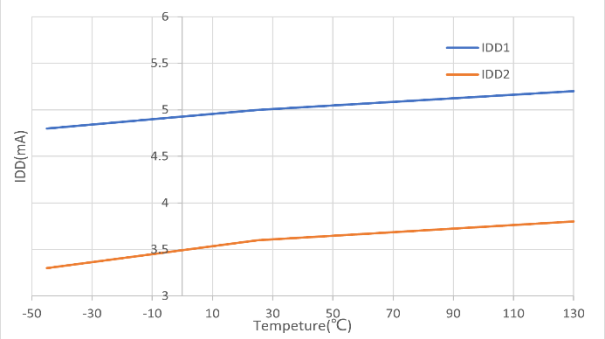


Figure 18. Supply Current vs Temperature

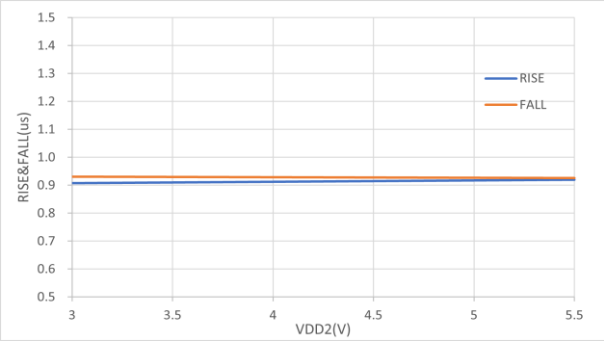


Figure 19. Output Rise and Fall Time vs Low-Side Supply

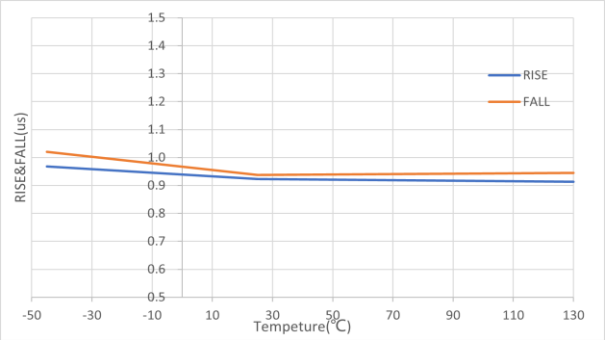


Figure 20. Output Rise and Fall Time vs Temperature

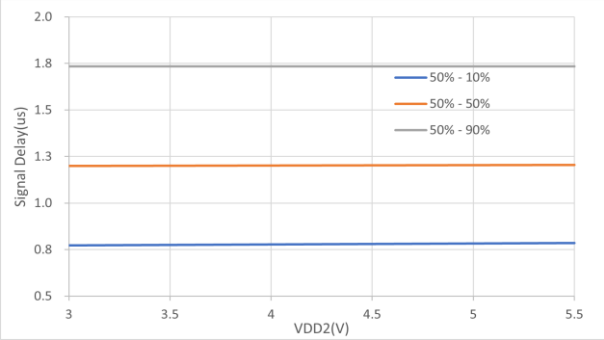


Figure 21. VIN to VOUT Signal Delay vs Low-Side Supply Voltage

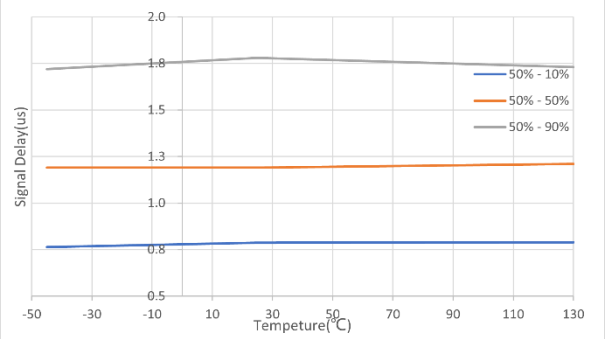


Figure 22. VIN to VOUT Signal Delay vs Temperature

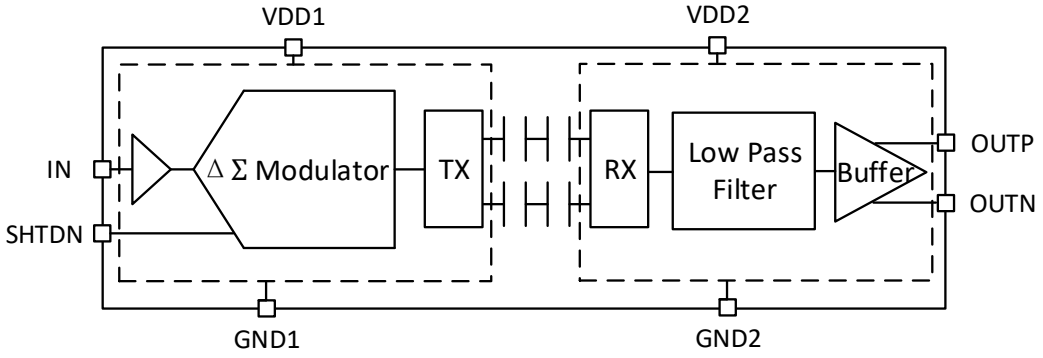
3 Detailed Description

3.1 Overview

The CH1311B single is a -ended input, precision, isolated amplifier with a high input impedance and wide input voltage range. The input stage drives a second-order, delta-sigma (ΔΣ) modulator. The modulator generates data pulse. The drivers (called TX in the Functional Block Diagram) transfer the data pulse of the modulator across the isolation barrier. The received data pulse is synchronized and processed, as shown in the Functional Block Diagram, by a low pass filter and out buffer on the low-side and presented as a differential output of the device.

CH1311B adopts single channel transfer architecture and saves one clock channel, compared with current other amplifiers products, CH1311B has the lowest power consumption. CH1311B also uses Intelligent voltage divider technology (iDivider® technology) which is a new generation digital isolator technology invented by Tokmas to support a high level of magnetic field immunity.

3.2 Function block diagram



3.3 Feature Description

3.3.1 Analog Input

The single-ended, high-impedance input stage of the CH1311B feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into data pulse that is transferred across the isolation barrier, as described in patented iDivider® technology.

There are two restrictions on the analog input signals (IN). First, if the input voltage exceeds the range GND1-6V to VDD1+0.5V, the input current must be limited to 10mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR).

3.3.2 Isolation Channel Signal Transmission

The CIH1311B uses the patentediDivider® technology to transmit the modulator output data pulse across the SiO_2 -based isolation barrier. The CH1311B also uses special circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

3.3.3 Failsafe Output

The CH1311B offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active when the high-side supply VDD1 of the CH1311B is missing.

The fail-safe outputs a negative differential output voltage value that does not occur under normal device operation which is marked as $V_{FAILSAFE}$ and specified in the electrical characteristics table as a reference value for the fail-safe detection on a system level.

4 Application and Implementation

4.1 Application Information

The high input impedance, low input bias current, low AC and DC errors, and low temperature drift make the CH1311B a high-performance solution for automotive applications where voltage sensing in the presence of high common-mode voltage levels is required.

4.2 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is high and only a small-value filter capacitor can be used to not limit the signal bandwidth to an unacceptable low value. Design the input filter such that:

• The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator.

• The input bias current does not generate significant voltage drop across the DC impedance of the input filter Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in Figure 23) is sufficient to filter the input signal.

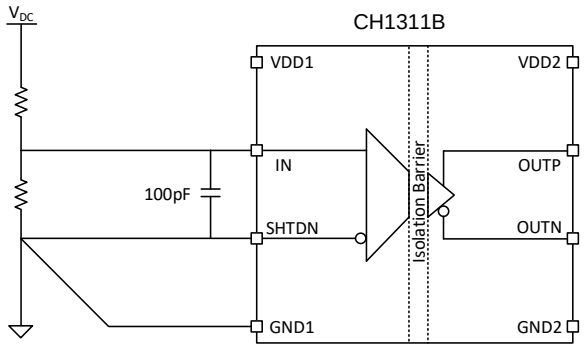


Figure 23. Input Filter Design

4.3 Differential to Single-Ended Output Conversion

Figure 24 shows an example of an amplifier-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (VOUTP – VOUTN) + VREF. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

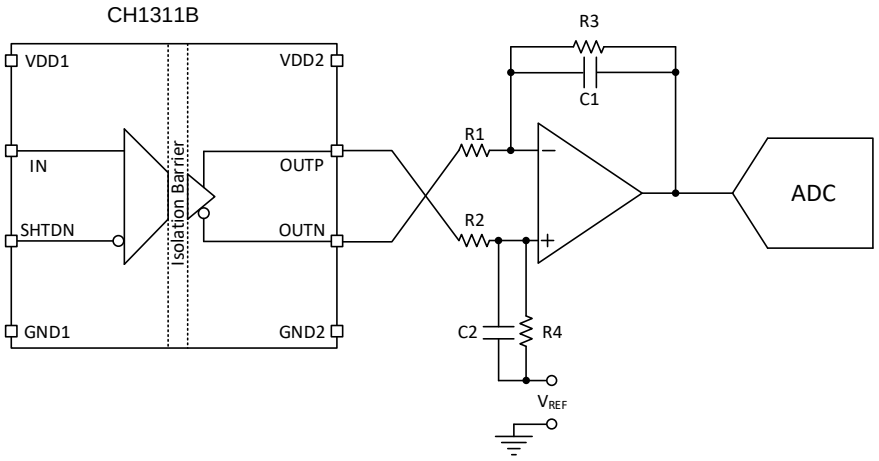


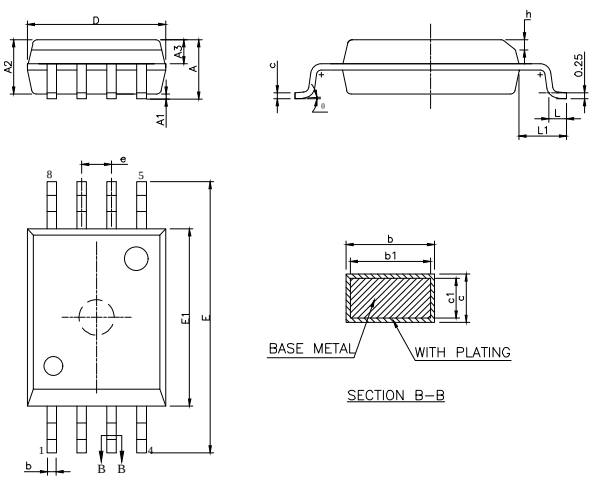
Figure 24. Connecting the CH1311B Output to a Single-Ended Input ADC

4.4 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5V or 3.3V ± 10%. Alternatively, a low-cost low-dropout (LDO) regulator may be used to minimize noise on the power supply. A low-ESR decoupling capacitor of 0.1µF to filter this power-supply path is recommended. Place this capacitor as close as possible to the VDD1 pin of the CH1311B for best performance.

If better filtering is required, an additional 2.2µF capacitor may be used. The floating ground reference (GND1) is derived from the end of the sensing resistor, which is connected to the shut-down pin of the device. To decouple the low-side power supply on the controller side, use a 0.1µF capacitor placed as close to the VDD2 pin of the CH1311B as possible, followed by an additional capacitor from 1 µF to 10 µF.

5 Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	1.00
L1	2.00REF		
θ	0	—	8°

Figure 25. Outline Package

6 Land Patterns

The Fig.26 illustrates the recommended land pattern details for the CH1311B in an 8-pin wide-body SOIC package.

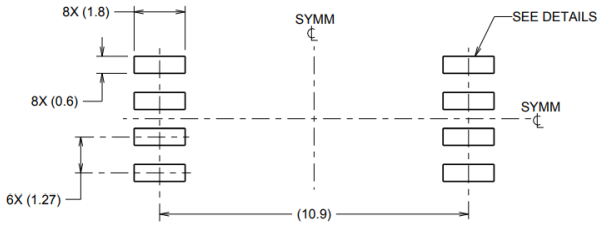


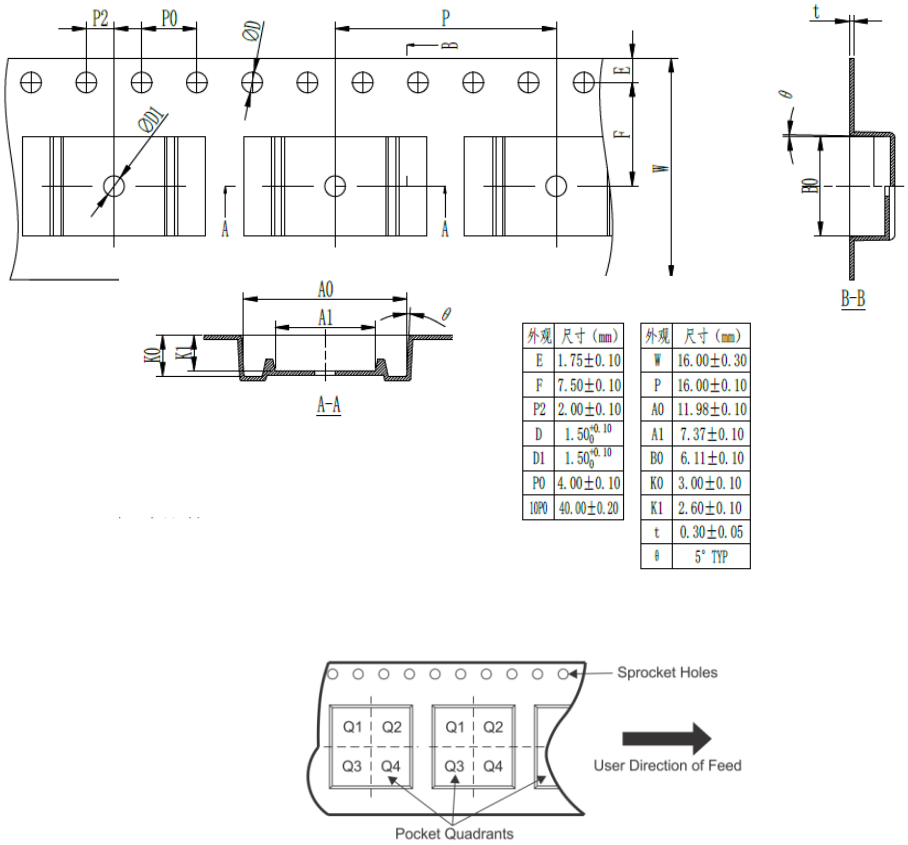
Figure 26. WB-SOIC-8 Land Pattern

Note：

(1) This land pattern design is based on IPC -7351

(2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

8 Reel Information



外观	尺寸（mm）
E	1.75±0.10
F	7.50±0.10
P2	2.00±0.10
D	$1.50^{+0.10}_{0}$
D1	$1.50^{+0.10}_{0}$
P0	4.00±0.10
10P0	40.00±0.20

外观	尺寸（mm）
W	16.00±0.30
P	16.00±0.10
A0	11.98±0.10
A1	7.37±0.10
B0	6.11±0.10
K0	3.00±0.10
K1	2.60±0.10
t	0.30±0.05
θ	5° TYP

Figure 28. Reel Information

Note: The Pin 1 of the chip is in the quadrant Q1.

9 Ordering Guide

Model Name	Temperature Range	Withstand Voltage Rating (kV_{RMS})	Package	MSL Peak Temp [1]	Quantity per Reel
CH1311BDWVR	−40~125°C	5.0	WB SOIC-8	Level-3-260C-168 HR	1000

(1) The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.