Capless 3V_{rms} Line Driver with Adjustable Gain

FEATURES

- Capless Structure
- Eliminates Pop/Clicks
- Eliminates Output DC-Blocking Capacitors
- Provides Flat Frequency Response from DC to 20kHz
- Low Noise and THD
  Typical SNR=90dB
  Typical THD+N=0.01%(f=1kHz)
- 3Vrms Output Voltage into 2.5kΩ Load with 5V Supply Voltage
- Differential Input

APPLICATIONS

- Set-Top Box
- LCD TV
- Blue-Ray DVD-Players
- Home Theater in a Box

GENERAL DESCRIPTION

The TMI8320B is a 3Vrms pop/click-free stereo line driver designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics when size and cost are critical design parameters.

The TMI8320B is capable of driving 3Vrms into a 2.5kΩ load with 5V supply voltage. The device has differential inputs and uses external gain setting resistors that supports a gain range of ±1V/V to ±10V/V. The TMI8320B has built-in shutdown control for pop/click-free on/off control.

Using the TMI8320B in audio products can reduce component count compared to traditional methods of generating a 3Vrms output. The TMI8320B doesn't require a power supply greater than 5V to generate an 8.5V_{PP} output, nor does the device require a split rail power supply. The TMI8320B integrates a charge pump to generate a negative supply rail that provides a clean, pop/click-free ground-biased 3Vrms output.

The TMI8320B is available in Green MSOP10-EP package. It operates over an ambient temperature range of -40°C to 85°C.

TYPICAL APPILCATION

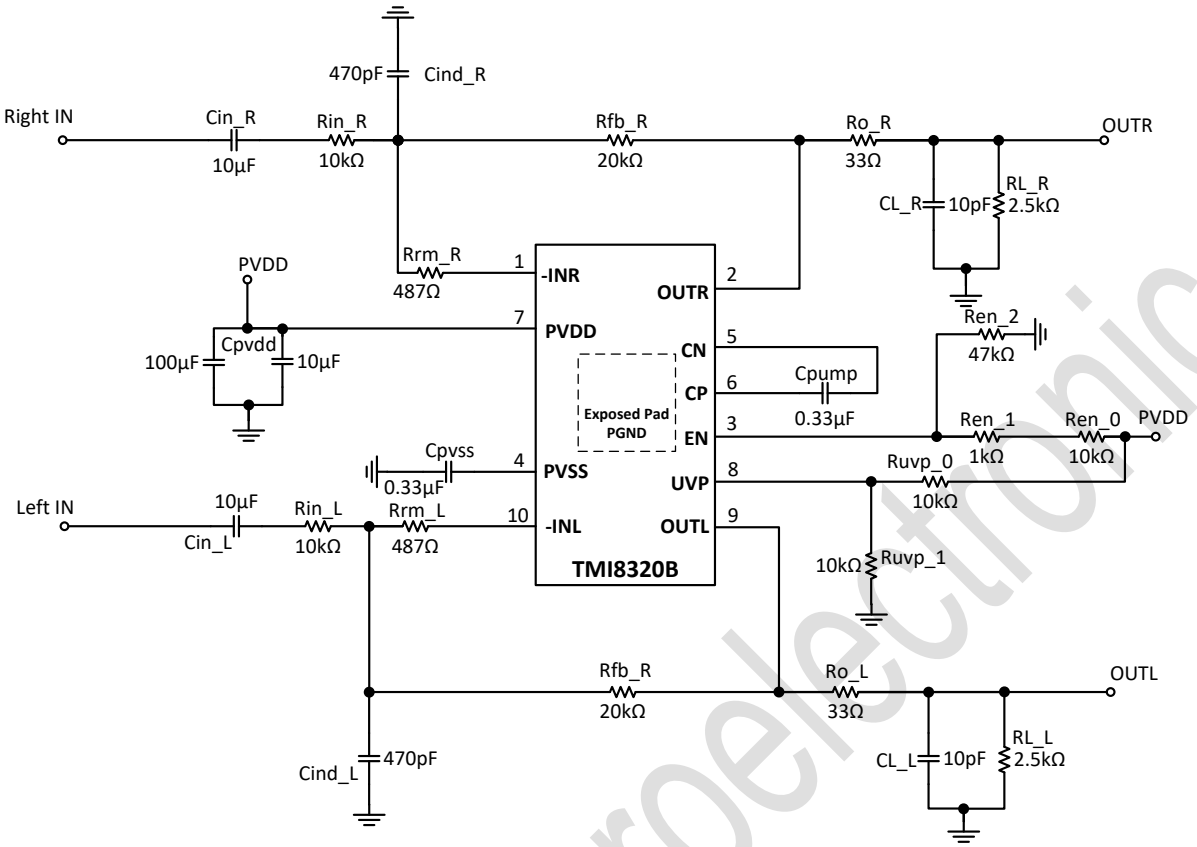
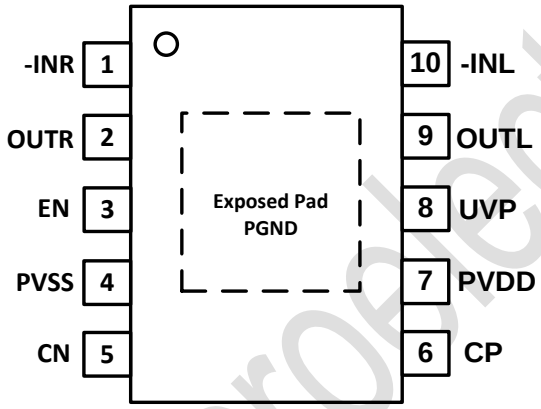


Figure 1. TMI8320B Application Circuit

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Value	Unit
Supply Voltage	-0.3~6	V
Input Voltage	Vss-0.3 to Vdd+0.3	V
Minimum Load Impedance (RL)	600	Ω
EN to GND	-0.3 to Vdd+0.3	V
Junction Temperature (Note2)	150	°C
Storage Temperature Range	-65~150	°C
Lead Temperature (Soldering,10s)	260	°C

PIN CONFIGURATION



MSOP10-EP

Top Mark: T8320B/YYXXX (T8320B: Device Code, YYXXX: Inside code)

Part Number	Package	Top mark	Quantity/ Reel
TMI8320B	MSOP10-EP	T8320B/YYXXX	4000

TMI8320B devices are Pb-free and RoHS compliant.

PIN FUNCTIONS

Pin No.	Name	Function
1	-INR	Right Channel OPAMP Positive input (connected to GND)
2	OUTR	Right Channel OPAMP Output
3	EN	Enable Input. Active high
4	PVSS	Negative Supply Voltage Output
5	CN	Charge Pump Flying Capacitor Negative Terminal
6	CP	Charge Pump Flying Capacitor Positive Terminal
7	PVDD	Positive Supply
8	UVP	Under voltage Protection Input
9	OUTL	Left Channel OPAMP Output
10	-INL	Left Channel OPAMP Negative Input
Exposed Pad	PGND	Power Ground

ESD RATINGS

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	3000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN	3	5.5	V
T_J	Operating Junction Temperature Range	-40	125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, T_A = 25°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{os}	Output Offset Voltage	V_{DD}=3V to 5V		1.5	5	mV
PSRR	Power Supply Rejection Ratio	V_{DD}=3V to 5V		90		dB
V_{CH}	High-Level Output Voltage	V_{DD}=3.3V, R_L=2.5kΩ	3.18			V
V_{OL}	Low-Level Output Voltage	V_{DD}=3.3V, R_L=2.5kΩ			-3.1	V
I_{IH}	High-Level Input Current (EN)	V_{DD}=5V, VI=V_{DD}			1	μA
I_{IH}	Low-Level Input Current (EN)	V_{DD}=5V, VI=0V			1	μA
I_{DD}	Supply Current	V_{DD}=3.3V, No load, EN=V_{DD}	8	11.3		mA
		V_{DD}=5V, No load, EN=V_{DD}		11.7	18	
		Shutdown mode, V_{DD}=3V to 5V		0.1	0.2	
V_O	Output Voltage (Outputs in Phase)	THD+N=1%, VDD=3.3V, f=1kHz, R_L=2.5kΩ		2.28		V_{rms}
		THD+N=1%, VDD=5V, f=1kHz, R_L=2.5kΩ		3.50		
		THD+N=1%, VDD=5V, f=1kHz, R_L=100kΩ		3.57		
THD+N	Total Harmonic Distortion Plus Noise	V_O=2Vrms, f=1kHz, R_L=2.5kΩ		0.01		%
		V_O=3Vrms, f=1kHz, R_L=2.5kΩ		0.01		%
X_{TALK}	Crosstalk	V_O=2Vrms, f=1kHz, R_L=2.5kΩ		-90		dB
		V_O=3Vrms, f=1kHz, R_L=2.5kΩ		-88		dB
I_O	Output Current Limit	V_{DD} = 3.3V		20		mA
R_{IN}	Input Resistor Range		1	10	47	kΩ
R_{FB}	Feedback Resistor Range		4.7	20	100	kΩ
SR	Slew Rate			8		V/μs
C_{LOAD_Max}	Maximum Capacitive Load			220		pF
V_N	Noise Output Voltage	A-weighted, BW = 20kHz		30		$μV_{rms}$
SNR	Signal to Noise Ratio	V_O=3Vrms, THD+N=0.1%, BW=20kHz, A-Weighted		90		dB
G_{BW}	Unity Gain Bandwidth			5.4		MHz
A_{VO}	Open-Loop Voltage Gain			110		dB

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CP}	Charge Pump Frequency		300	417	540	kHz
V_{UVP}	External Under Voltage Detection		1.05	1.15	1.25	V
I_{HYS}	External Under Voltage Detection Hysteresis Current			4.6		μA
V_{EN_H}	Input High Voltage Threshold	V_{DD}=5V		1.65		V
V_{EN_L}	Input Low Voltage Threshold	V_{DD}=5V		0.6		V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula: $T_J = T_A + (P_D) \times \theta_{JA}$.

FUNCTIONAL BLOCK DIAGRAM

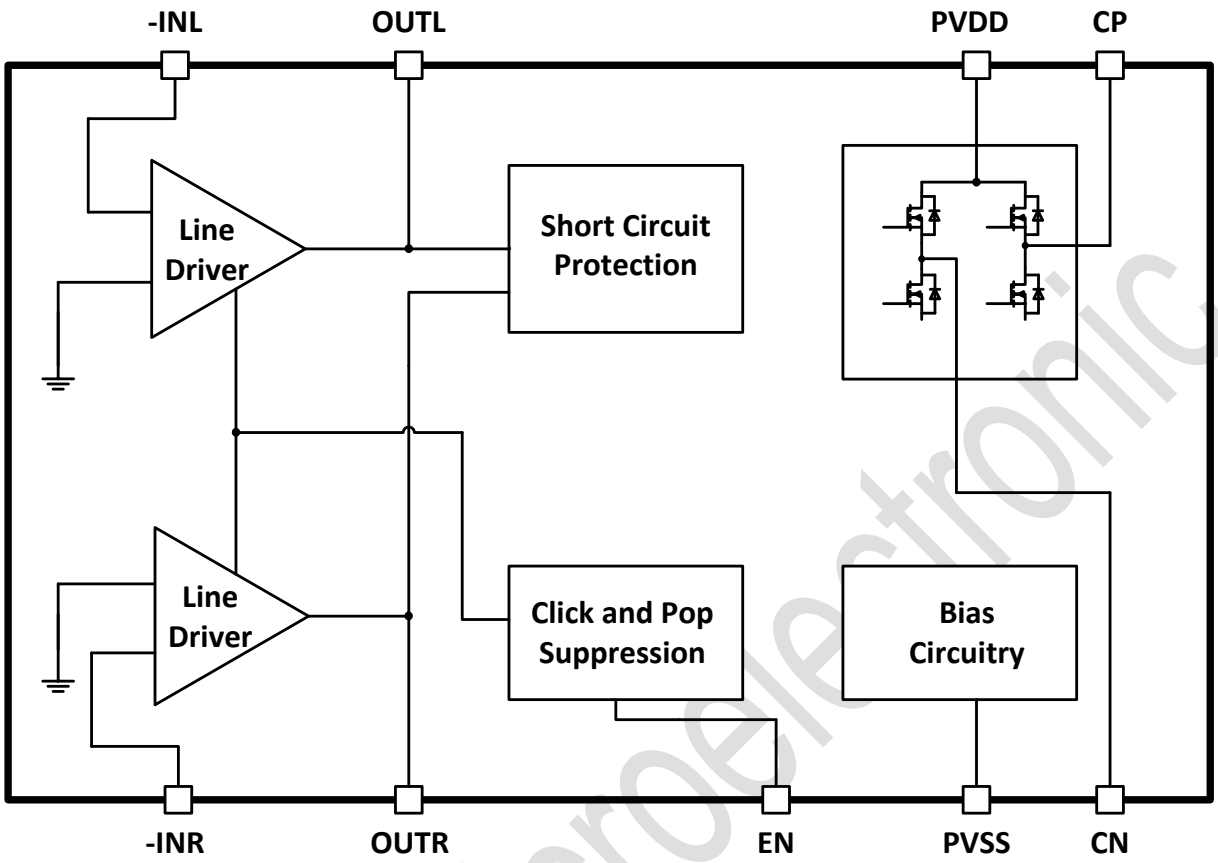
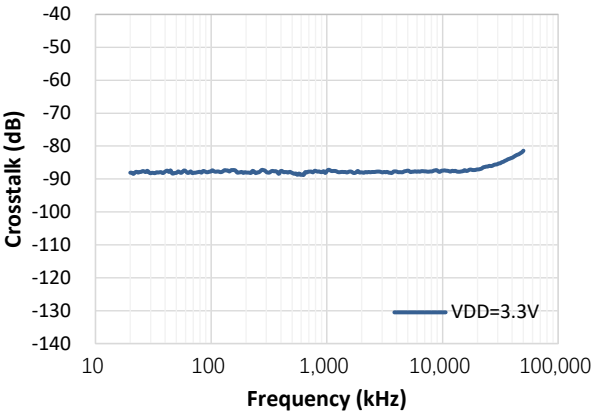


Figure 2. TMI8320B Block Diagram

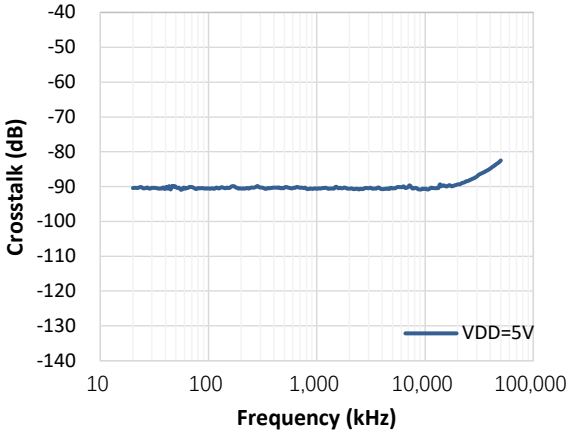
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = 3.3V, R_L = 2.5kΩ, C_{PUMP} = 0.33μF, C_{PVSS} = 0.33μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, T_A = 25°C, unless otherwise noted.)

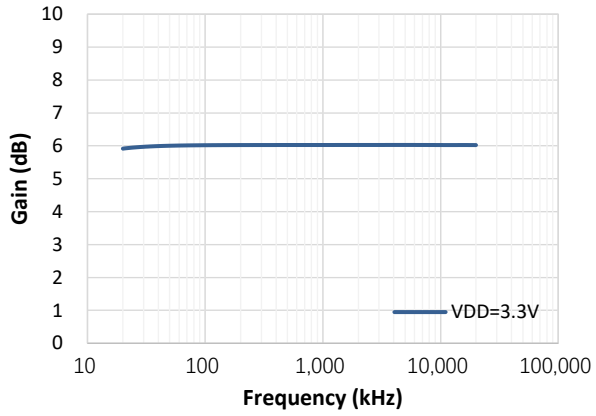
Crosstalk at V_{DD}=3.3V



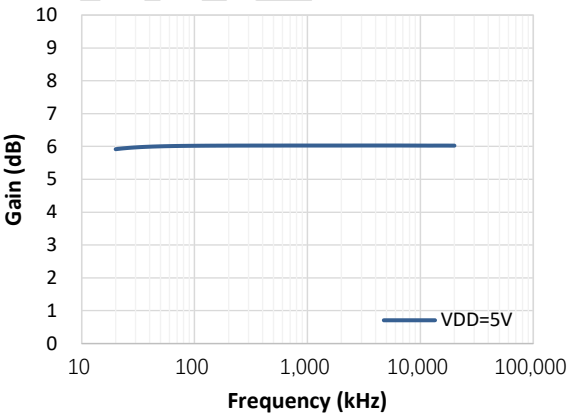
Crosstalk at V_{DD}=5V



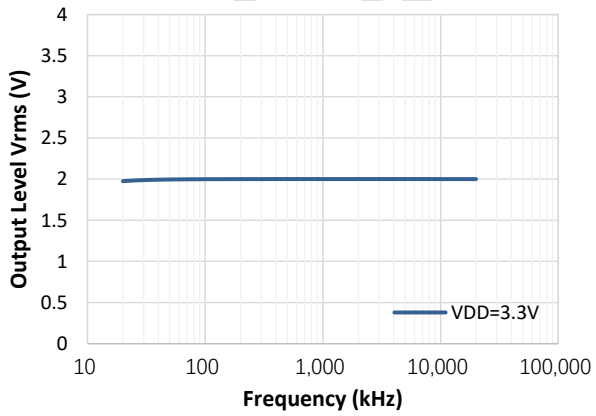
Gain at V_{DD}=3.3V



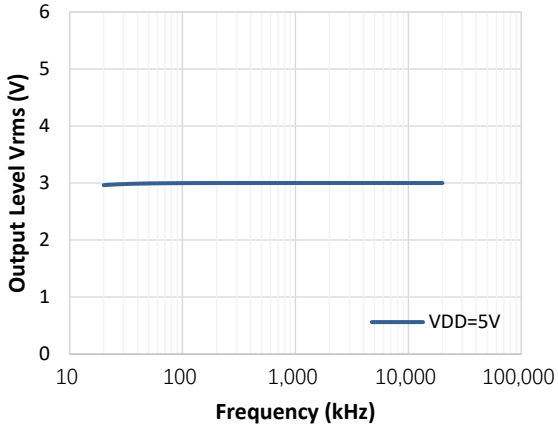
Gain at V_{DD}=5V



Output V_{rms} Level at V_{DD}=3.3V



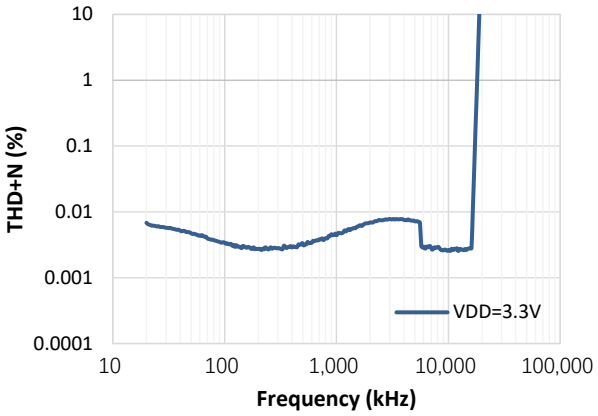
Output V_{rms} Level at V_{DD}=5V



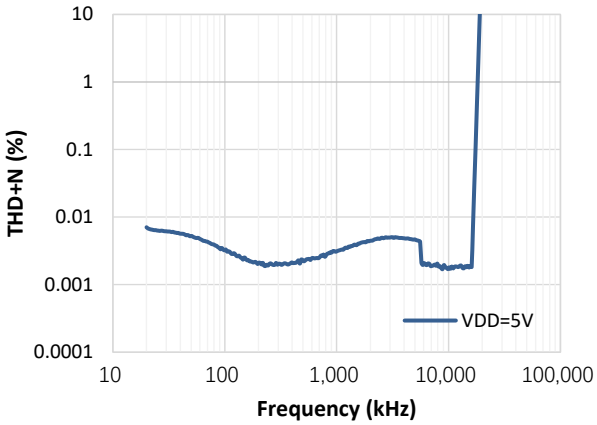
TYPICAL PERFORMANCE CHARACTERISTICS (Continuous)

(V_{DD} = 3.3V, R_L = 2.5kΩ, C_{PUMP} = 0.33µF, C_{PVSS} = 0.33µF, C_{IN} = 10µF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, T_A = 25°C, unless otherwise noted.)

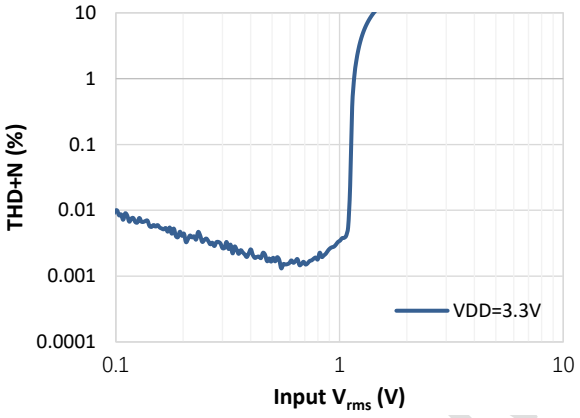
THD+N vs. Frequency at V_{DD}=3.3V



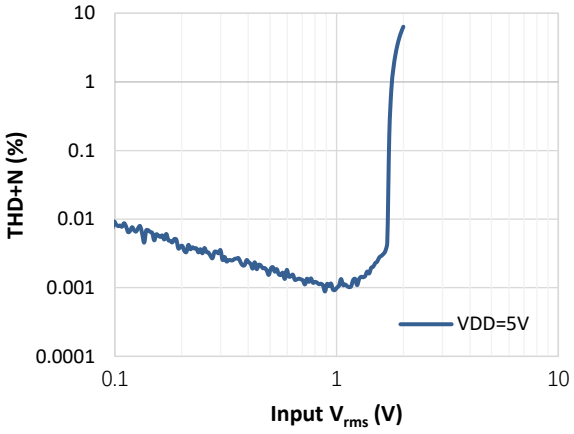
THD+N vs. Frequency at V_{DD}=5V



THD+N vs Input V_{rms} at V_{DD}=3.3V



THD+N vs Input V_{rms} at V_{DD}=5V



APPLICATION INFORMATION

Decoupling Capacitors

The TMI8320B is a capless line driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device PVDD lead, works best. Placing this decoupling capacitor close to the TMI8320B is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10μF or larger capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Gain Setting Resistors Ranges

The gain setting resistors, R_{IN} and R_{FB}, must be chosen so that noise, stability and input capacitor size of the TMI8320B are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN}.
Selecting values that are too low demands a large input AC coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Input Resistor Value, R_{IN}	Feedback Resistor Value, R_{FB}	Inverting Input Gain
22kΩ	22kΩ	1.0V/V
20kΩ	30kΩ	1.5V/V
33kΩ	68kΩ	2.1V/V
10kΩ	100kΩ	10.0V/V

Table 1. Recommended Resistor Values

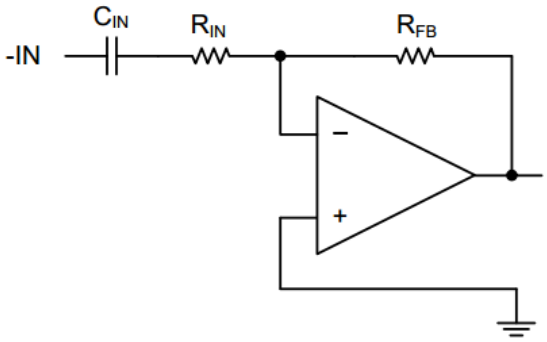


Figure 3.R_{IN} R_{FB} resistor

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TMI8320B. These capacitors block the DC portion of the audio source and allow the TMI8320B inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC-gain to one, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the tow values are given.

$f_{CIN}=1/(2\pi \times R_{IN} \times C_{IN})$ or $C_{IN}=1/(2\pi \times f_{CIN} \times R_{IN})$ (Equation 1)

Pop-Free Power Up

Pop-free power up is ensured by keeping the SD (EN) (shutdown pin) low during power supply ramp up and down. The EN pin should be kept low until the input AC coupling capacitors are fully charged before asserting the EN pin high. This way proper pre-charge of the AC coupling is performed, and pop-free power-up is achieved. Figure below illustrates the preferred sequence.

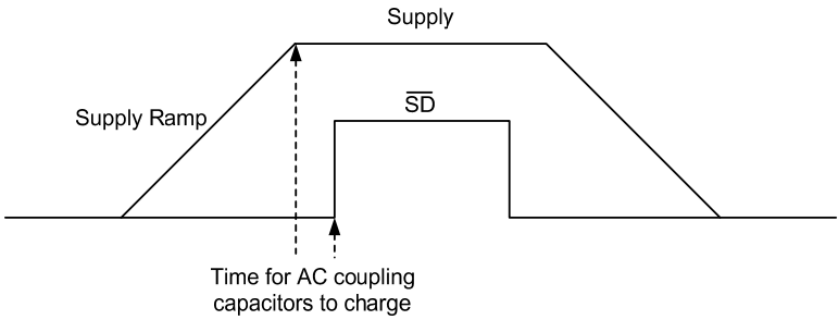


Figure 4. Power-Up Sequence

External Under Voltage Detection

External under voltage detection can be used to mute/shut down the TMI8320B before an input device can generate a pop.

The threshold seen at the UVP pin is 1.15V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:

Startup Threshold: VUDPR= 1.15 x (R11+R12)/R12

Shutdown Threshold: VUDPF= 1.15 x (R11+R12)/R12-Iuvp x (R13+R11||R12) x (R11+R12)/R12

Hysteresis: Iuvp x (R13+R11||R12) x (R11+R12)/R12

The R13 is optional. If the R13 is not used, the UVP pin connects to the divider center tap directly.

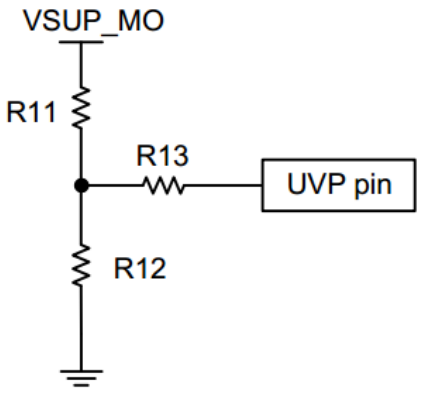


Figure 5. UVP Resistors

Capacitive Load

The TMI8320B has the ability to drive large capacitive load up to 220pF directly, and larger capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

Gain-Setting Resistors

The gain setting resistors, R_{IN} and R_{FB}, must be placed close to the input pins to minimize the capacitive loading on these pins and to ensure maximum stability of the TMI8320B.

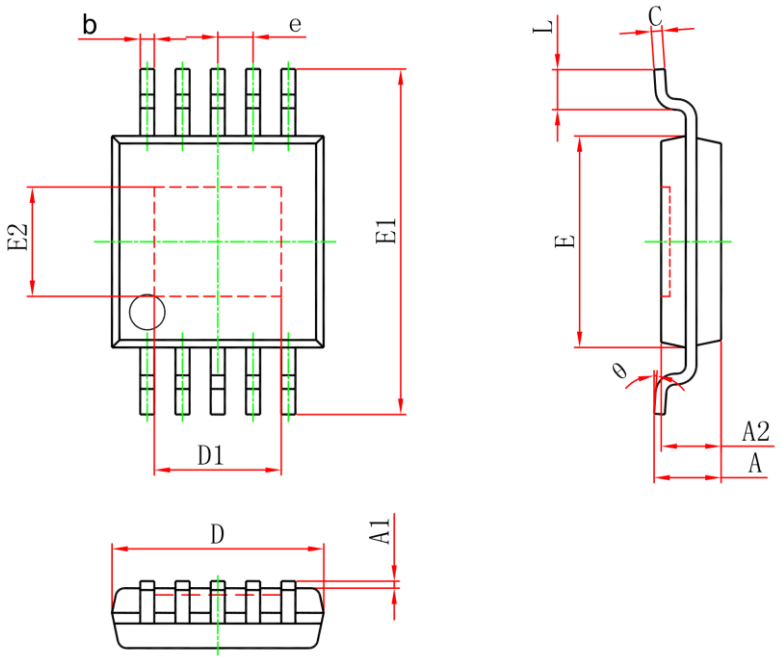
Layout Consideration

For best performance of the TMI8320B, the following guidelines must be strictly followed.

1) 0.1μF decoupling capacitor must be close to PGND and PVDD pins.
2) Capacitor can be connected between PVDD and PGND pins directly and then connect PGND pin to GND layer.

PACKAGE INFORMATION

MSOP10-EP



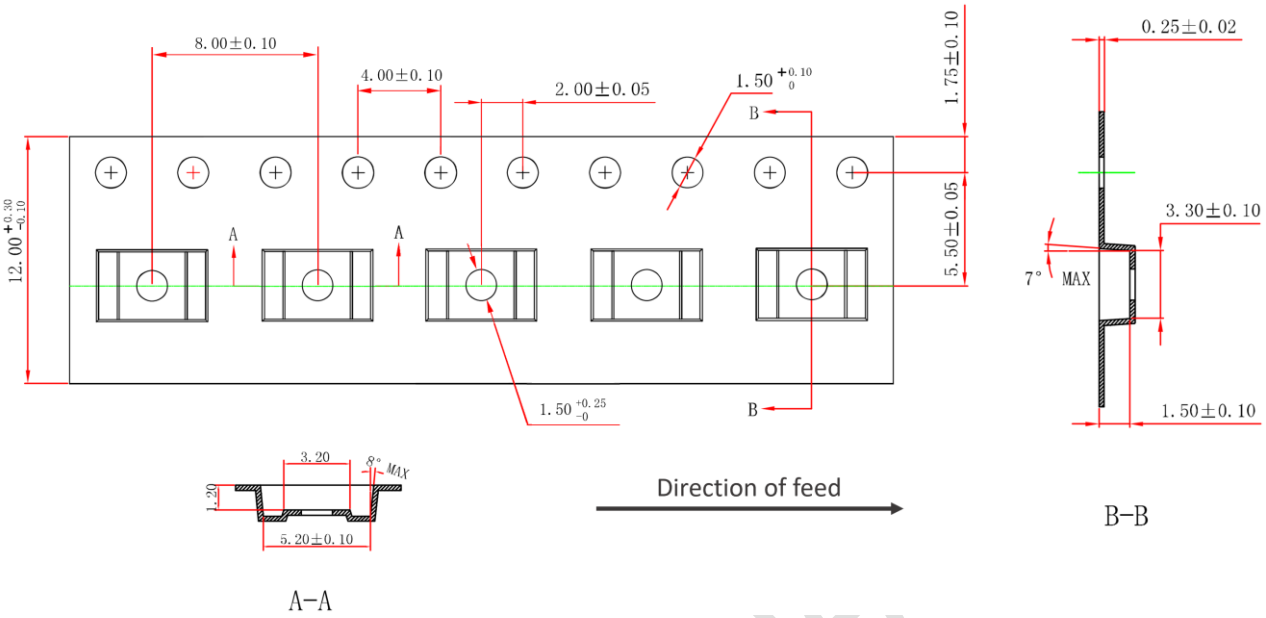
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.820	0.960	1.100	0.032	0.0375	0.043
A1	0.020	0.585	1.150	0.001	0.0035	0.006
A2	0.750	0.850	0.950	0.030	0.0335	0.037
b	0.180	0.230	0.280	0.007	0.009	0.011
c	0.090	0.160	0.230	0.004	0.0065	0.009
D	2.900	3.000	3.100	0.114	0.118	0.122
D1	1.700	1.800	1.900	0.067	0.071	0.075
E	2.900	3.000	3.100	0.114	0.118	0.122
E1	4.750	4.900	5.050	0.187	0.193	0.199
E2	1.450	1.550	1.650	0.057	0.061	0.065
e	0.500 BSC			0.020 BSC		
L	0.400	0.600	0.800	0.016	0.0235	0.031
θ	0°	3°	6°	0°	3°	6°

Note:

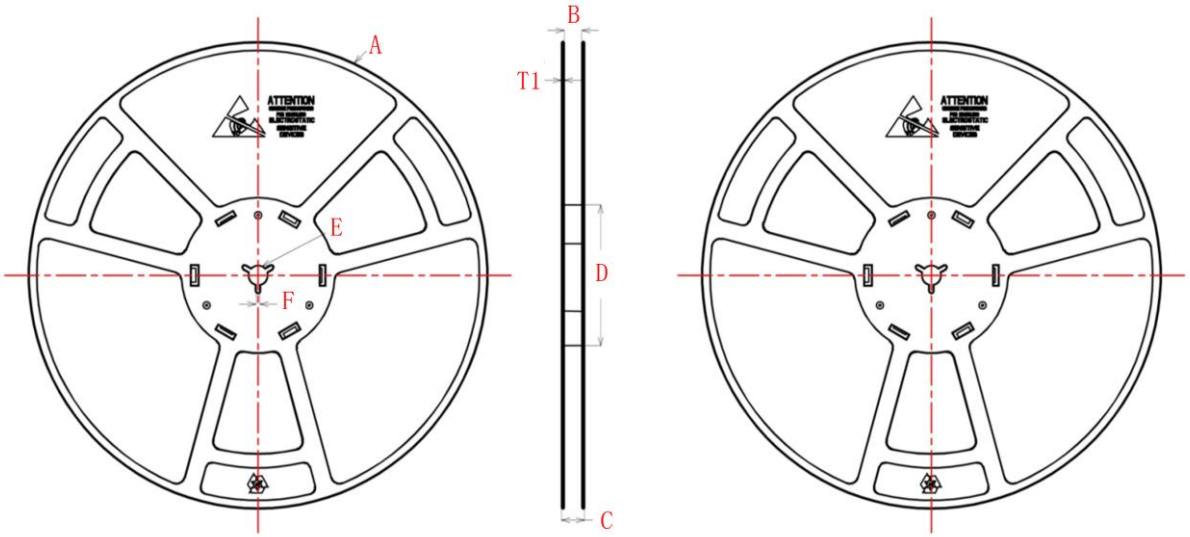
1) All dimensions are in millimeters.

TAPE AND REEL INFORMATION

TAPE DIMENSIONS:



REEL DIMENSIONS:



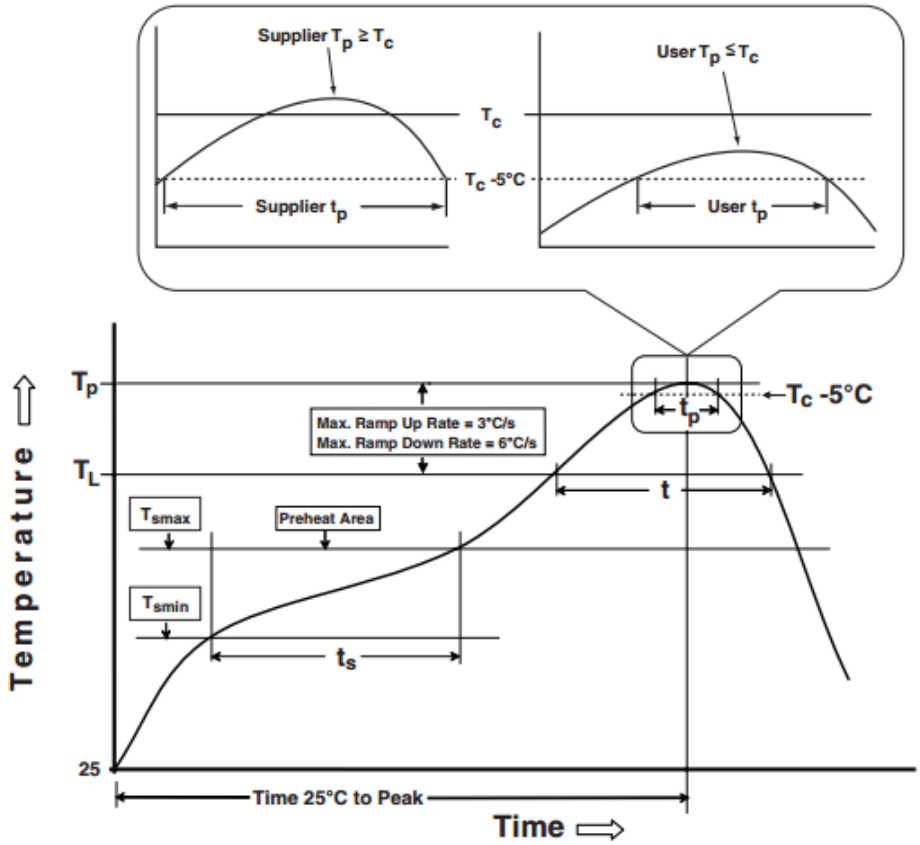
Unit: mm

A	B	C	D	E	F	T1
Ø 330±1.0	$12.4^{+1.0}_{-0.0}$	$17.6^{+1.0}_{-0.0}$	Ø 100.0±0.5	Ø 13.0±0.2	1.9±0.4	1.9±0.2

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 4000
3) MSL level is level 3.

RECOMMENDED REFLOW SOLDERING TEMPERATURE PROFILE



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	235 °C	260 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		