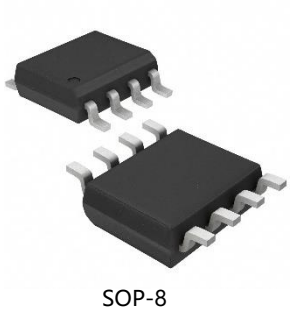
HX37323-S/HX27323-S
Dual channel 2A ultra high speed power switch drive

HX37323-S/HX27323-S is a power switch driver. It has a matching rise and fall Time is used to charge and discharge the gate of the power switch. Under any conditions within the rated power and voltage range, HX37323-S/ HX27323-S has high latch resistance capability. Even if there is a noise spike of up to 5V (of any polarity) on the ground pin, HX37323-S/HX27323-S will not be damaged. It can withstand reverse currents of up to 500mA without causing damage or logical confusion. In addition, all terminals of HX37323-S/ HX27323-S are fully protected by electrostatic discharge (ESD) up to 2.0kV.



SOP-8

Device Information		
Part Number	**Encapsulation**	**Classification**
HX37323-S	SOIC8	Consumer category
HX27323-S	SOIC8	Industry

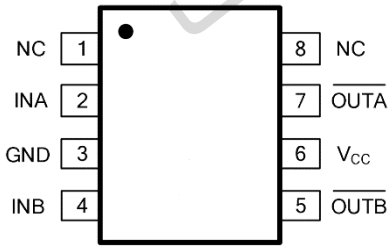
Peculiarity

- Latch protection: can withstand reverse current of 0.5A
- Input logic protection: capable of protecting input signals as low as -10V
- Low output imped ance
- Single chip integrated dual driver
- Peak output current: 2A
- Scope of work: 4.5V~25V
- The maximum input negative pressure can reach -5V
- High capacitance load driving capability: Under a 1nF load, the switching time is less than 25ns, and the rise/fall time is matched
- Propagation delay: 40ns
- Wide temperature range: -40 ℃~125 ℃
- Chip on/off delay characteristics: Ton/Off=70ns/70ns
- Compliant with RoSH standards
- Package type: SOIC8/DFN8

Apply

- Switching power supply, switching converter
- line driver
- Pulse Transformer Drive
- Drive MOSFETs and IGBTs
- motor control
- pulse generator
- power switch
- DC-DC conventer
- Class D switching amplifier

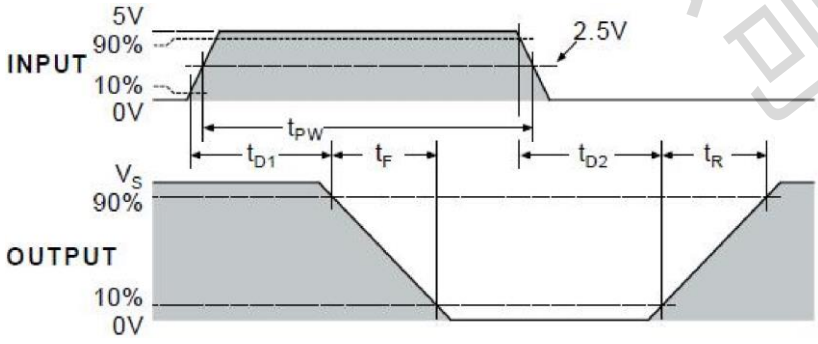
Chip Pin Descr Iption		
NUMBER	**NAME**	FUNCTION
1	NC	Empty pin
2	INA	**Channel A input terminal**
3	GND	**Pin ground**
4	INB	**Channel B input terminal**
5	$\overline{OUTB}$	Channel B output
6	V_{CC}	powe supply
7	$\overline{OUTA}$	Channel A output
8	NC	Empty pin



Product Specification				
SYMBOL	DEFINITION	MIN	MAX	UNIT
V_{CC}	Supply voltage		25	V
V_{IN}	Logic input voltage(INA/INB)	-10	V_{CC}+0.3	
ESD Rating				
E_{SD}	Human body discharge mode		2000	V
	Machine discharge mode		500	
Rated Power				
P_D	SOIC Package power (TA ≤70°C)		470	mW
Caloric Information				
T_J	Junction temperature		+150	°C
T_S	Storage temperature	-45	+150	
Recommended Scope of Work				
V_{CC}	Supply voltage	4.5	20	V
T_C	Ambient temperature	-40	125	°C

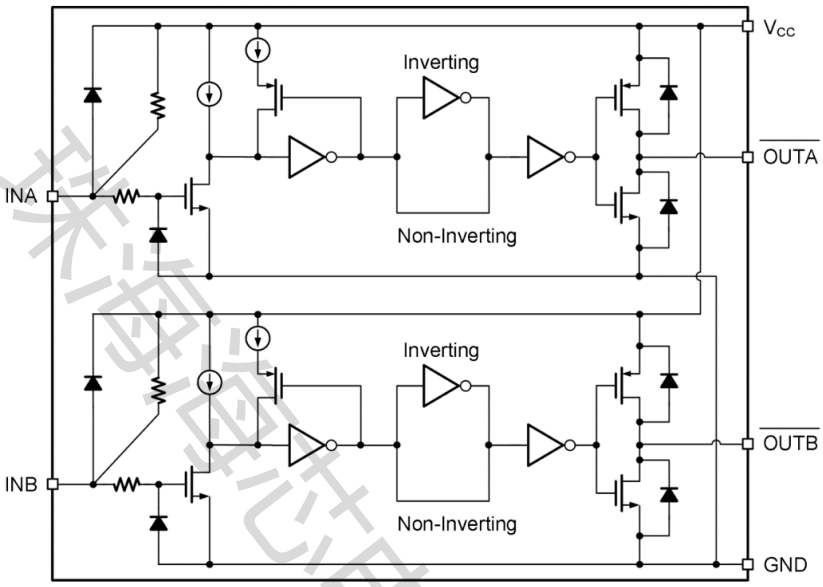
Electrical characteristics without special instructions TA= 25℃, 4.5V ≤VCC≤18V					
SYMBOL	DEFINITION	MIN	TYP	MAX	UNIT
V_{IH}	Logic High level "1" input voltage	2.4			V
V_{IL}	Logic Low "0" input voltage			0.8	V
I_{IN}	Input current(0V≤V_{IN}≤V_{CC})			200	μA
V_{OH}	High level output voltage drop	V_{CC}–0.025			V
V_{OL}	Low output voltage drop			0.025	V
R_{OH}	High level state, output resistance(V_{CC}=18V,I_O=100mA)		4	8	Ω
R_{OL}	Low level state, output resistance(V_{CC}=18V,I_O=100mA)		2	4	Ω
I_{PK}	Peak output current		2		A
I_{REV}	Latch protection withstands reverse current (Working cycle≤2%,t≤300us,V_{CC}=18V)		>0.5		A
t_R	Rise time(V_{CC}=18V,C_{LOAD}=100pF)			30	ns
t_F	Descent time(V_{CC}=18V,C_{LOAD}=100pF)			30	ns
t_{ON}	Open transmission delay(V_{CC} =18V,C_{LOAD}=100pF)			70	ns
t_{OFF}	Turn off the transmission delay(V_{CC}=18V,C_{LOAD}=100pF)			70	ns
I_{Q1}	Supply current(V_{INA}=V_{INB}=High logic)			1	mA
I_{Q0}	Supply current(V_{INA}=V_{INB}=Low logic)			1	mA

Input/output (inverted) waveform diagram



Explain

Functional Block Diagram



Chip working logic

The signal input ports (INA, INB) of HX37323-S/HX27323-S adopt a level triggered mode, which means that when the voltage value meets the logic requirements, the chip will work normally, as shown in the table.

Input-output logic table

INPUT		OUTPUT	
INA	INB	OUTA/	OUTB/
L	L	H	H
H	H	L	L
L	H	H	L
H	L	L	H
Note: H represents high level; L represents low level			

Signal input port

HX37323-S/HX27323-S contains two independent signal input ports for receiving control signals sent by the main control, and there will be no mutual interference between these two ports. These two port designs have high reliability and will not cause damage or logical confusion even when subjected to a reverse current of 500mA. The signal input port can directly handle a voltage of -10V, and even in high noise environments, the chip can still operate safely, improving stability. It is not recommended to adjust the output waveform by adjusting the slope or delay of the input port waveform. If it is necessary to adjust the rise and fall time of the power end, it is recommended to add additional resistors between the output end and the power end. The signal input port of HX37323-S/HX27323-S has a pull-up resistor to VCC. It is recommended to short-circuit this port to VCC when not in use.

Output port

The output and input of HX37323-S/HX27323-S are reversed and can be used to drive P-type or N-type MOSFETs. Each output port can provide a peak pull-up or pull-down current of 2A, which is suitable for driving MOSFET designs in high-frequency applications due to its high-speed and high current characteristics.

Application Information

The high-speed, high-current characteristics of the HX37323-S/HX27323-S are suitable for applications such as high-frequency power supplies. Typical applications include using a high-power driver chip to drive the gate voltage of the MOSFET when the PWM output level of the main control IC is not sufficient to drive the power end MOSFET, in order to ensure that the MOSFET is in a stable state.

In the high frequency and high power application environment, it is very important to ensure the stable operation of the chip. Therefore, the following recommendations are made when applying HX37323-S/HX27 323-S:

1. During the switching process, HX37323-S/HX27323-S outputs a peak switching current of 2A. As frequency increases, VCC stability may decrease. To stabilize VCC voltage, select a larger electrolytic capacitor during design and use low ESR/ESL capacitors (like ceramic or patch capacitors) in parallel to address high-frequency characteristics address high-frequency characteristics. Position the capacitor as close as possible to the VCC and GND pins.
2. The output port is part of the power loop; therefore, to ensure a flat output waveform, place it near the MOSFET on the power grid during design. Additionally, consider adding external resistors at OUT for smoother operating waveforms.

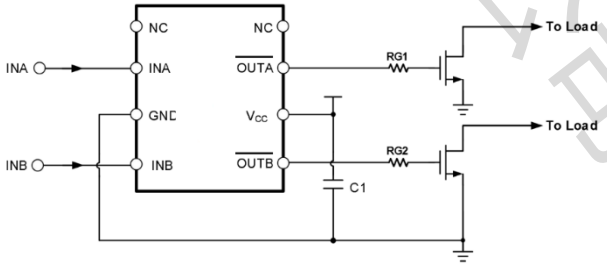
When achieving the best performance from high speed low side door drives, the following points need to be noted:

1. Connect the low ESR/ESL capacitor tightly between the VCC and GND pins of the IC to support the peak current drawn from the VDD when the MOSFET is on Time.
2. Grounding considerations:

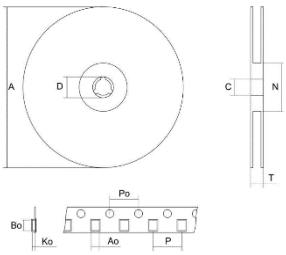
-The primary goal of designing grounding connections is to limit the MOSFET gate charging and discharging circuit to the smallest possible loop area, in order to reduce loop inductance and effectively avoid noise issues on the MOSFET gate. Meanwhile, the gate driver chip should be as close as possible to the MOSFET.
-Star point grounding is a good method to reduce noise coupling between current circuits. Connect the ground point of the driver to other circuit nodes such as the source of the power MOSFET and the ground of the PWM controller. The connection path should be as short as possible to reduce inductance and as wide as possible to reduce resistance.
-Use ground plane to shield noise. Due to the rapid rise and fall time of OUT, which may disrupt the input signal during the transition period, shielding noise through the ground plane can ensure that the input signal is not disturbed. The ground plane cannot become a conduction path for any current circuit, and the ground plane must establish a ground potential connection with the star point. In addition to shielding noise, the grounding plane can also help dissipate heat.

3. In a noisy environment, to prevent noise from causing output failures, you can connect unused pins to VDD or GND.
4. Separate the power loop from the signal loop, such as output and input signals.

Inverting typical application circuit diagram



Package



Packing Method	Quantity
Tape and Reel	2500PCS/ Disk