

MSQ100N03D

Dual N-Channel 100-V (D-S) MOSFET

Description

The device is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- $R_{DS(ON)} = 152m\Omega @ V_{GS} = 10V$
- Fast switching
- Improve dv/dt Capability
- 100% EAS Guaranteed
- Green Device Available

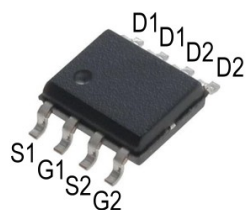
Typical Applications

- Networking
- Load Switch
- LED Applications

Package type : SOP-8

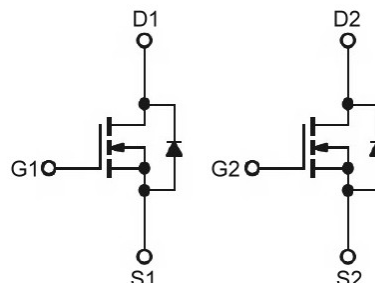
Packing & Order Information

3,000/Reel

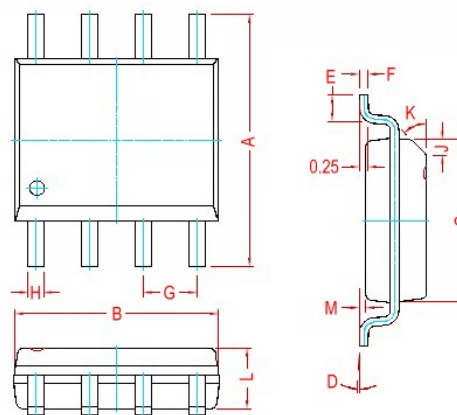


RoHS Compliant

Graphic Symbol

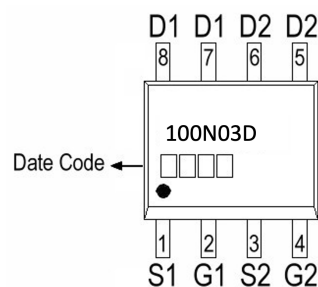


Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.51
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.40 Ref.	
E	0.40	0.90	K	45° Ref.	
F	0.19	0.26	G	1.27 Typ.	

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings			
Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ¹ ($T_A = 25^\circ\text{C}$)	2.3	A
	Continuous Drain Current ¹ ($T_A = 70^\circ\text{C}$)	2.1	A
I_{DM}	Pulsed Drain Current ^{1,2}	13.2	A
I_{AS}	Single Pulse Avalanche Current, $L = 0.1\text{mH}^3$	5	A
E_{AS}	Single Pulse Avalanche Energy, $L = 0.1\text{mH}^3$	1.3	mJ
P_D	Power Dissipation ⁴ ($T_A = 25^\circ\text{C}$)	2.5	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Resistance Ratings			
Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ¹	85	$^\circ\text{C/W}$
	Maximum Junction-to-Ambient ¹ ($t \leq 10\text{s}$)	50	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1.0	1.7	2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	100	-	-	V
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS} = 10\text{V}$, $I_D = 2.0\text{A}$	-	130	152	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}$, $I_D = 1.0\text{A}$	-	135	158	
E_{AS}	Single Pulse Avalanche Energy ⁵	$V_{DD} = 25\text{V}$, $L = 0.1\text{mH}$, $I_{AS} = 1.5\text{A}$	0.11	-	-	mJ
V_{SD}	Diode Forward Voltage ²	$I_S = 1\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	-	0.74	1.2	V
I_S	Continuous Source Current ^{1,6}	$V_G = V_D = 0\text{V}$, Force Current	-	-	5	A
I_{SM}	Pulsed Source Current ^{2,6}		-	-	10	

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. The EAS data shows maximum rating. The test condition is $V_{DD} = 25\text{V}$, $V_{GS} = 10\text{V}$, $L = 0.1\text{mH}$, $I_{AS} = 5\text{A}$.
4. The power dissipation is limited by 150°C junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

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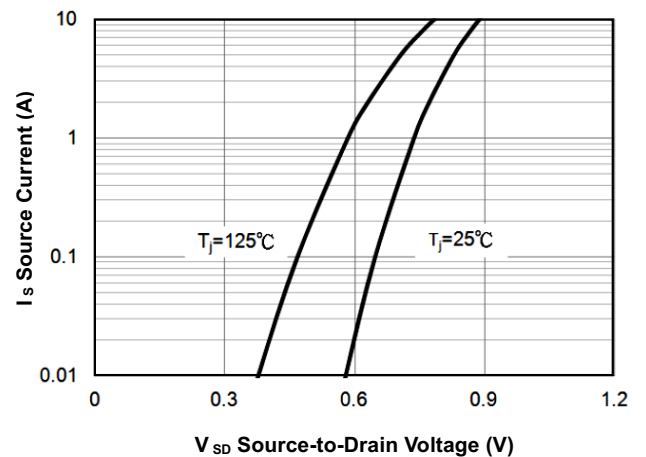
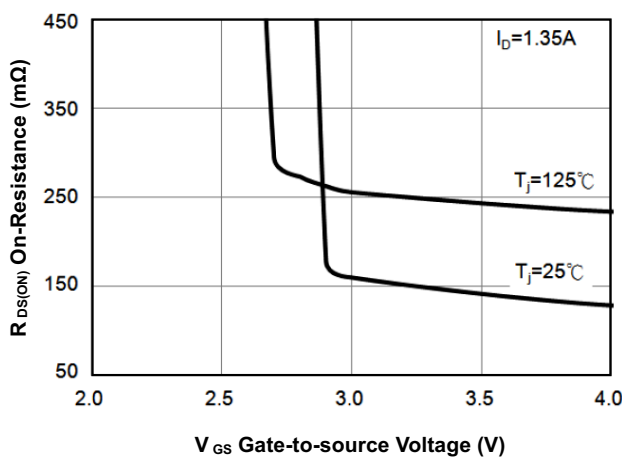
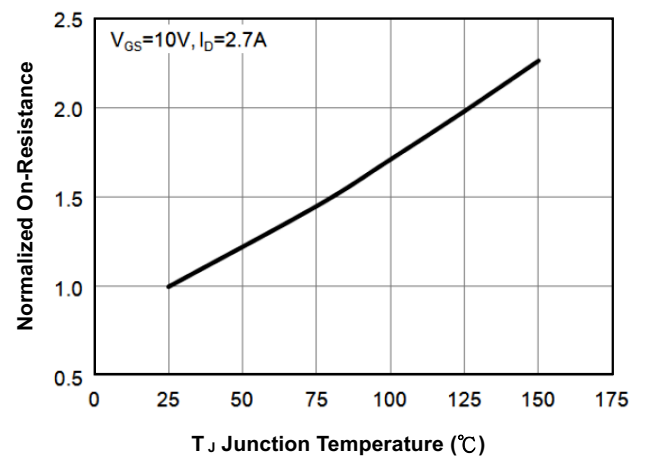
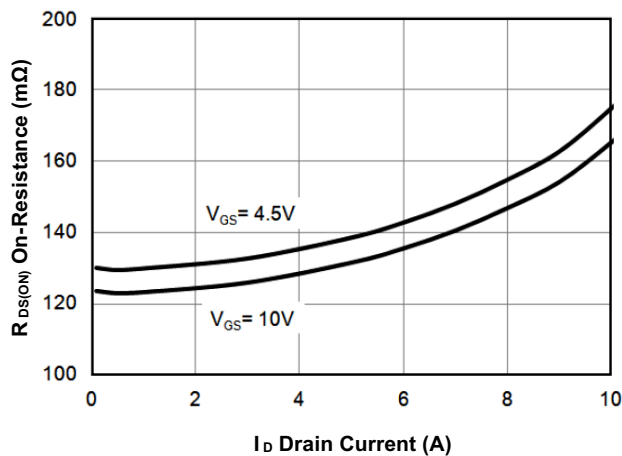
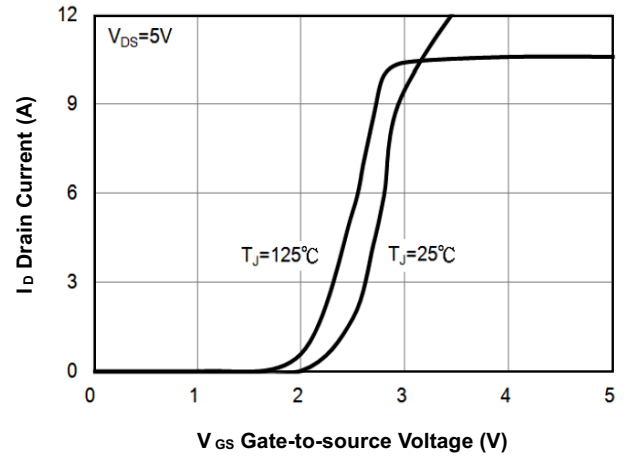
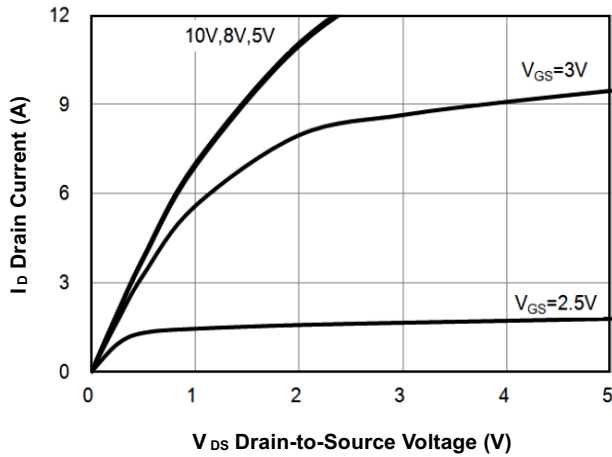
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Dynamic						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q_g	Total Gate Charge ²	$V_{DS} = 60V$ $I_D = 2.7A$ $V_{GS} = 10V$	--	19	--	nC
Q_{gs}	Gate-Source Charge		--	2.9	--	
Q_{gd}	Gate-Drain Charge		--	3.2	--	
$t_{d(on)}$	Turn-On Delay Time ²	$V_{DS} = 50V$ $V_{GS} = 10V$ $R_G = 6\Omega$ $R_L = 18.5\Omega$	--	6.1	--	ns
t_r	Rise Time		--	27	--	
$t_{d(off)}$	Turn-Off Delay Time		--	28	--	
t_f	Fall Time		--	11	--	
C_{ISS}	Input Capacitance	$V_{DS} = 25V$ $V_{GS} = 0V$ $f = 1.0MHz$	--	1021	--	pF
C_{OSS}	Output Capacitance		--	38	--	
C_{RSS}	Reverse Transfer Capacitance		--	17	--	

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• Typical Electrical Characteristics



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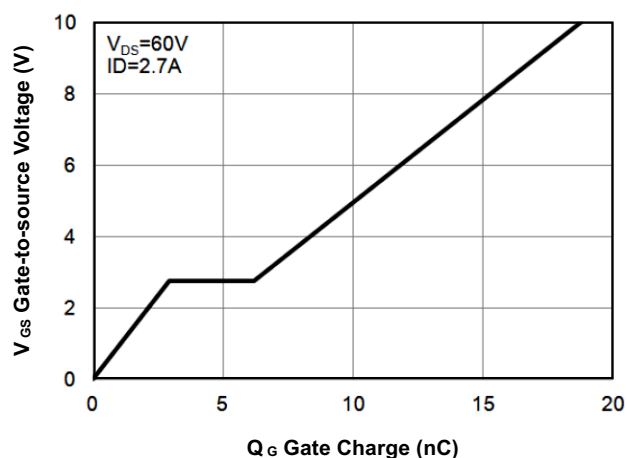


FIG.7-Gate Charge Characteristics

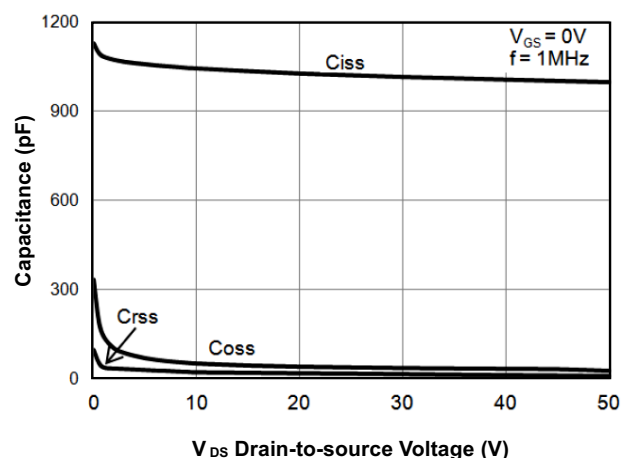


FIG.8-Capacitance Characteristics

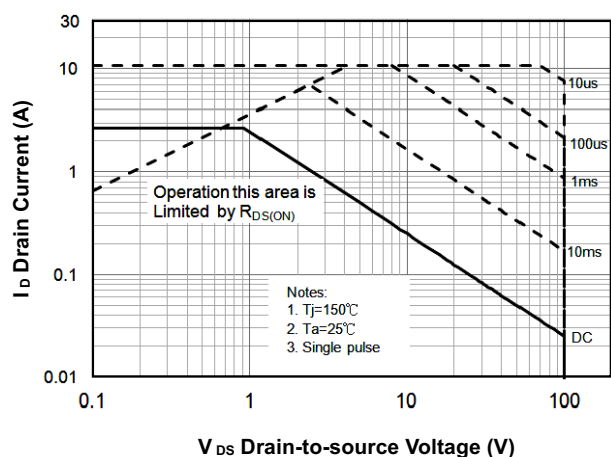


FIG.9-Safe Operating Area

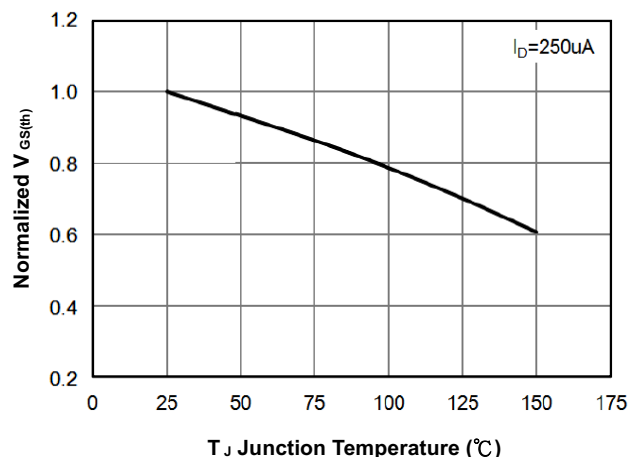


FIG.10-Normalized $V_{GS(th)}$ vs. T_J

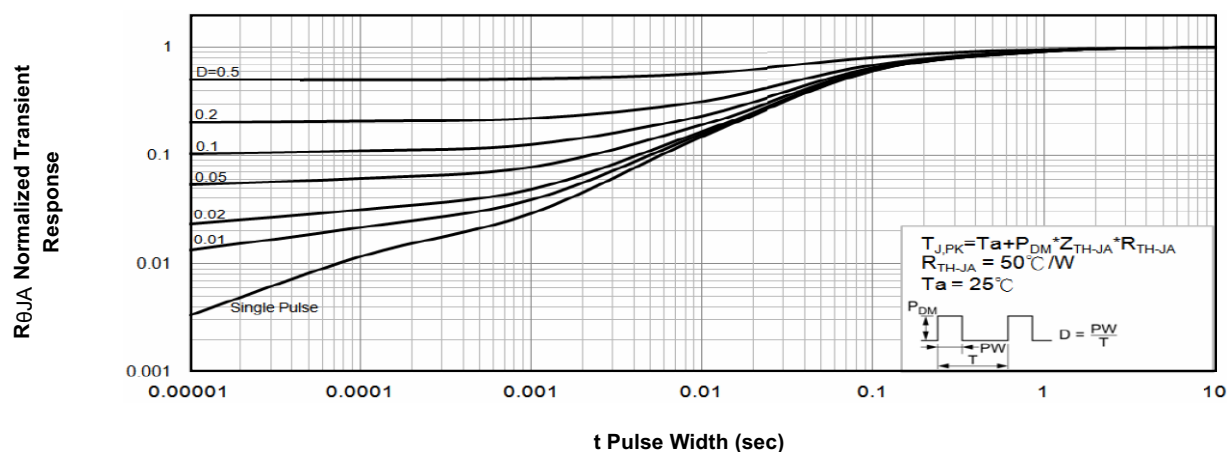


FIG.11-Normalized Maximum Transient Thermal Impedance

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