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Nyfea product specification

PRODUCT SPECIFICATION

产品规格书

Customer 客户名称： _____

Product Name品名： Real Time Clock

PART NO. 型号规格： FRTC1337S

Issue Date发布日期： _____

Prepared 制作	Checked 审核	Customer Check客户核准
ChenTT	Zelig	

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Features

- Using external 32.768kHz quartz crystal
- Supports I2C-Bus high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Operating range:1.8V to 5.5V

Description

The FRTC1337S serial real-time clock is a low -power clock/
calendar with two programmable time-of-day alarms and a programmable square- wave output.

Address and data are transferred serially via a 2-wire bidirectional bus.The clock/calendar provides seconds,minutes,hours,day,date,month, and year information.The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

Applications

- Portable instruments
- Electronic metering
- Telecom equipments

Ordering Information

Ordering Code	Package	Description
FRTC1337S	SOP8	pitch 1.27mm

Pb-free and Gree

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Function Block

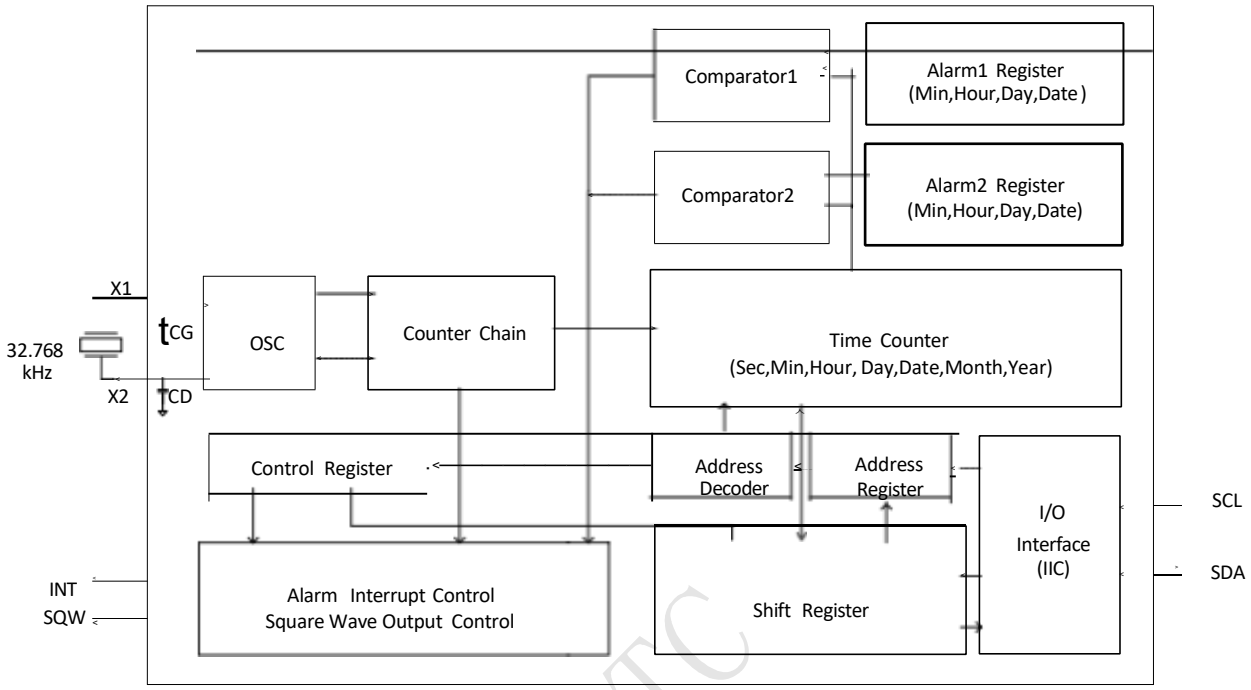

Figure1 Function Block

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Pin Configuration

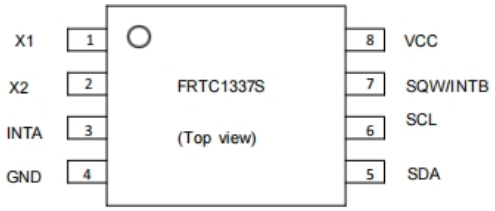

Figure2 Pin Configuration

Pin No	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them. Or external clock input.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768 kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the IIC serial interface.
5	SDA	I/O	**Serial Data Input/ Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
3	INTA	O	**Interrupt Output.** When enabled, INTA is asserted low when the time matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull up resistor.
7	SQW/INTB	O	**Square-Wave/ Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor.
8	VCC	P	**Power.**
4	GND	P	**Ground.**

Typical Application Circuit

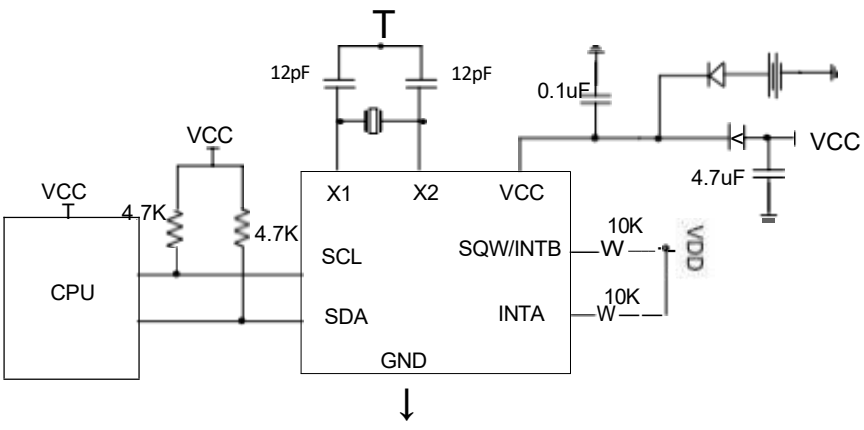

Figure3 Typical Application Circuit

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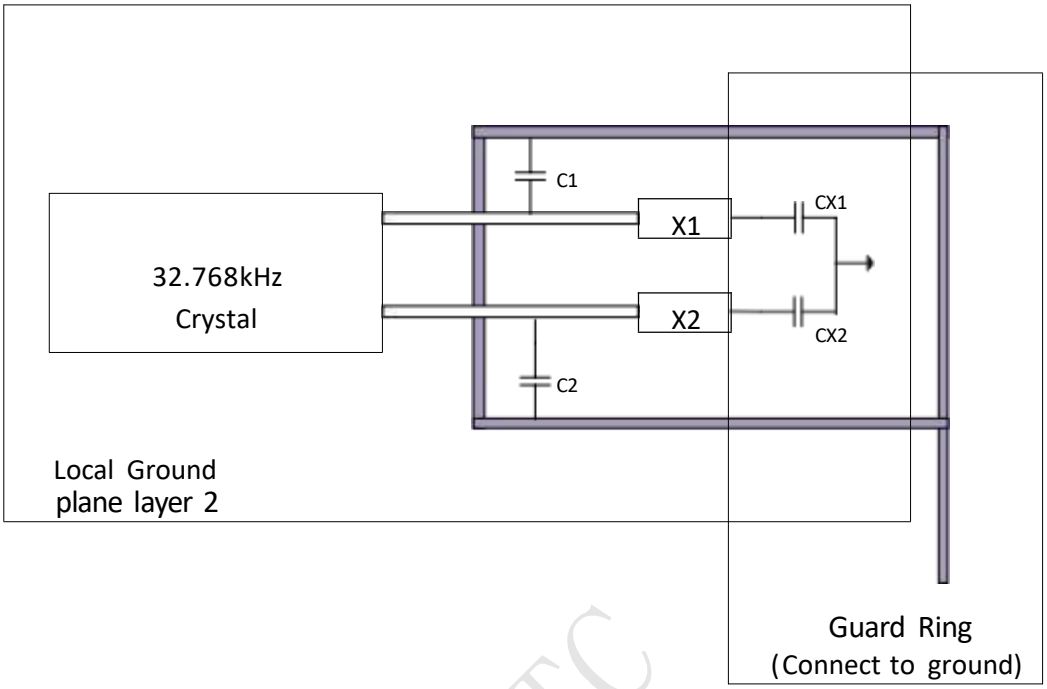
Recommended Layout for Crystal



Parameter	Symbol	MIN	TYP	MAX	Unit
Nominal Frequency	fo	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C 1(Optional)	0	-	15	pF
Load Capacitance	C2(Optional)	0	-	15	pF
Build- in Cap	CX1 , CX2	-	12	-	pF

Note:
The crystal, traces and crystal input pins should be isolated from RF generating signals.

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Function Description

Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100 .

Alarm function

This device has two alarm system (Alarm 1 and Alarm 2) that outputs interrupt signals from INTA or INTB to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8. 192k, 32.768k Hz.

Interface with CPU

Data is read and written via the I2C bus interface using two signal lines: SCL (clock) and SDA (data). Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz,which supports the I2C bus's high-speed mode.

Oscillator fail detect

When oscillator fail, FRTC1337S OSF bit will be set.

Oscillator enable/ disable

Oscillator and time count chain can be enabled or disabled at the same time by /ETIME bit.

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Registers

Addr. (hex)*1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01- 12)	Century	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Alarm 1: Seconds	A1M1*2	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2*2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3*2	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4*2	Day, / Date	0, D20	0, D10	0, D8	W4 , D4	W2 , D2	W1 , D1
0B	Alarm 2: Minutes	A2M2*3	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3*3	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4*3	Day, / Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/ETIME*4	0	0	RS2*5	RS1 *5	INTCN*6	A2IE*7	A1IE*7
0F	Status	OSF*9	0	0	0	0	0	A2F*8	A1F*8

Note:

*1. FRTC1337S uses 8 bits for address. For excess 0FH address, 1337S will not respond (no acknowledge signal was given)

*2. Alarm 1 mask bits. Select alarm repeated rate when an alarm occurs.

*3. Alarm 2 mask bits. Select alarm repeated rate when an alarm occurs.

*4. Oscillator and time count chain enable/disable bit.

*5. Square wave output frequency select.

*6. Interrupt output pin select bit.

*7. Alarm 1 and alarm 2 enable bits.

*8. Alarm 1 and alarm 2 flag bits.

*9. Oscillator stop flag.

*10. All bits marked with "0" are read-only bits. Their value when read is always "0".

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Control and status register

Addr (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
0E	Control	/ ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
	(default)	0	0	0	1	1	0	0	0
0F	Status	OSF	0	0	0	0	0	A2F	A1F
	(default)	1	0	0	0	0	0	-	-

Oscillator related bits

●/ ETIME

Enable oscillator and time count chain bit.

/ ETIME	Data	Description	
Read / Write	0	Enable oscillator and time count chain.	Default
	1	Disable oscillator and time count chain.	

● OSF

Oscillator Stop Flag.

A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC is insufficient to support oscillation.
3) The /ETIME bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc).

This bit remains at logic 1 until written to logic 0.

Square wave frequency selection bits

● RS2, RS1

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

RS2, RS1	Data	SQW output freq. (Hz)	
Read / Write	00	1	
	01	4.096k	
	10	8. 192k	
	11	32.768k	Default

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Interrupt related bits

- **INTCN**

Interrupt Output pin select bit. This bit controls the relationship between the two alarms and the interrupt output pins.

INTCN	Data	Description	
Read / Write	1	A match between the timekeeping registers and the alarm 1 registers activates the $\overline{\text{INTA}}$ pin (if the alarm 1 is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/INTB pin (if the alarm 2 is enabled).	
	0	A match_between the timekeeping registers and either alarm 1 or alarm 2 registers activates the INTA pin (if the alarms are enabled) . In this configuration, a square wave is output on the SQW/ INTB pin.	Default

- **A1IE**

Alarm 1 Interrupt Enable.

A 1 IE	Data	Description	
Read / Write	0	The A1 F bit does not initiate the INTA signal.	Default
	1	Permits the alarm 1 flag (A1F) bit in the status register to assert INTA.	

- **A1F**

Alarm 1 Flag.

A1F	Data	Description	
Read / Write	0	The time do not match the alarm 1 registers.	Default
Read	1	Indicates that the time matched the alarm 1 registers. If the A1 IE bit is also logic 1, the INTA pin goes low. A1F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	

- **A2IE**

Alarm 2 Interrupt Enable.

A2 IE	Data	Description	
Read / Write	0	The A2 F bit does not initiate an interrupt signal.	Default
	1	Permits the alarm 2 flag (A2F) bit in the status register to assert INTA (when INTCN = 0) or to assert SQW/INTB (when INTCN = 1) .	

- **A2F**

Alarm 2 Flag.

A1F	Data	Description	
Read / Write	0	The time do not match the alarm 2 registers.	Default
Read	1	Indicates that the time matched the alarm 1 registers. This flag can be used to generate an interrupt on either INTA or SQW/INTB depending on the status of the INTCN bit. If the INTCN = 0 and A2F = 1(and A2IE = 1), the INTA pin goes low. If the INTCN = 1 and A2F = 1 (and A2IE = 1), the SQW/ INTB pin goes low. A2F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	

Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the / 12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
	(default)	0	-	-	-	-	-	-	-
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	-	-	-	-	-	-	-
02	Hours	0	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	-	-	-	-	-	-	-

Note:

Any registered imaginary time should be replaced with correct time, otherwise it will cause the clock counter malfunction.

12, /24 bit

This bit is used to select between 12-hour clock system and 24-hour clock system.

12, /24	Data	Description
Read / Write	0	24-hour mode
	1	12-hour mode

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12, /24	Description	Hours register
0	24-hour time display	
1	12-hour time display	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	52 (AM 12)	12	72 (PM 12)
01	41 (AM 01)	13	61 (PM 01)
02	42 (AM 02)	14	62 (PM 02)
03	43 (AM 03)	15	63 (PM 03)
04	44 (AM 04)	16	64 (PM 04)
05	45 (AM 05)	17	65 (PM 05)
06	46 (AM 06)	18	66 (PM 06)
07	47 (AM 07)	19	67 (PM 07)
08	48 (AM 08)	20	68 (PM 08)
09	49 (AM 09)	21	69 (PM 09)
10	50 (AM 10)	22	70 (PM 10)
11	51 (AM 11)	23	71 (PM 11)

Note:

This bit is used to select between 12-hour clock operation and 24-hour clock operation.
Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

Days of the week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e. , if 1 equals Sunday, then 2 equals Monday, and so on) . Illogical time and date entries result in - operation.

Addr (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	-	-	-

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Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	-	-	-	-	-	-
05	Months	Century*1	0	0	M10	M8	M4	M2	M1
	(default)	-	0	0	-	-	-	-	-
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	-	-	-	-	-	-	-	-

Note:
The century bit is toggled when the years register overflows from 99 to 00.

Alarm Register

Addr	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Alarm 1: Seconds	A1M1*1	S40	S20	S10	S8	S4	S2	S1
	(default)	-	-	-	-	-	-	-	-
08	Alarm 1: Minutes	A1M2*1	M40	M20	M10	M8	M4	M2	M1
	(default)	-	-	-	-	-	-	-	-
09	Alarm 1: Hours	A1M3*1	12, /24	H20 or P/A	H10	H8	H4	H2	H1
	(default)	-	-	-	-	-	-	-	-
0A	Alarm 1: Day, Date	A1M4*1	Day, * 1 /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	-	-	-	-	-	-	-	-
0B	Alarm 2: Minutes	A2M2*2	M40	M20	M10	M8	M4	M2	M1
	(default)	-	-	-	-	-	-	-	-
0C	Alarm 2: Hours	A2M3*2	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	-	-	-	-	-	-	-	-
0D	Alarm 2: Day, Date	A2M4*2	Day, / Date*2	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	-	-	-	-	-	-	-	-

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Note:

1、Alarm mask bit, using to select Alarm 1 alarm rate.

2、Alarm mask bit, using to select Alarm 2 alarm rate.

Alarm Function

Addr. (hex)	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
02	Hours	0	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
03	Days of the week	0	0	0	0	0	W4	W2	W1
04	Dates	0	0	D20	D10	D8	D4	D2	D1
07	Alarm 1: Seconds	A1M1	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4	Day, / Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4	Day, / Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/ ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
0F	Status	OSF	0	0	0	0	0	A2F	A1F

Note:

Alarm function does not support different hour system adopted in time and alarm register.

The FRTC1337S contains two time-of-day/date alarms.

The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits.

When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h ~ 04h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 and Table 3 shows the possible settings.

The Day, /Date bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 ~ 5 of that register reflects the day of the week or the date of the month. If the bit is

written to logic 0, the alarm is the result of a match with date of the month. If the bit is written to logic 1, the alarm is the result of a match with day of the week.

When the FRTC1337S register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output (INTA or SQW/INTB) signals. The
match is tested on the once-per-second update of the time and date registers.

Alarm 1 Mask Bits

Day, /Date	Alarm 1 register mask bits				Alarm rate
	A1M4	A1M3	A1M2	A1M1	
×	1	1	1	1	Alarm once per second
×	1	1	1	0	Alarm when seconds match
×	1	1	0	0	Alarm when minutes and seconds match
×	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
Others					Ignored.

Alarm 2 Mask Bits

Day, /Date	Alarm 2 register mask bits			Alarm rate
	A2M4	A2M3	A2M2	
×	1	1	1	Alarm once per minute (00 seconds of every minute)
×	1	1	0	Alarm when minutes match
×	1	0	0	Alarm when hours, minutes
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match
Others				Ignored.

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I2C Bus Interface

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be pulled up via pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain high.

Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

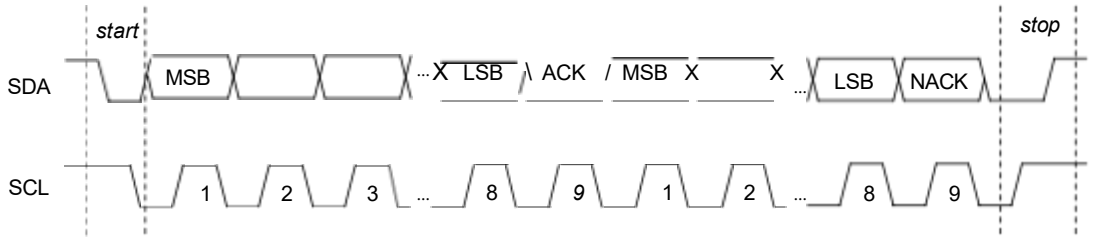
Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.



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Read mode

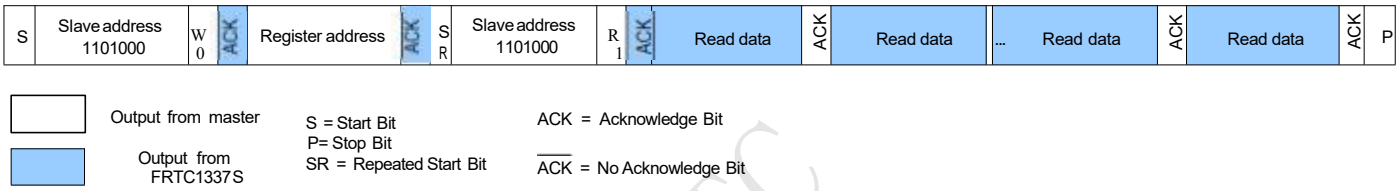
In this mode, the master reads the FRTC1337S slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W =

1). At this point, the

master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

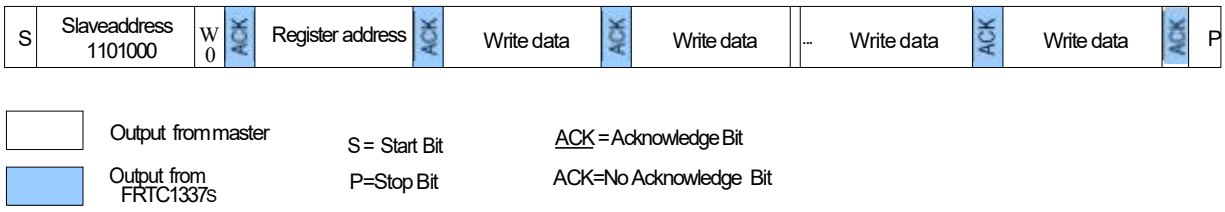
The FRTC1337S slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.



Write mode

In this mode the master transmitter transmits to the FRTC1337S slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The FRTC1337S slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.



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Maximum Ratings

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-40 °C to +125 °C
Supply Voltage to Ground Potential (Vcc to GND)	- 0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	- 0.3V to (Vcc+0.3V)
DC Output Voltage (SDA, /INT pins)	-0.3V to +6.5V
Power Dissipation	320mW (Depend on package

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Part No.	Symbol	Description		MIN	TYP	MAX	Unit
FRTC1337S	VCC	Power voltage		1.8	-	5.5	V
	VOSC	Oscillator voltage		1.7	-	5.5	
	VIH	Input high level	SCL, SDA	0.7VCC	-	VCC+0.3	
			INTA, SQW/ INTB	-	-	5.5	
	VIL	Input low level		-0.3	-	0.3VCC	
	TA	Operating temperature		-40	-	85	°C

DC Electrical Characteristics

Unless otherwise specified, VCC = 1.8~5.5V, TA = -40 °C to +85 °C

Sym.	Item	PIN	Condition	MIN	TYP	MAX	Unit
VCC	Supply voltage	VCC		1.8	-	5.5	V
VOSC	Oscillator voltage	VCC		1.7	-	5.5	V
ICC	Active supply current	VCC	Note 1, 5	-	-	150	μA
	Standby current	VCC	Note 2, 3, 5	-	0.5	0.8	
	Timekeeping current	VCC	Note 2, 4, 5	-	350	600	nA
	Data retention current	VCC	Note 2, 6	-	-	150	
VIL1	Low- level input voltage	SCL		-0.3	-	0.3VCC	V
VIH1	High- level input voltage	SCL		0.7VCC	-	VCC+0.3	
IOL	Low- level output current	SDA, /INTA, /INTB	VOL = 0.4V	-	-	3	mA
IIL	Input leakage current	SCL		-	-	1	μA
IOZ	Output current when OFF	SDA, INTA, INTB		-	-	1	μA

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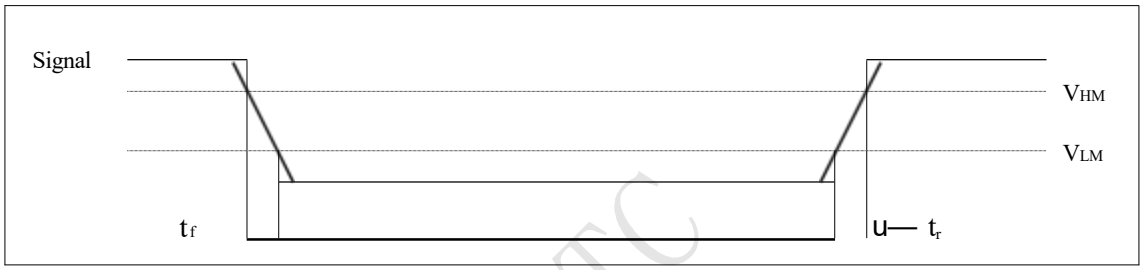
Note:

1. SCL clocking at max frequency = 400kHz, VIL = 0.0V, VIH = VCC.
2. Specified with 2-wire bus inactive, VIL = 0.0V, VIH = VCC.
3. SQW enabled.
4. Specified with the SQW function disabled by setting INTCN = 1.
5. Using recommended crystal on X1 and X2.
6. Crystal oscillator is disabled.

AC Electrical Characteristics

Sym	Description	Value	Unit
VHM	Rising and falling threshold voltage high	0.8 VCC	V
VHL	Rising and falling threshold voltage low	0.2 VCC	V



I2C AC Characteristics

Symbol	Item	MIN	TYP	MAX	Unit
fSCL	SCL clock frequency			400	kHz
tSU; STA	START condition set- up time	0.6			us
tHD; STA	START condition hold time	0.6			us
tSU; DAT	Data set-up time (RTC read/write)	200			ns
tHD;DAT1	Data hold time (RTC write)	35			ns
tHD;DAT2	Data hold time (RTC read)	0			us
tSU; STO	STOP condition setup time	0.6			us
tBUF	Bus idle time between a START and STOP condition	1.3			us
tLOW	When SCL = "L"	1.3			us
tHIGH	When SCL = "H"	0.6			us
tr	Rise time for SCL and SDA			0.3	us
tf	Fall time for SCL and SDA			0.3	us
tSP *	Allowable spike time on bus			50	ns
CB	Capacitance load for each bus line			400	pF

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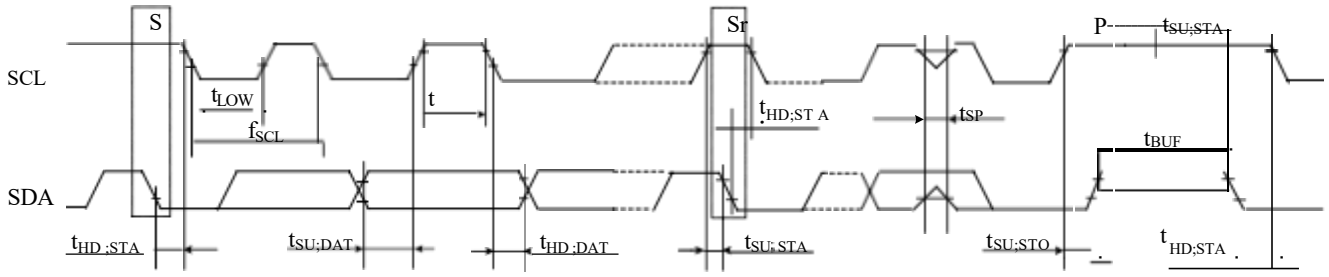

S: condition P: Stop condition SR: Restart condition

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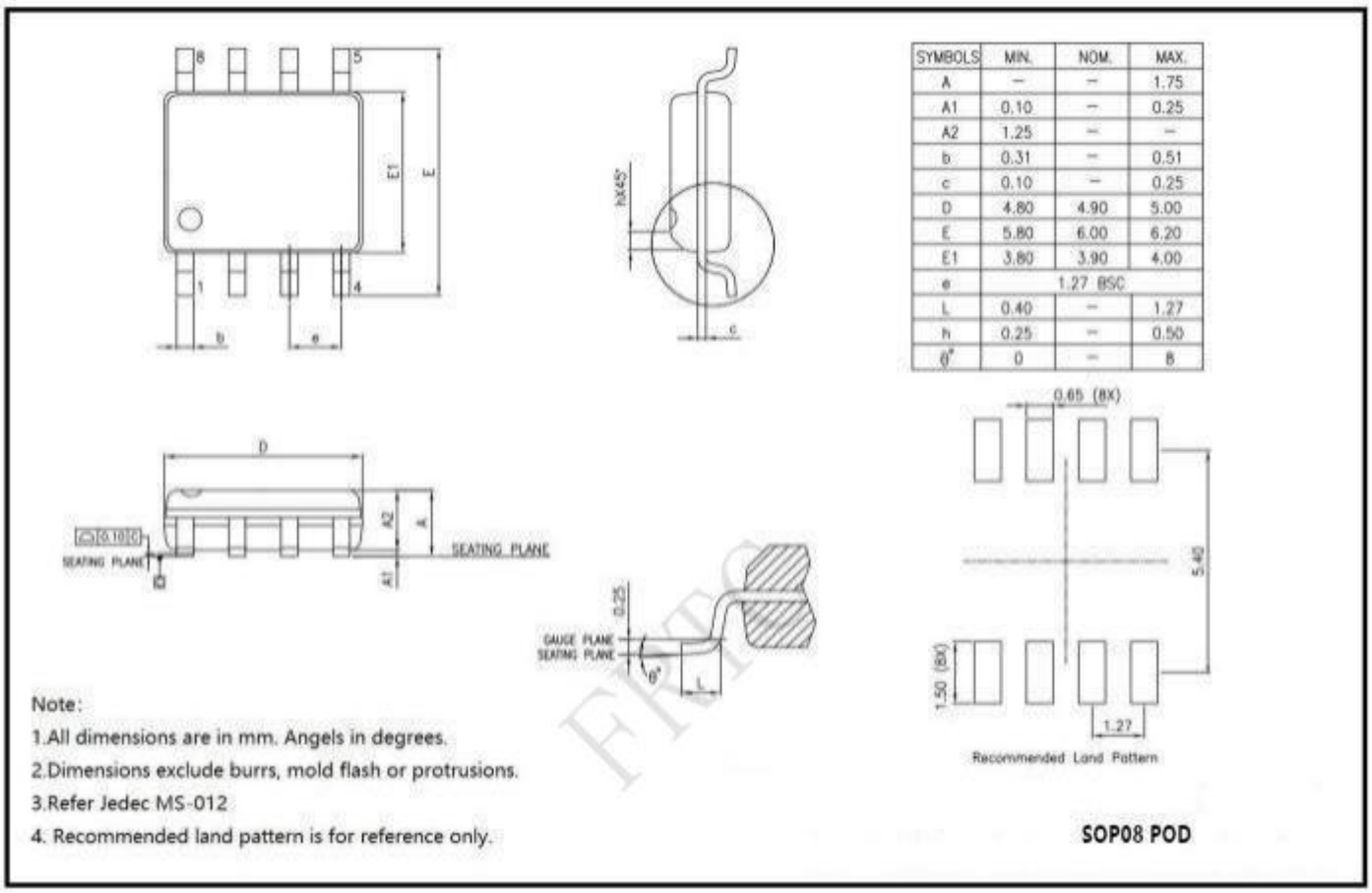
Package Information

FRTC1337S SOP8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

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Revision History

Revision	Description	Date
1.3		2024/11/1