1-MSPS/800-KSPS, ULTRA LOW POWER, 12-/10-/8-BIT, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Fast Throughput Rate:
  800 KSPS for CI7886/87/88
  1 MSPS for CI7886E
  1.25 MSPS for CI7887/88E
- Single 3.3V to 4.8V Supply Operation for CI7886E/87E/88E
  Single 4V to 5.25V Supply Operation for CI7886/87/88
- Zero Latency
- ±1.5LSB INL, ±1.25LSB DNL (CI7886)
- 20MHz Serial Interface(CI7886E/87E/88E)
- Variable Power Management
- Low Power (CI7886 typical):
  3.50mW (4V, 800KSPS)
  6.05mW (5V, 800KSPS)
- Second-Source for ADS7886/87/88
- 6-Pin SOT-23 Package

APPLICATIONS

- Base Band Converters in Radio Communication
- Optical Networking
- Optical Sensors
- Medical Instrumentations
- Battery-Powered Systems
- High-speed Closed-Loop Systems
- High-Speed Data Acquisition Systems

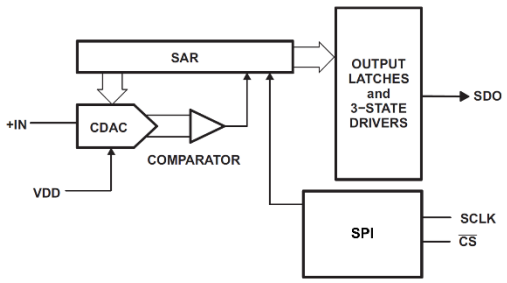


Figure 1. Functional Block Diagram

DESCRIPTION

The CI7886, CI7887, and CI7888 are, respectively, 12-bit, 10-bit, and 8-bit, high speed, low power, small size, successive approximation ADCs. These devices can operate from a single 4 V to 5.25 V supply with an 800 KSPS throughput (CI7886 /CI7887 /CI7888). When the parts operate from a single 3.3 V to 4.8 V power supply, the CI 7886E feature throughput rates up to 1 MSPS, the CI7887E/CI7888 E 1.25MSPS.

The CI7886/ CI7887/ CI7888 is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The C7886/ C7887/ C7888 is a drop-in replacement for the ADS7886/ADS7887/ADS7888 and consumes only half dynamic power of their counterpart.

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 1 MSPS and f_{SCLK} = 20 MHz if 3.3 V ≤ V_{DD} ≤ 4.8 V ; f_{SAMPLE} = 800 KSPS and f_{SCLK} = 16 MHz if 4 V ≤ V_{DD} ≤ 5.25 V . (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CI7886/86E			CI7887/87E			CI7888/88E			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			12			10			8		Bits
No missing codes		12			10			8			Bits
Integral linearity		-1.5		1.5	-1		1	-0.5		0.5	LSB
Differential linearity		-1.25		1.25	-0.75		0.75	-0.5		0.5	LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 16 MHz, 4 V ≤ V_{DD} ≤ 5.25 V			800			800			800	KSPS
	f_{SCLK} = 20 MHz, 3.3 V ≤ V_{DD} ≤ 4.8 V			1			1.25			1.25	MSPS
SNR	f_{IN} = 100 kHz		72.5			61.5			49.5		dB
THD	f_{IN} = 100 kHz		-84.5			-74.5			-68.5		dB

CI7886

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		0.87	0.95	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		1.21	1.31	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		0.48	0.55	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		0.88	0.98	
POWER DISSIPATION, CI7886						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		3.50	3.80	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		6.05	6.50	mW

CI7887

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		0.77	0.91	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		1.02	1.13	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		0.44	0.50	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		0.75	0.85	
POWER DISSIPATION, CI7887						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		3.10	3.65	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		5.10	5.65	mW

CI7888

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.70**	**0.82**	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**0.98**	**1.10**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.40**	**0.48**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.70**	**0.80**	
POWER DISSIPATION, XC7888						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**2.80**	**3.30**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**4.90**	**5.50**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

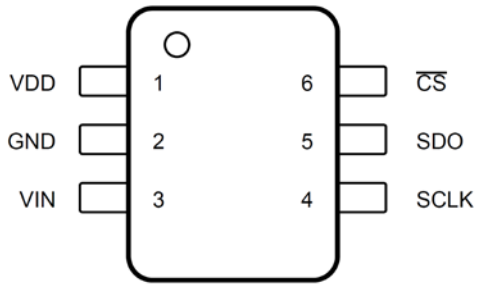


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
VDD	1	Power supply input also acts like a reference voltage to ADC.
GND	2	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	Analog signal input. This signal can range from 0 V to VDD.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDO	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the CI7886/87/88. The 5 V supply should come from a stable power supply such as an LDO. The supply to CI7886/87/88 should be decoupled to the ground. A 1-µF and a 10-nF decoupling capacitor are required between the VDD and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Always set the VDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

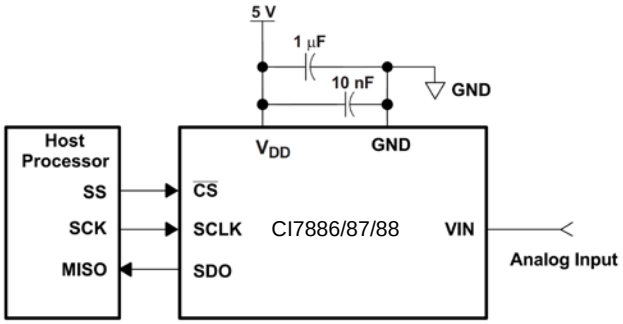


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

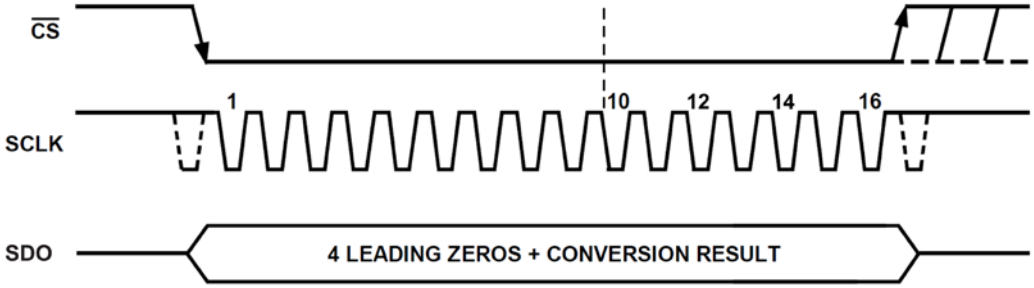


Figure 4. Timing Diagram

The conversion is initiated on the falling edge of $\overline{CS}$. The device outputs data while the conversion is in progress, and it requires 16/14/12 serial clock cycles to complete the conversion and access the full results. The CI7886/CI7887/CI7888 data word contains 4 leading zeros, followed by 12-bit/10-bit/8-bit data in MSB first format.

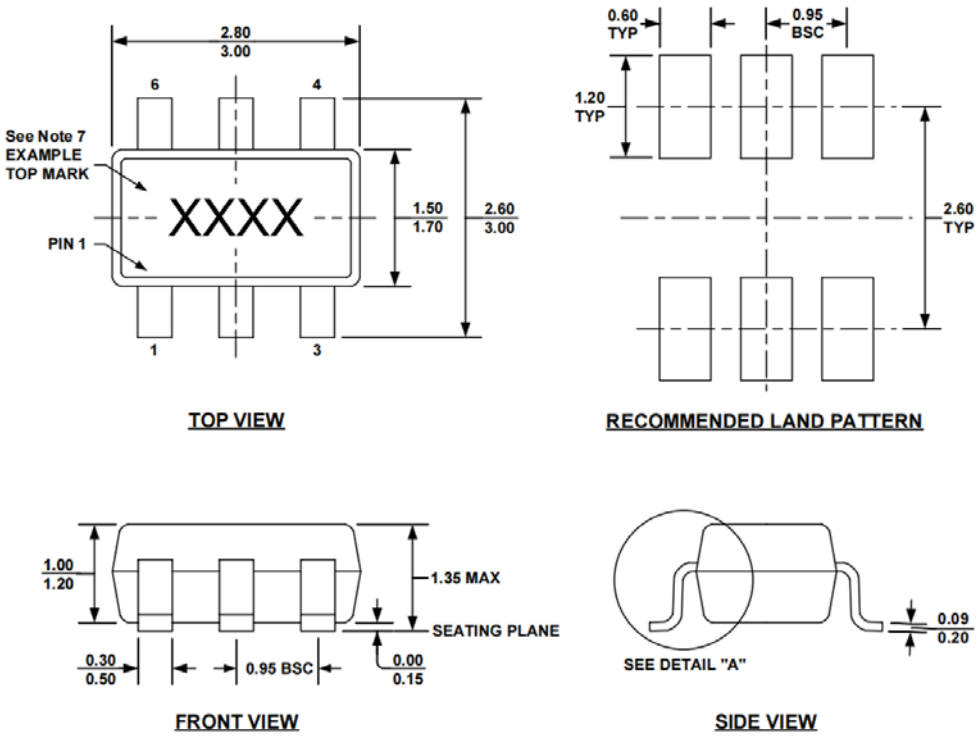
Once a data transfer is complete, SDO will return to the tri-state mode, and another conversion can be initiated after the quiet time has elapsed by again bringing $\overline{CS}$ low.

POWER-DOWN MODE

The CI7886/87/88 family has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion which is the 16th falling edge of SCLK for the CI7886 (the 14th and 12th for the CI7887 and CI7888, respectively). The device enters power down mode if $\overline{CS}$ goes high before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

OUTLINE DIMENTIONS



NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.