500 to 1000 KSPS, ULTRA LOW POWER, 12-/10-/8-BIT SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Single 4V to 5.25V Supply Operation for CI12/10/081S101
  Single 3.3V to 4.8V Supply Operation for CI12/10/081S101E
- Throughput Rate:
  500 to 800 KSPS for CI12/10/081S101
  800 to 1000 KSPS for CI12/10/081S101E
- Specified Over a Range of Sample Rates
- ±1.25LSB INL, ±1LSB DNL (CI121S101)
- Zero Latency
- SPI/DSP/MICROWIRE™/QSPI™ Compatible Serial Interface
- Variable Power Management
- Low Power (CI121S101 typical):
  3.60mW (4V, 800 KSPS)
  6.05mW (5V, 800 KSPS)
- Second-Source for ADC121S101-/ADC101S101/ADC081S101
- 6-Pin SOT-23 Package

APPLICATIONS

- Battery Powered Systems
- Base Band Converters in Radio Communication
- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems

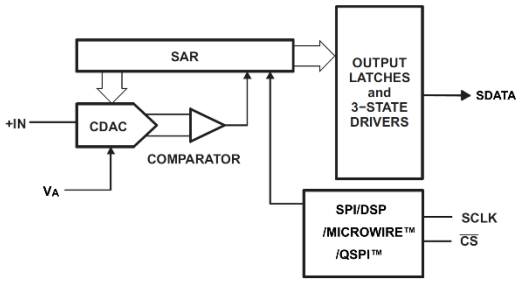


Figure 1. Functional Block Diagram

DESCRIPTION

The CI121S101 /CI101S101/CI081S101 is an ultra-low power, small size, single-channel 12-bit/10-bit/8-bit analog-to-digital converter with a high speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the CI121S101/CI101S101/CI081S101 is fully specified over a sample rate range of 500 KSPS to 800 KSPS from a single 4 V to 5.25 V supply, while the CI121S101E/CI101S101E/CI081S101E is ful ly specified over a sample rate range of 800 KSPS to 1 MSPS from a single 3.3 V to 4.8 V supply. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit.

The CI121S101 /CI101S101/CI081S101 is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The CI121S101/CI101S101/CI081S101 is a drop-in replacement for the ADC121S101/ADC101S101 /ADC081S101 and consumes only half dynamic power of their counterpart.

Pin-Compatible Alternatives by Resolution and Speed

Resolution	Specified for Sample Rate Range of:			
	50 to 200 KSPS	200 to 500 KSPS	500 to 800 KSPS	800 to 1000 KSPS
12-bit	CI121S021	CI121S051	**CI121S101**	**CI121S101E**
10-bit	CI101S021	CI101S051	**CI101S101**	**CI101S101E**
8-bit	CI081S021	CI081S051	**CI081S101**	**CI081S101E**

SPECIFICATIONS

At -40°C to 85°C, f_{SAMPLE} = 800 KSPS and f_{SCLK} = 16 MHz if 4 V ≤ V_{DD} ≤ 5.25 V ; f_{SAMPLE} = 1 MSPS and f_{SCLK} = 20 MHz if 3.3 V ≤ V_{DD} ≤ 4.8 V . (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CI121S101/E			CI101S101/E			CI081S101/E			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			**12**			**10**			**8**		Bits
No missing codes		**12**			**10**			**8**			Bits
Integral linearity		**-1.25**		**1.25**	**-1**		**1**	**-0.5**		**0.5**	LSB
Differential linearity		**-1**		**1**	**-1**		**1**	**-0.5**		**0.5**	LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 16 MHz, 4 V ≤ V_{DD} ≤ 5.25 V	**500**		**800**	**500**		**800**	**500**		**800**	KSPS
	f_{SCLK} = 20 MHz, 3.3 V ≤ V_{DD} ≤ 4.8 V	**800**		**1000**	**800**		**1000**	**800**		**1000**	KSPS
SNR	f_{IN} = 100 kHz		**72.5**			**61**			**49**		dB
THD	f_{IN} = 100 kHz		**-81**			**-78**			**-68**		dB

CI121S101

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.90**	**0.99**	mA
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**1.21**	**1.35**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.50**	**0.58**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.80**	**0.90**	
POWER DISSIPATION, CI121S101						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**3.60**	**3.95**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**6.05**	**6.75**	mW

CI101S101

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.80**	**0.95**	mA
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**1.02**	**1.22**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.55**	**0.60**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.70**	**0.80**	
POWER DISSIPATION, CI101S101						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**3.18**	**3.80**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**5.09**	**6.10**	mW

CI081S101

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.74**	**0.88**	mA
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**1.02**	**1.25**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.45**	**0.45**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.75**	**0.90**	
POWER DISSIPATION, CI081S101						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**2.95**	**3.55**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**5.10**	**6.25**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

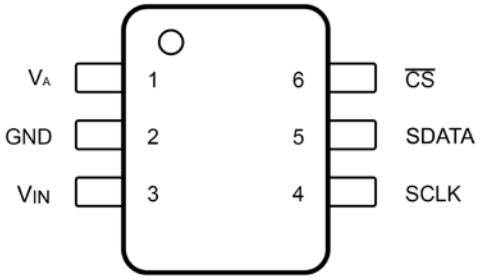


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_A	1	Power supply input.
GND	2	Ground for power supply, all analog and digital signals are referred with respect to this pin.
V_{IN}	3	Analog input. This signal can range from 0 V to V_A.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDATA	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the CI121S101/CI101S101/CI081S101 . The 5 V supply should come from a stable power supply such as an LDO. The supply to CI121S101 /CI101S101/CI081S101 should be decoupled to the ground. A 1-µF and a 10-nF decoupling capacitor are required between the V_A and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Always set the V_A supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

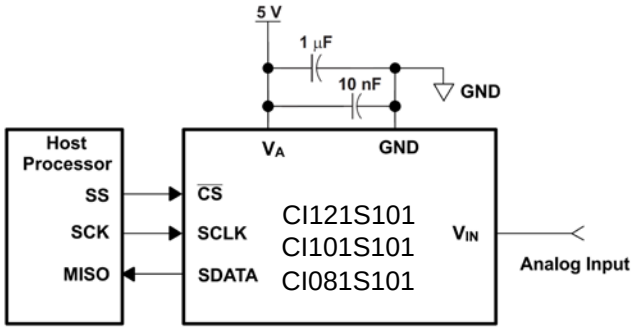
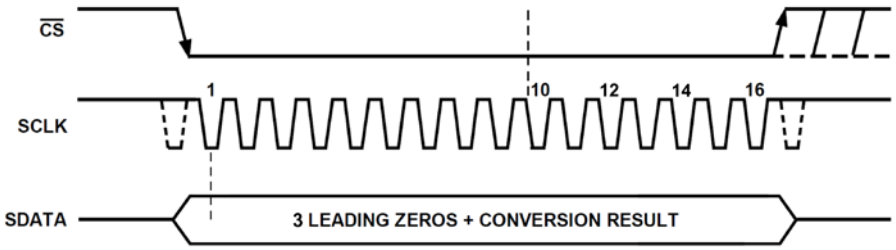


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM



The conversion is initiated on the falling edge of $\overline{CS}$. The device outputs data while the conversion is in progress, and it requires 16/14/12 serial clock cycles to complete the conversion and access the full results. The CI121S101 /CI101S101/CI081S101 data word contains 3 leading zeros, followed by 12-bit/10-bit/8-bit data in MSB first format.

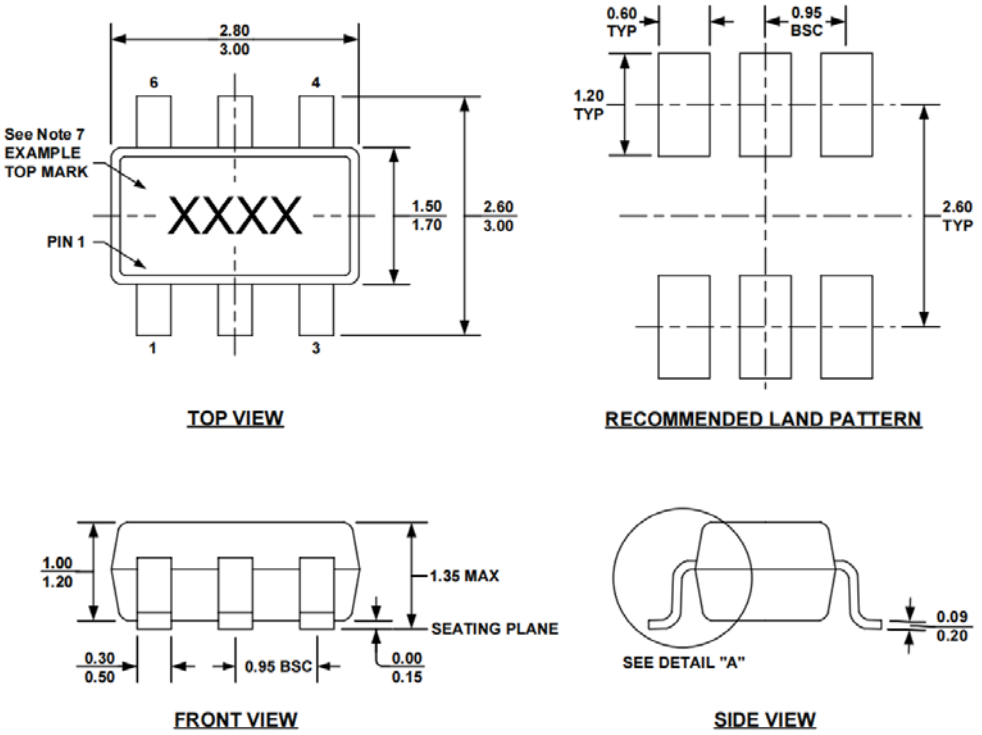
Once a data transfer is complete, SDATA will return to the tri-state mode, and another conversion can be initiated after the quiet time has elapsed by again bringing $\overline{CS}$ low.

POWER-DOWN MODE

The CI121S101 /CI101S101/CI081S101 family has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion which is the 16th falling edge of SCLK for the CI121S101 (the 14th and 12th for the CI101S101 and CI081S101, respectively). The device enters power down mode if $\overline{CS}$ goes high before the 10th SCLK falling edge. Ongoing conversion stops and SDATA goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

OUTLINE DIMENTIONS



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.