## Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

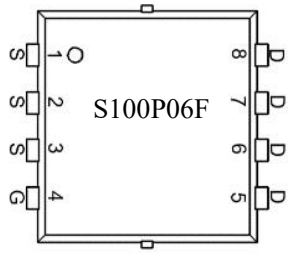
| Bvdss | Rdson | ID |
|---|---|---|
| -60V | 5.5mΩ | -100A |

## Application

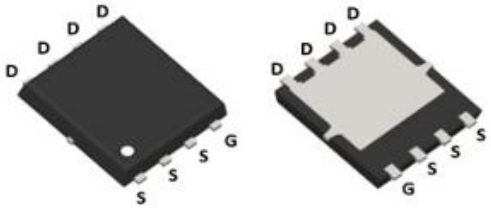
RoHS

- Battery switching application
- Hard switched and high frequency circuits
- Power management

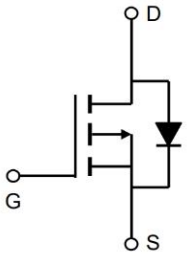
## Package




Marking and pin assignment




PDFN5*6-8L top view




Schematic diagram

## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Quantity |
|---|---|---|---|
| 100P06 | S100P06F | PDFN5*6-8L | 5000 |

## Absolute Maximum Ratings ($T_J$=25℃ unless otherwise specified)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current[1, 6] | $T_C$=25° C | $I_D$ | -100 | A |
| | $T_C$=100° C | $I_D$ | -70 | A |
| Pulsed Drain Current[2] | | $I_{DM}$ | -440 | A |
| Single Pulse Avalanche Energy[3] | | $E_{AS}$ | 960 | mJ |
| Power Dissipation[4] | $T_C$ = 25℃ | $P_D$ | 180 | W |
| Operating junction and storage temperature | | $T_J$, $T_{STG}$ | -55+150 | ℃ |

## Thermal Resistance Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance Junction-Case[1] | $R_{\theta JC}$ | 0.69 | ℃/W |
| Thermal resistance, junction – ambient[1] | $R_{\theta JA^*}$ | 60 | ℃/W |

## Ordering Information

| Ordering Number | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|
| Halogen Free | | G | D | S | |
| HLS100P06F | PDFN5*6-8L | 4 | 5,6,7,8 | 1,2,3 | Tape Reel |

## Electrical Characteristics (Tj=25℃ unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250μA | -60 | - | - | V |
| Gate-body Leakage current | $I_{GSS}$ | $V_{DS}$ = 0V, $V_{GS}$ = ±20V | - | - | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -60V, $V_{GS}$ = 0V $T_J$=25℃ | - | - | -1 | μA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -60V, $V_{GS}$ = 0V $T_J$=100℃ | - | - | -100 | μA |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$ , $I_D$ = -250μA | -1.6 | -2.0 | -2.4 | V |
| Drain-Source On-Resistance[2] | $R_{DS(on)}$ | $V_{GS}$ = -10V, $I_D$ = -15A | - | 5.5 | 7.2 | mΩ |
| Input Capacitance | $C_{lss}$ | $V_{DS}$ = -30V,$V_{GS}$ =0V, f =1MHz | - | 5403 | - | pF |
| Output Capacitance | $C_{OSS}$ | | - | 941 | - | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | - | 48 | - | |
| Gate Resistance | $R_g$ | $V_{GS}$=0V, $V_{DS}$ =0V, f=1HMz | - | 2 | - | Ω |
| Gate Resistance | gfs | $V_{DS}$=-10V , $I_D$=-30A | - | - | - | S |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = -10V,$V_{DS}$ = -30V, $I_D$ = -15A | - | 80.2 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 15.2 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 11 | - | |
| Turn-On Delay Time | $T_{d(on)}$ | $V_{GS}$ = -10V, $V_{DD}$= -30V, $R_G$ = 3Ω, $I_D$ = -15A | - | 4.5 | - | ns |
| Rise Time | $T_R$ | | - | 2.5 | - | |
| Turn-Off Delay Time | $T_{d(off)}$ | | - | 14.5 | - | |
| Fall Time | $T_F$ | | - | 3.5 | - | |
| Diode Forward Current[1,4] | $I_S$ | $V_G$=$V_D$=0V , Force Current | - | - | -100 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-15.0A, $V_{GS}$=0V,$T_J$=25℃ | - | - | -1.2 | V |
| Reverse Recovery time | $T_{rr}$ | $I_S$=-15A, dI/dt=100A/μs,$T_J$=25℃ | - | 60 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 105 | - | nC |

Note :

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is TJ = C,$V_{DD}$=-30V,$V_{GS}$=-10V,L=0.5mH

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power

## Typical Performance Characteristics

**Fig1:Typ. output characteristics**

$I_D=f(V_{DS})$

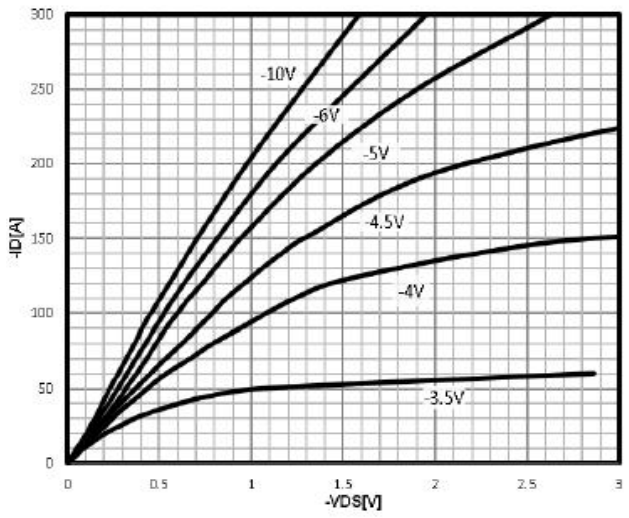



**Fig2:Typ. drain-source on resistance**

$R_{DS}(on)=f(I_D)$

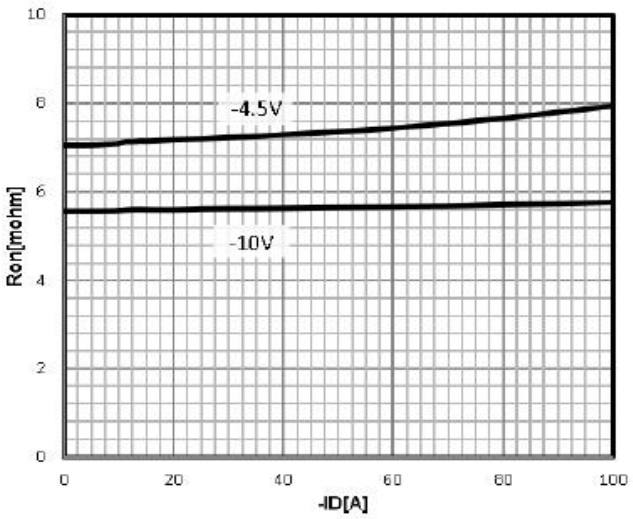



**Fig3:Typ. transfer characteristics**

$-I_D=f(-V_{GS})$

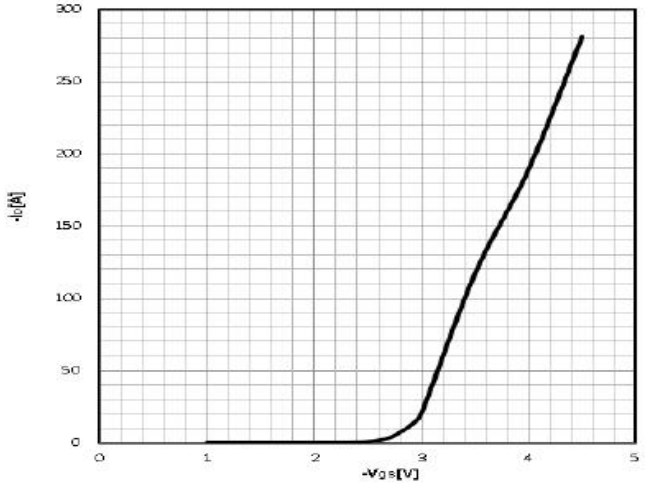



**Fig4:Drain-source on-state resistance**

RDS(on)= f(Tj)$I_D$=-15A; $V_{GS}$=-10V

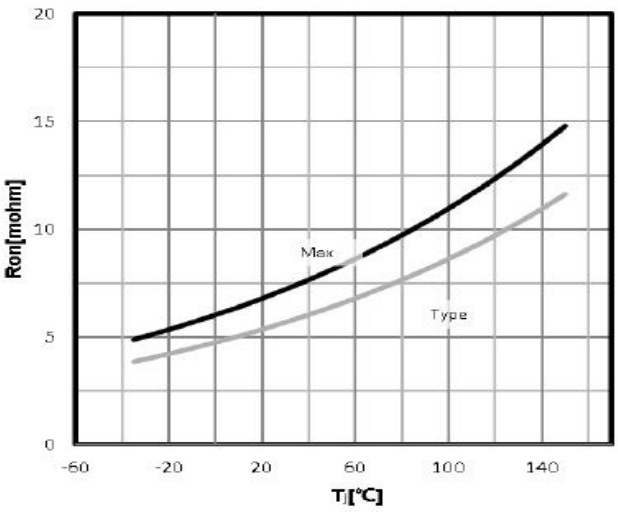


**Fig5:Gate Threshold Voltage**

$-V_{TH}=f(T_j)$; $I_D$=-250uA

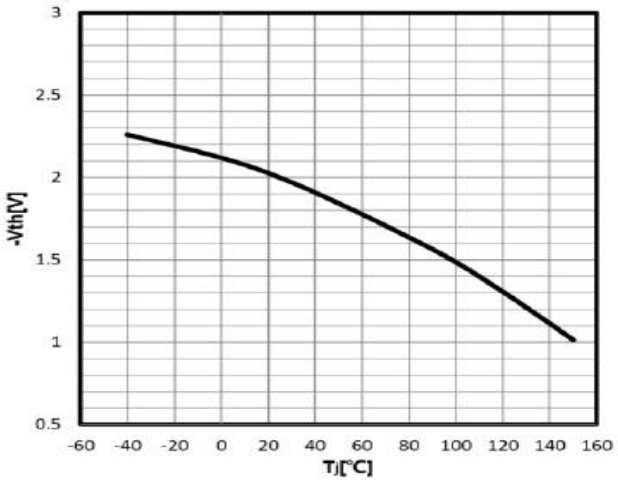



**Fig6:Drain-source breakdown voltage**

$-V_{BR(DSS)}=f(T_j)$; $I_D$=-250uA

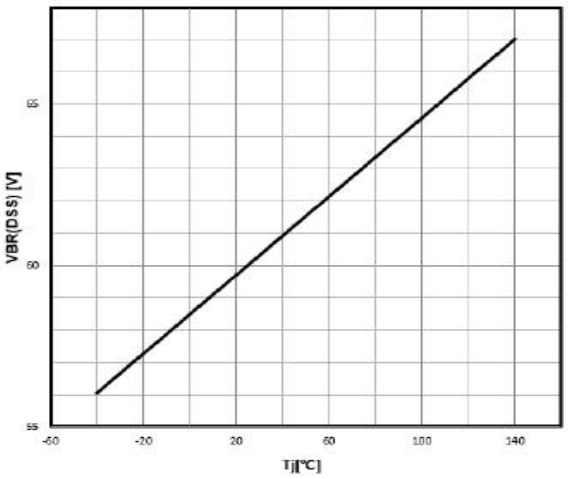



**Fig7:Typ. gate charge**

$V_{GS}=f(Q_{gate})$ ; $I_D$=-15A

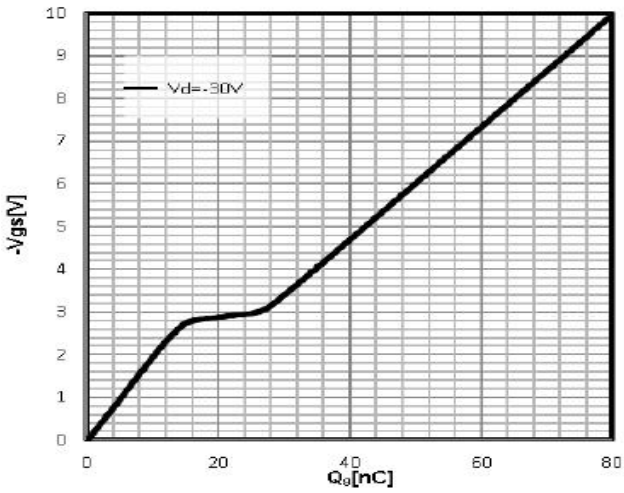



**Fig8:Typ. Capacitances**

C =f(-$V_{DS}$); $V_{GS}$=0V; f =1MHz

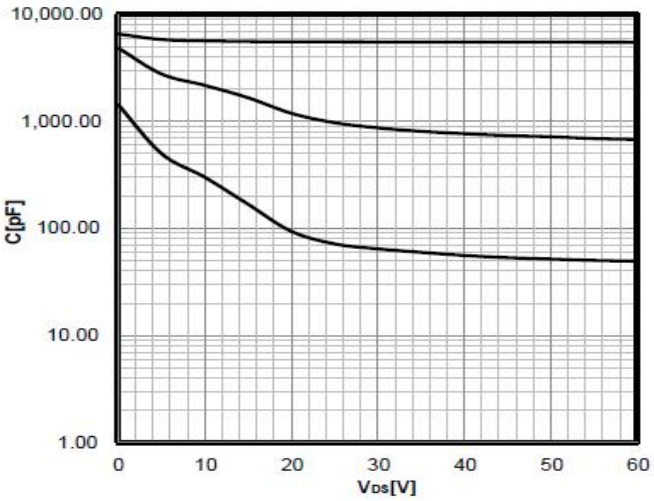



**Fig9:Power Dissipation**

$P_{tot}=f(T_C)$

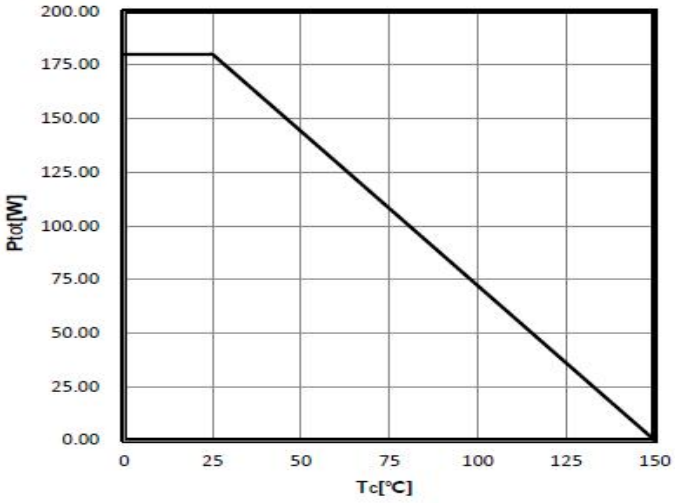



**Fig10:Maximum Drain Current**

$-I_D=f(T_C)$

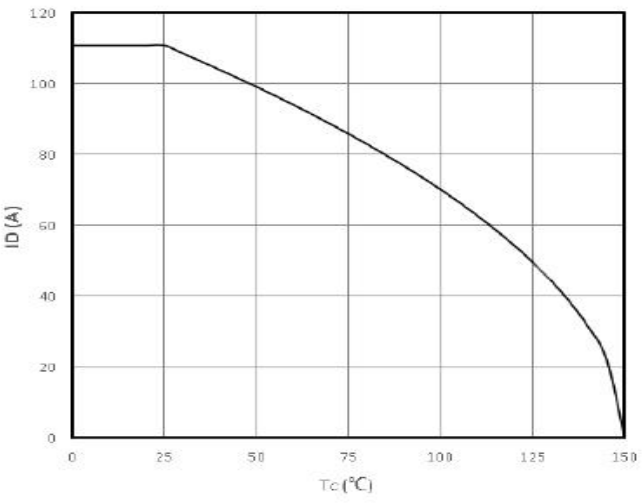


**Fig11:Safe operating area**

$-I_D=f(-V_{DS})$

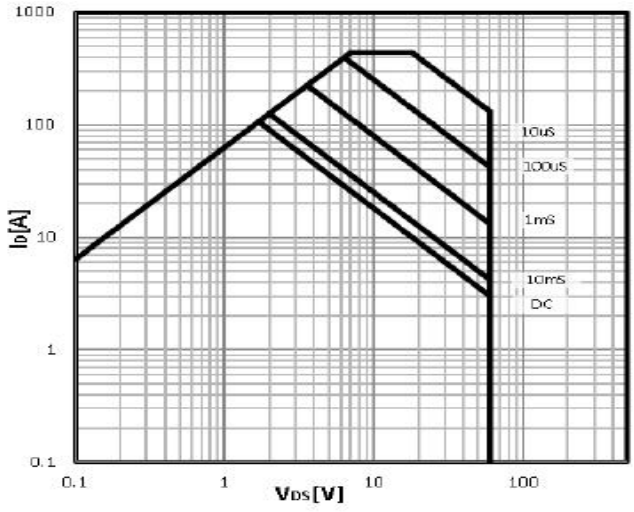



**Fig12:Body Diode Forward Voltage Variation**

$-I_F=f(-V_{DS})$

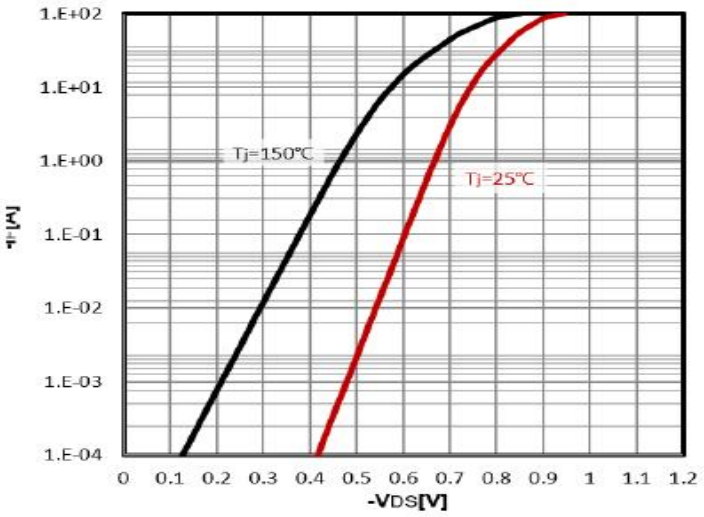
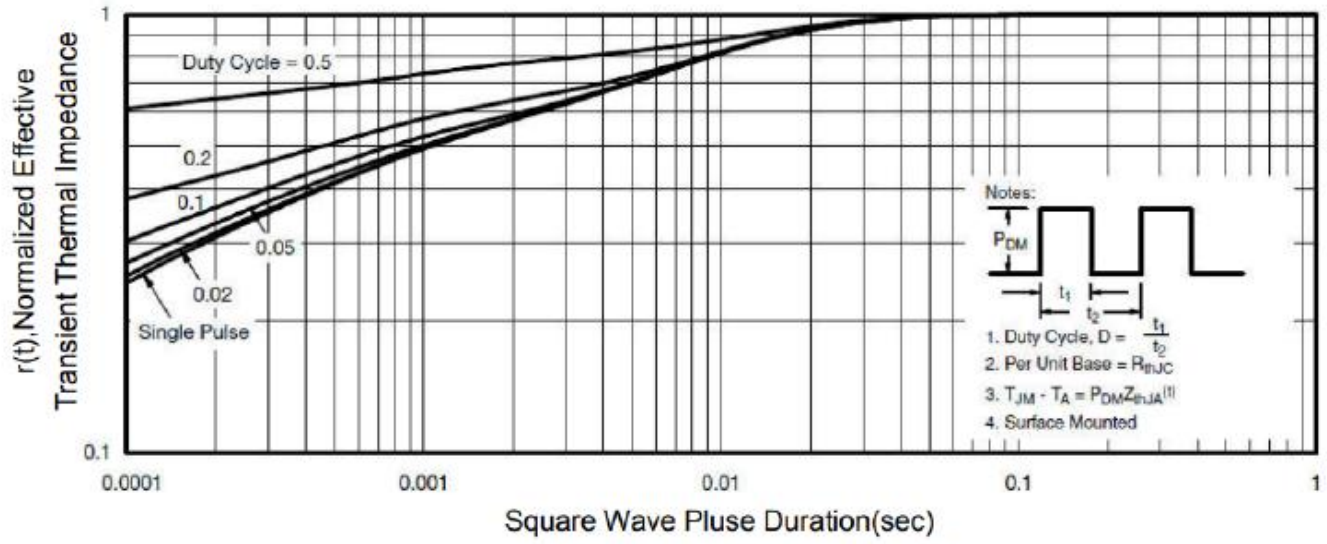


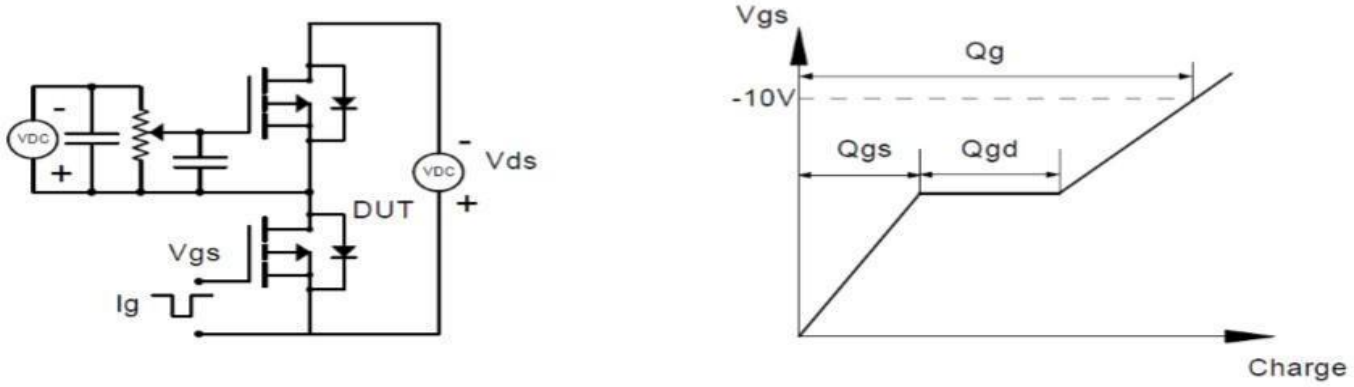

**Fig12:Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

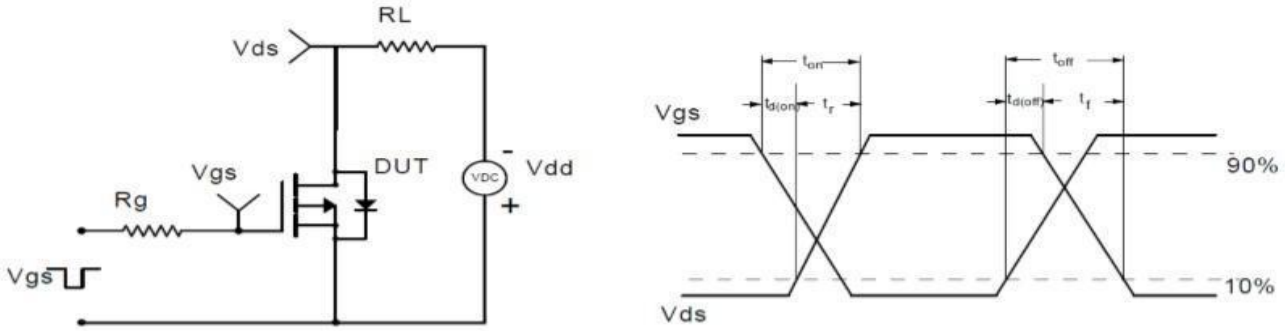


## Test Circuit and Waveform

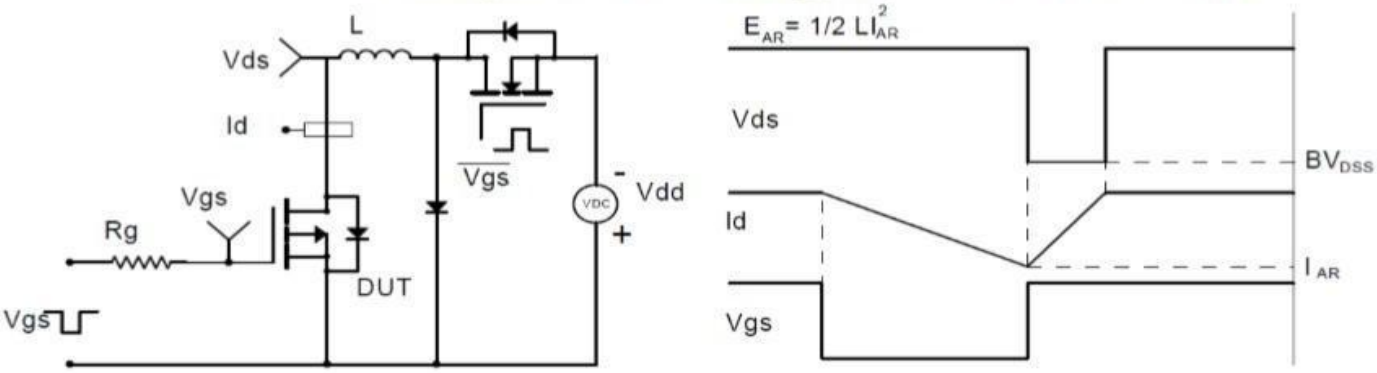
### Gate Charge Test Circuit & Waveform



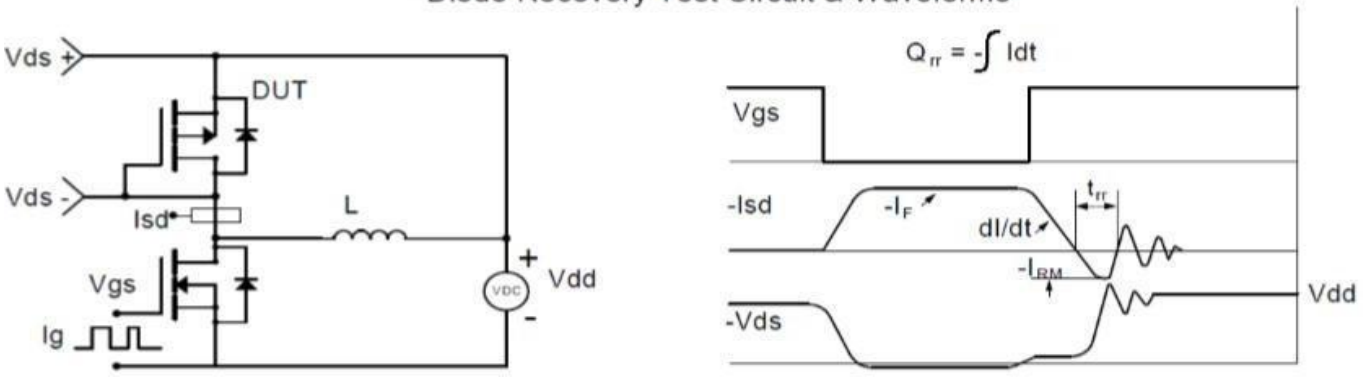

### Resistive Switching Test Circuit & Waveforms



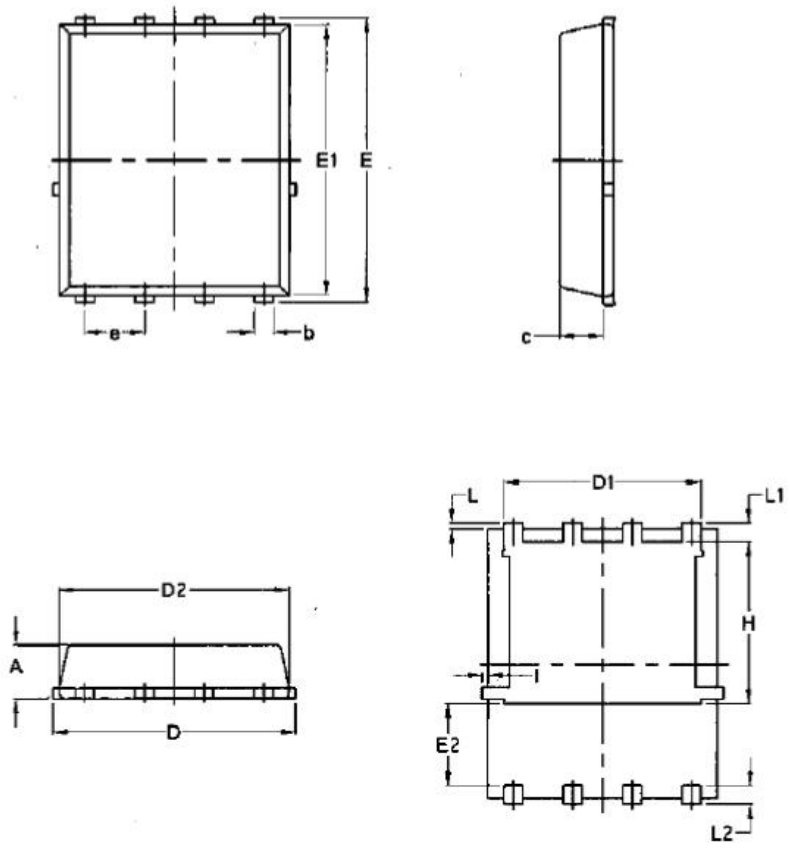

### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




### Diode Recovery Test Circuit & Waveforms



## Package Dimensions PDFN5*6-8L




| Symbol | Common | | | |
|---|---|---|---|---|
| | mm | | Inch | |
| | Mim | Max | Min | Max |
| A | 1.03 | 1.17 | 0.0406 | 0.0461 |
| b | 0.34 | 0.48 | 0.0134 | 0.0189 |
| c | 0.824 | 0.0970 | 0.0324 | 0.082 |
| D | 4.80 | 5.40 | 0.1890 | 0.2126 |
| D1 | 4.11 | 4.31 | 0.1618 | 0.1697 |
| D2 | 4.80 | 5.00 | 0.1890 | 0.1969 |
| E | 5.95 | 6.15 | 0.2343 | 0.2421 |
| E1 | 5.65 | 5.85 | 0.2224 | 0.2303 |
| E2 | 1.60 | / | 0.0630 | / |
| e | 1.27 BSC | | 0.05 BSC | |
| L | 0.05 | 0.25 | 0.0020 | 0.0098 |
| L1 | 0.38 | 0.50 | 0.0150 | 0.0197 |
| L2 | 0.38 | 0.50 | 0.0150 | 0.0197 |
| H | 3.30 | 3.50 | 0.1299 | 0.1378 |
| I | / | 0.18 | / | 0.0070 |

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