

TDS:EMIC

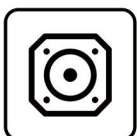
拓 電 半 導 體

自主封測 品質把控 售後保障

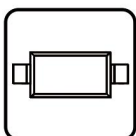
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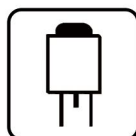
電源管理



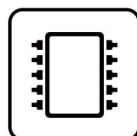
顯示驅動



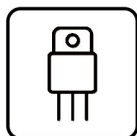
二三極管



LDO穩壓器



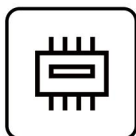
觸摸芯片



MOS管



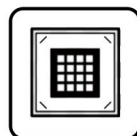
運算放大器



存儲芯片



MCU



串口通信

8205A

產品規格說明書

General Description

The 8205A is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(on)}$ and gate charge for most of the small power switching and load switch applications. They meet the RoHS and Product requirement with full function reliability approved.

General Features

$V_{DS} = 20V$ $I_D = 6A$

$R_{DS(on)} < 27m\Omega$ @ $V_{GS} = 4.5V$

$R_{DS(on)} < 37m\Omega$ @ $V_{GS} = 2.5V$

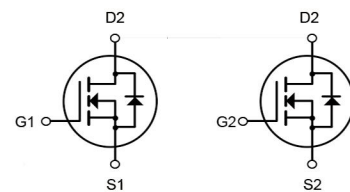
Application

Battery protection

Load switch

Uninterruptible power supply

TSSOP-8



Dual N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
8205A	TSSOP-8	8205	5000

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous	6	A
I_{DM}	Drain Current-Pulsed (Note 1)	25	A
P_D	Maximum Power Dissipation	1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	83	$^\circ C/W$

Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	21	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =19.5V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5	0.7	1.2	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =4.5A	-	21	27	mΩ
		V _{GS} =2.5V, I _D =3.5A	-	27	37	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =4.5A	-	10	-	S
Input Capacitance	C _{iss}	V _{DS} =8V, V _{GS} =0V, F=1.0MHz	-	600	-	PF
Output Capacitance	C _{oss}		-	330	-	PF
Reverse Transfer Capacitance	C _{rss}		-	140	-	PF
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, I _D =1A V _{GS} =4.5V, R _{GEN} =6Ω	-	10	20	nS
Turn-on Rise Time	t _r		-	11	25	nS
Turn-Off Delay Time	t _{d(off)}		-	35	70	nS
Turn-Off Fall Time	t _f		-	30	60	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =6A, V _{GS} =4.5V	-	10	15	nC
Gate-Source Charge	Q _{gs}		-	2.3	-	nC
Gate-Drain Charge	Q _{gd}		-	1.5	-	nC
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =1.7A	-	0.75	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	1.7	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Characteristics

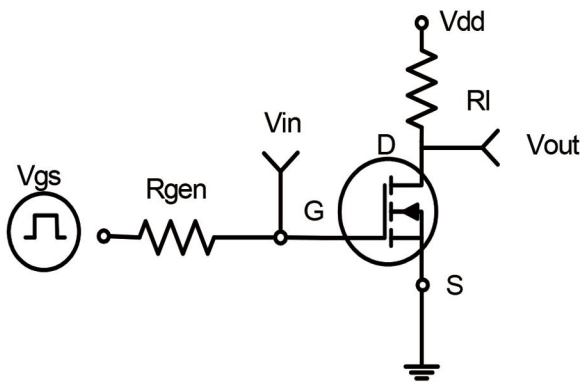


Figure 1: Switching Test Circuit

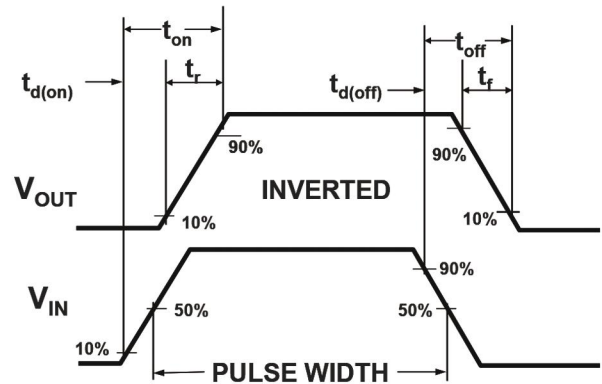


Figure 2: Switching Waveforms

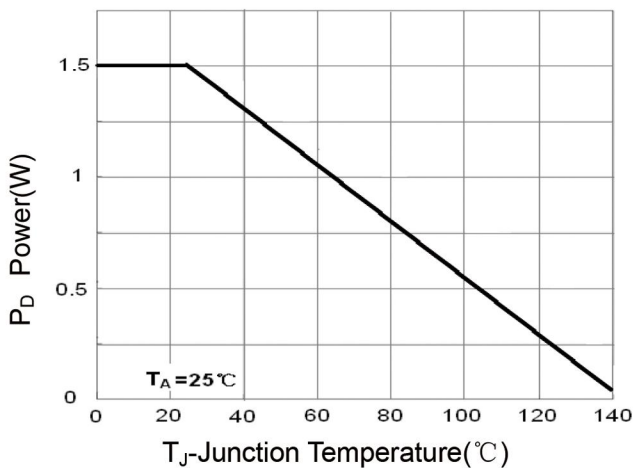


Figure 3 Power Dissipation

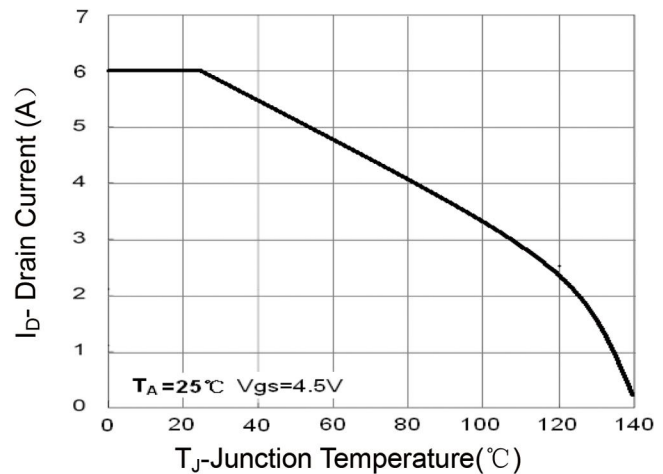


Figure 4 Drain Current

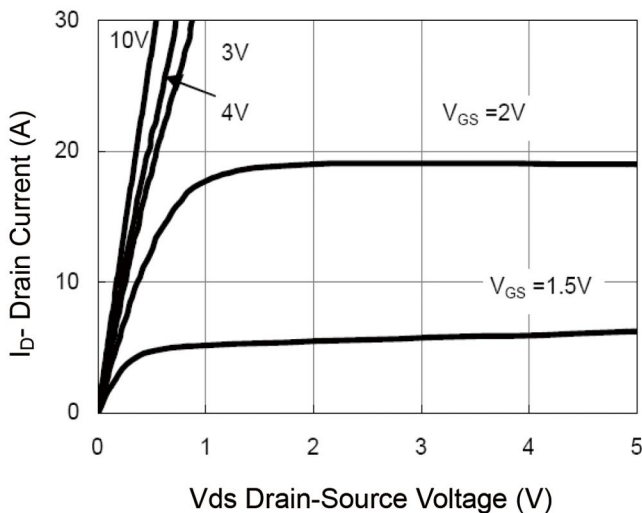


Figure 5 Output Characteristics

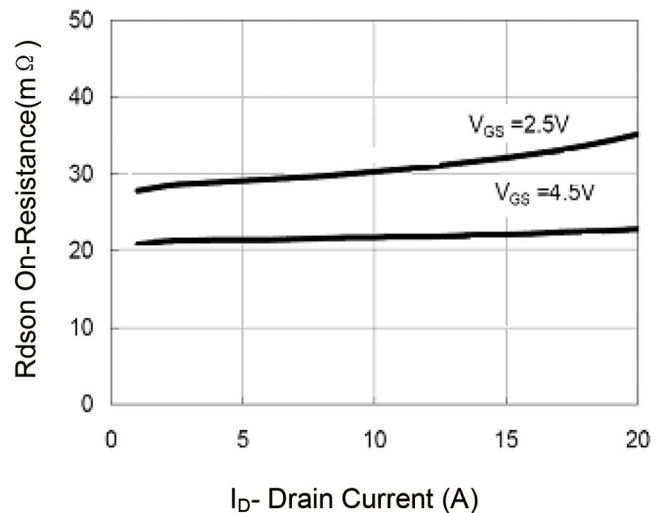


Figure 6 Drain-Source On-Resistance

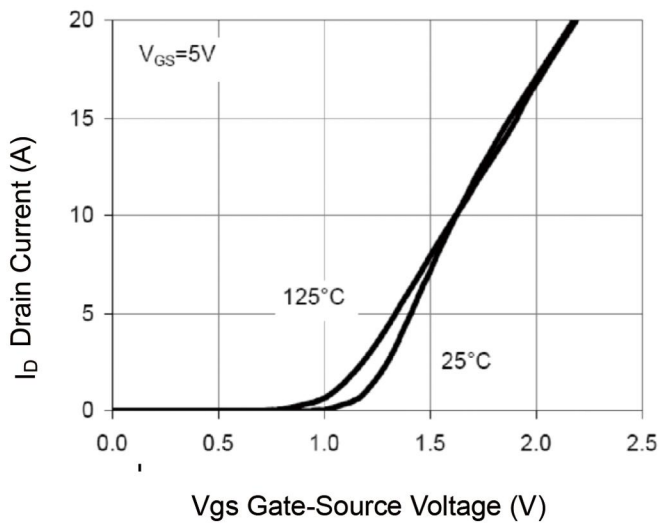


Figure 7 Transfer Characteristics

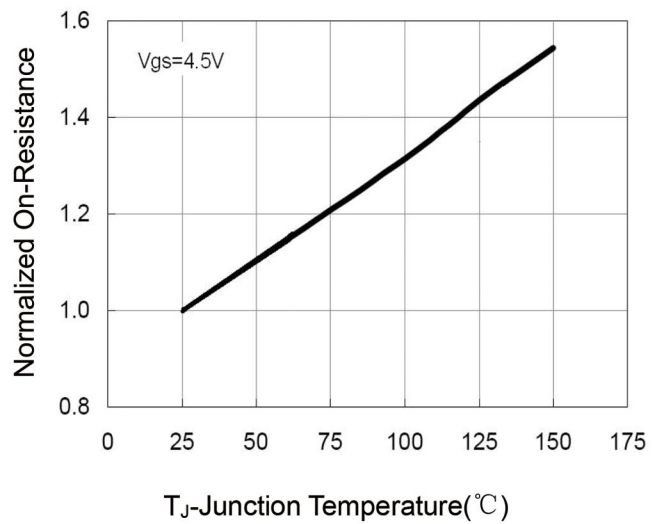


Figure 8 Drain-Source On-Resistance

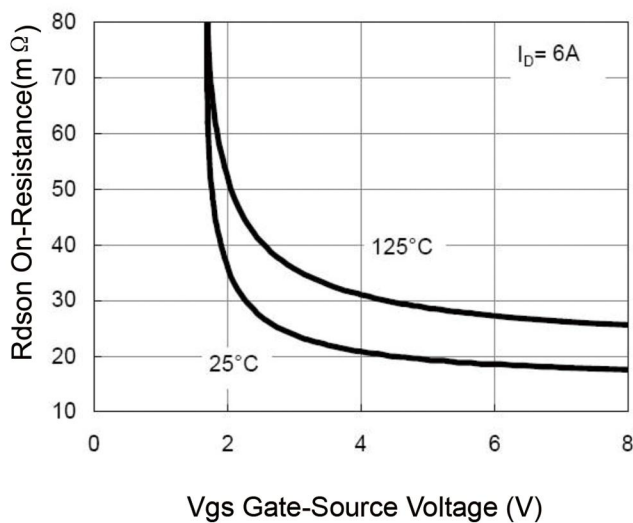


Figure 9 Rdson vs Vgs

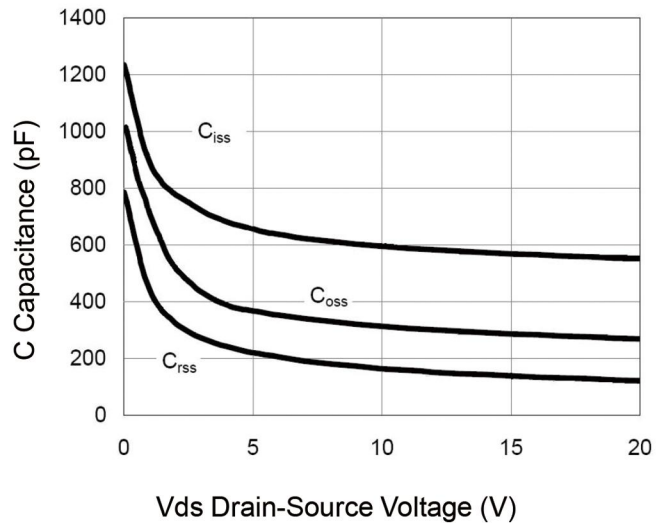


Figure 10 Capacitance vs Vds

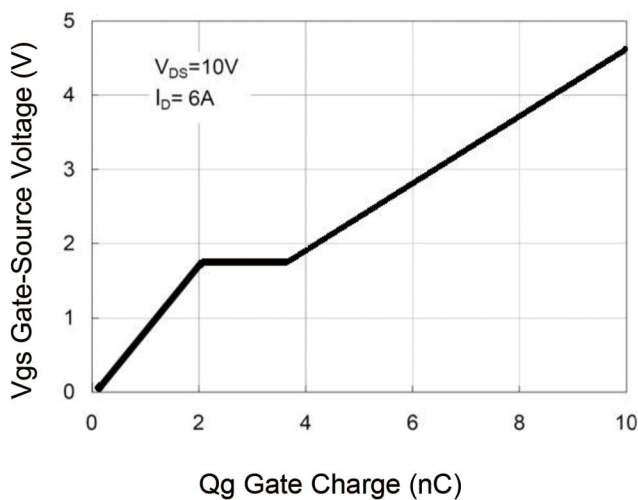


Figure 11 Gate Charge

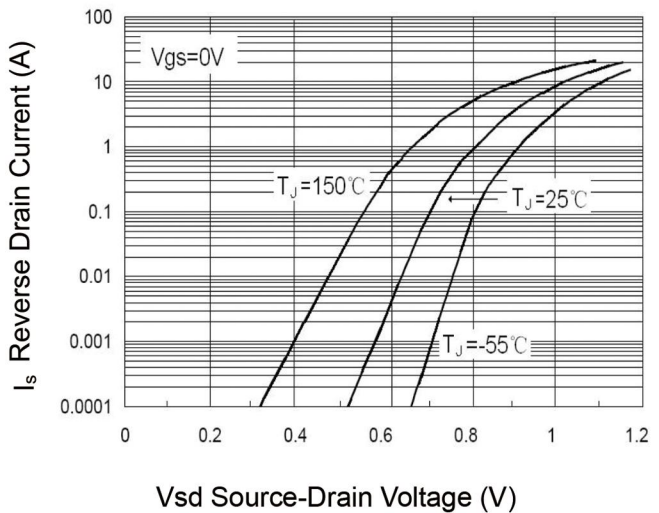


Figure 12 Source- Drain Diode Forward

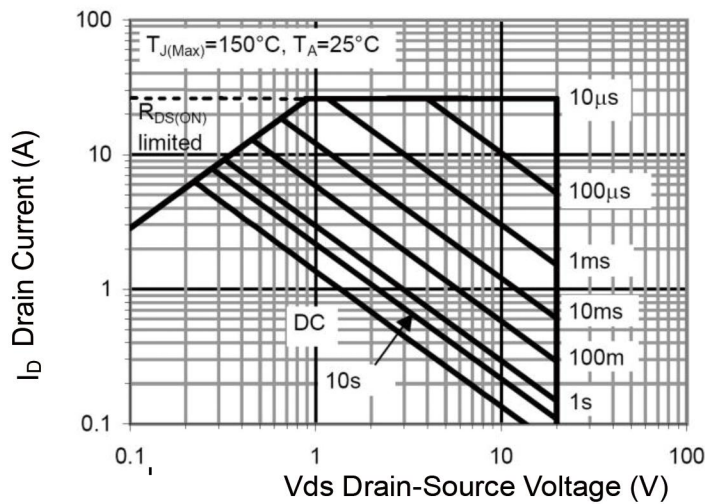


Figure 13 Safe Operation Area

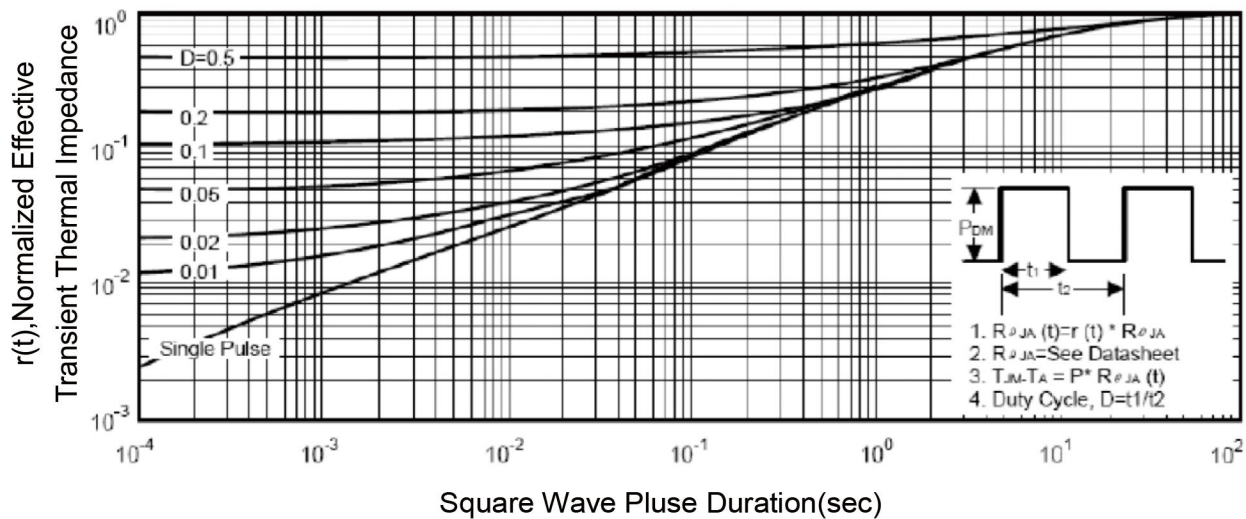
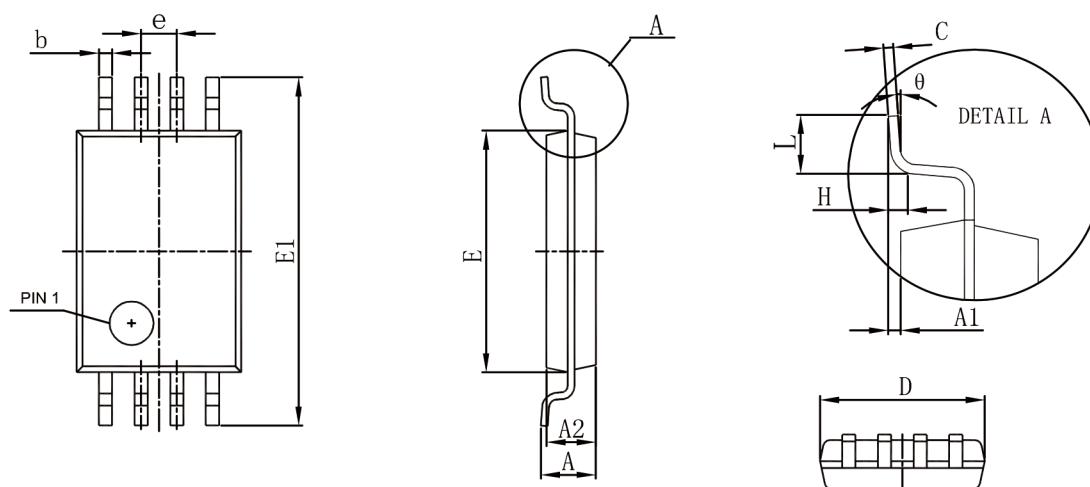


Figure 14 Normalized Maximum Transient Thermal Impedance

TSSOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°