3D Low Frequency Wake-Up Receiver

Key Features

- 3-channel ASK wake-up receiver
- Carrier frequency range 15 - 150 kHz
- Current consumption in low power listening mode 2.1 μA
- Wake-up sensitivity 80μVRMS
- Adjustable sensitivity level
- Programmable wake-up pattern 16-bit or 32-bit Manchester
- Supporting for two types of awake : frequency detection ,wake-up pattern
- Periodic artificial wake supported (1s - 2h)
- Operating supply range 2.4V - 3.6V (TA = 25°C)
- Operation temperature range -40°C to 85°C

Applications

- Active RFID tag
- High value asset tracking
- Access management system
- Real-time location system
- Wireless sensor network
- Operator identification
- Access control
- Remote keyless entry

Contents

1 General Description

The Si3933 is a 3-channel low power ASK receiver that is able to generate a wake-up upon detection of a data signal which uses a LF carrier frequency between 15-150 kHz. The integrated correlator can be used for detection of a programmable 16-bit or 32-bit Manchester wake-up pattern.

The Si3933 can operate using one, two, or three active channels. The device provides digital RSSI value and frequency detection for each active channel. The programmable features of Si3933 enable to optimize its settings for achieving a longer distance while retaining a reliable wake-up generation. The sensitivity level of Si3933 can be adjusted in presence of a strong field or in noisy environments.

The Si3933 offers an internal Clock Generator, which is either derived from a crystal oscillator or the internal RC oscillator. The user can decide to use the external clock generator instead.

The Si3933 supports a programmable data rate and Manchester decoding with clock recovery. Antenna tuning is greatly simplified, as the automatic tuning feature ensures perfect matching to the desired carrier frequency.

1.1 Key Features

3-channel ASK wake-up receiver
Carrier frequency range 15 - 150 kHz
Current consumption in low power listening mode 2.1 μA
Wake-up sensitivity 80μVRMS
Wake-up sensitivity level adjustable
programmable 16-bit or 32-bit Manchester wake-up pattern
Supporting doubling of wake-up pattern: frequency detection ,wake-up pattern
False wake-up counter
Periodical forced wake-up supported (1s-2h)
Operating supply range 2.4V-3.6V (TA = 25°C)
Operation temperature range -40°C to 85°C

1.2 Applications

The Si3933, 3D Low Frequency Wake-Up Receiver is ideal for Active RFID tags, Access management systems, High value asset tracking, PKE Remote key-less entry systems, Real-time location systems, Operator identification, Access control, and Wireless sensors.

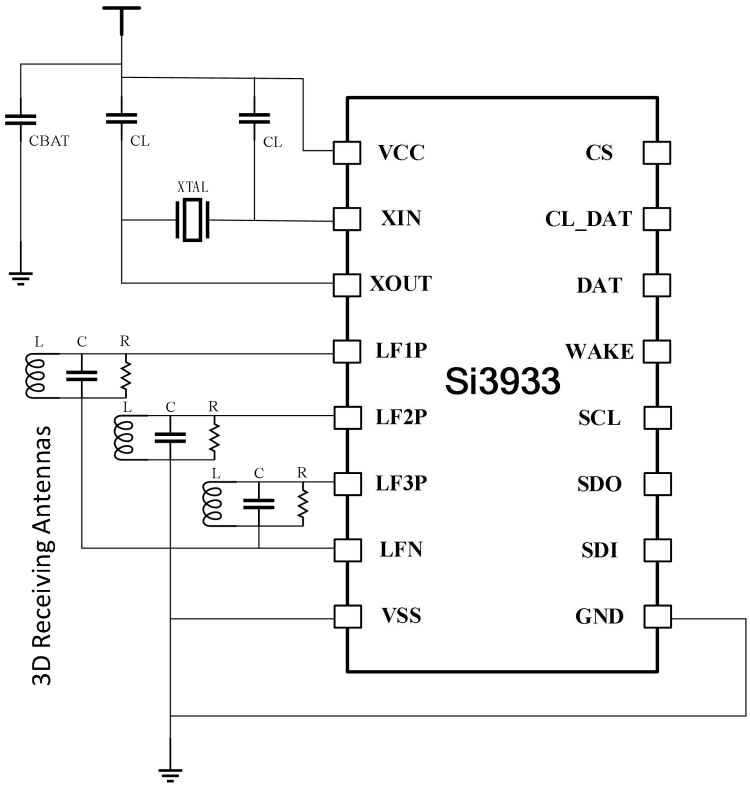


Figure 1-1 Si3933 Typical Application Diagram with Crystal Oscillator

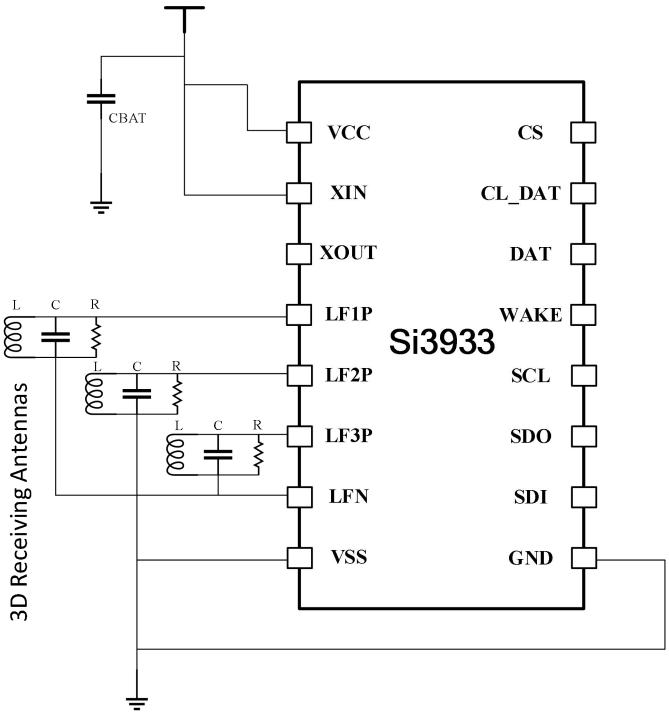


Figure 1-2 Si3933 Typical Application Diagram with RC Oscillator

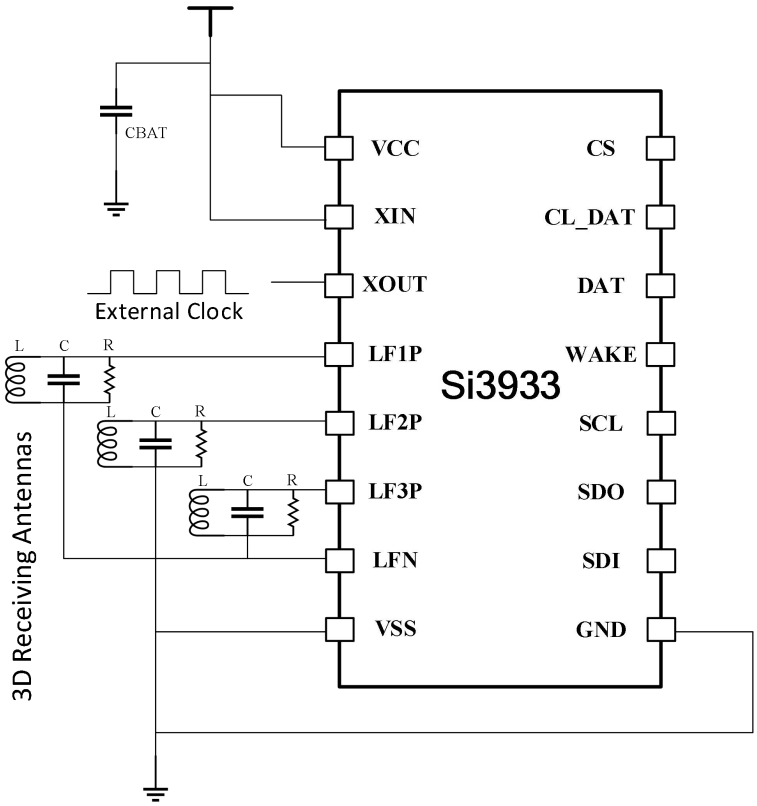


Figure 1-3 Si3933 Typical Application Diagram with Clock from External Source

When using the internal RC oscillator to do the clock, the XIN pin needs to be connected to the VCC, while XOUT pin should stay floating. When using the external clock source, the XIN pin needs to be connected to the VCC and XOUT pin needs to be connected to the external clock source.

External devices required for Si3933:

1.Power stabilized capacitor CBAT

2.32.768kHZ crystal XTAL and two pull-up capacitor CL (If you use the internal RC oscillator instead of the oscillator, it can be omitted)

3.1~ 3 LC resonant network, depending on the number of channels used.

Table 1-1 Typical application value of external devices in 125khz carrier

External device	Typical application value for 125khz carrier
CBAT	10uF
CL	12pF
L	7.2mH
C	110pF
R	240K

2 Block Diagram

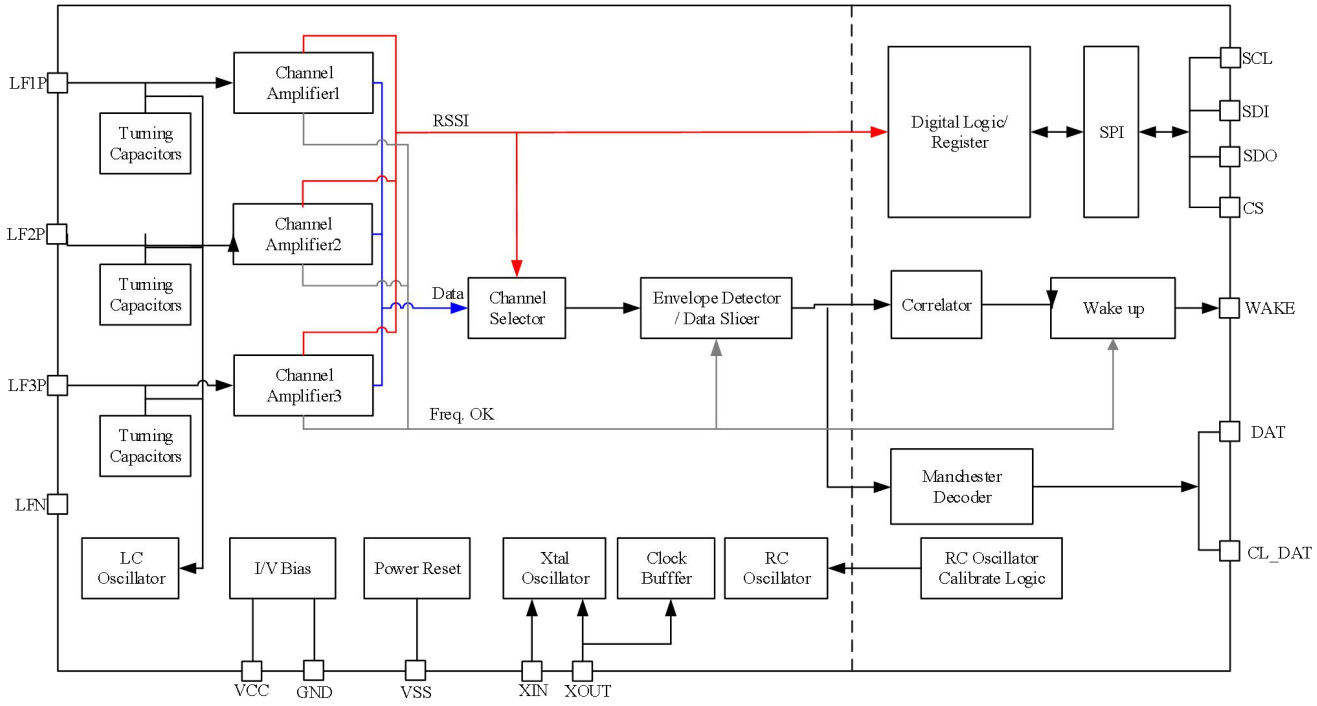


Figure 2-1 Block Diagram of Si3933

3 Pin Description

3.1 TSSOP Package

Si3933 uses TSSOP-16 package. The pin is shown in figure 3-1 and description of the pin is shown in table 3-1.

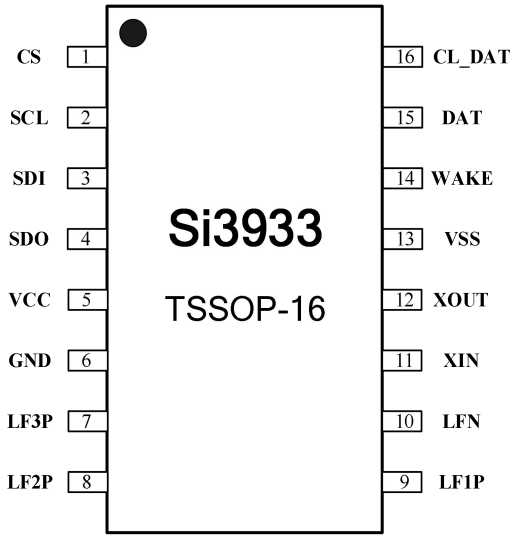


Figure 3-1 The figure of Si3933 TSSOP-16 Pin

Table 3-1 Si3933 TSSOP-16 Pin Description

Pin Name	Pin Number	Pin Type	Description
CS	1	Digital input	Chip select
SCL	2	Digital input	SDI interface clock
SDI	3	Digital input	SDI data input
SDO	4	Digital output /Tristate	SDI data output (Tristate when CS is low)
VCC	5	Supply pad	Positive supply voltage
GND	6	Supply pad	Negative supply voltage
LF3P	7	Analog I/O	Channel 3 of Input antenna
LF2P	8	Analog I/O	Channel 2 of Input antenna
LF1P	9	Analog I/O	Channel 1 of Input antenna
LFN	10	Analog I/O	Common ground for antenna 1/2/3
XIN	11	Analog I/O	Crystal oscillator input
XOUT	12	Analog I/O	Crystal oscillator output

VSS	13	Supply pad	Substrate
WAKE	14	Digital output	Wake-up output IRQ
DAT	15	Digital output	Data output
CL_DAT	16	Digital output	Manchester recovered clock

3.2 QFN-16 Package

Si3933 uses QFN-16 package. The pin is shown in figure 3-2 and description of the pin is shown in Table 3-2.

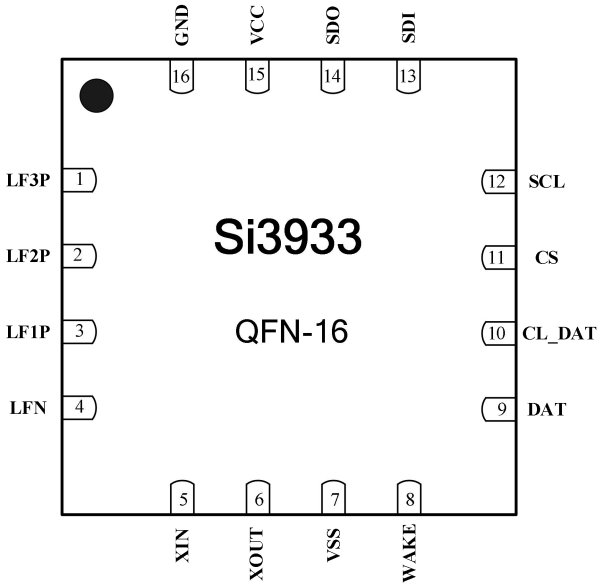


Figure 3-2 The figure of Si3933 QFN-16 Pin

Table 3-2 Si3933 QFN-16 Pin Description

Pin Name	Pin Number	Pin Type	Description
LF3P	1	Analog I/O	Channel 3 of Input antenna
LF2P	2	Analog I/O	Channel 2 of Input antenna
LF1P	3	Analog I/O	Channel 1 of Input antenna
LFN	4	Analog I/O	Common ground for antenna 1/2/3
XIN	5	Analog I/O	Crystal oscillator input
XOUT	6	Analog I/O	Crystal oscillator output
VSS	7	Supply pad	Substrate
WAKE	8	Digital output	Wake-up output IRQ

DAT	9	Digital output	Data output
CL_DAT	10	Digital output	Manchester recovered clock
CS	11	Digital input	Chip select
SCL	12	Digital input	SDI interface clock
SDI	13	Digital input	SDI data input
SDO	14	Digital output / Tristate	SDI data output (Tristate when CS is low)
VCC	15	Supply pad	Positive supply voltage
GND	16	Supply pad	Negative supply voltage

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those Absolute Maximum Ratings listed in table 4-1 may cause permanent damage to the device.

Table 4-1 Si3933 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
VCC	DC supply voltage	-0.5	5	V	
V_{IN}	Input pin voltage	-0.5	5	V	
I_{SOURCE}	Input current (latch up immunity)	-100	100	mA	
ESD	Electrostatic discharge	±2		kV	HBM
P_t	Total power dissipation (all supplies and outputs)		0.07	mW	
T_{strg}	Storage temperature	-65	150	℃	
T_{body}	Package body temperature		260	℃	
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			

4.2 Operating Conditions

Table 4-2 Si3933 Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Positive supply voltage	2.4	3	3.6	V
VSS	Negative supply voltage	0		0	V
T_{AMB}	Ambient temperature	-40		85	℃

4.3 DC/AC Characteristics for Digital Inputs and Outputs

Table 4-3 Si3933 DC/AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMOS Input						
V_{IH}	High level input voltage		0.6VCC	0.7VCC	0.8VCC	V
V_{IL}	Low level input voltage		0.12VCC	0.2VCC	0.3VCC	V
I_{LAEK}	Input leakage current				100	nA
CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	VCC-0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			VSS+0.4	V
C_L	Capacitive load	For a clock frequency of 1 MHz			400	pF
Tristate CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	VCC-0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			VSS+0.4	V
I_{OZ}	Tristate leakage current	To VDD and VSS			100	nA

4.4 Electrical System Specifications

Table 4-4 Si3933 Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Characteristics						
RIN	AC Input Impedance at 125kHz	In case no antenna damper is set (R1<4 >=0)		5		kΩ
F1MAX	Maximum Input Frequency Band1			150		kHz
F1MIN	Minimum Input Frequency Band1			95		kHz
F2MAX	Maximum Input Frequency Band2			95		kHz
F2MIN	Minimum Input Frequency Band2			65		kHz
F3MAX	Maximum Input Frequency Band3			65		kHz
F3MIN	Minimum Input Frequency Band3			40		kHz
F4MAX	Maximum Input Frequency Band4			40		kHz
F4MIN	Minimum Input Frequency Band4			23		kHz
F5MAX	Maximum Input Frequency Band5			23		kHz
F5MIN	Minimum Input Frequency Band5			15		kHz
Current Consumption						
I1CHRC	Current Consumption in standard listening mode with one active channel and RC-oscillator as Clock Generator			3.2		uA
I2CHRC	Current Consumption in standard listening mode with two active channels and			4.8		uA

	RC-oscillator as Clock Generator					
I3CHRC	Current Consumption in standard listening mode with three active channels and RC-oscillator as Clock Generator			6.4		uA
I3CHSCRC	Current Consumption in scanning mode with three active channels and RC-oscillator as Clock Generator			3.2		uA
I3CHOORC	Current Consumption in ON/OFF mode with three active channels and RC-oscillator as Clock Generator	11% Duty Cycle		2.1		uA
		50% Duty Cycle		4		
I3CHXT	Current Consumption in standard listening mode with three active channels and crystal oscillator as Clock Generator			6.6		uA
IDATA	Current Consumption in Preamble detection / Pattern correlation / Data receiving mode (RC-oscillator)	With 125 kHz carrier frequency and 1 kbps data-rate. No load on the output pins.		8.6		uA
IBOOST	Additional current consumption per channel if gain boost enabled			80		nA
Input Sensitivity						
SENS1	Input Sensitivity on	With 125 kHz carrier frequency,		100		uVrms

	all channels in the Band1	chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection				
SENS1B	Input Sensitivity on all channels in the Band1 with 3dB gain boost	With 125 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
SENS2	Input Sensitivity on all channels in the Band2	With 90 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		100		uVrms
SENS2B	Input Sensitivity on all channels in the Band2 with 3dB gain boost	With 90 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
SENS3	Input Sensitivity on all channels in the Band3	With 60 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		100		uVrms
SENS3B	Input Sensitivity on all channels in the Band3 with 3dB gain boost	With 60 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
SENS4B	Input Sensitivity on all channels in the Band4 with 3dB gain boost	With 30 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
SENS5B	Input Sensitivity on all channels in the Band5 with 3dB gain boost	With 18 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		80		uVrms
Channel Settling Time						
TSAMP	Amplifier settling time			250		us
Crystal Oscillator						
FXTAL	Frequency	Crystal dependent	25	32.768	45	kHz
TXTAL	Start-up Time			1		s
IXTAL	Current consumption			560		nA
External Clock Source						
IEXTCL	Current consumption			0.8		uA
FEXTCL	Frequency		25		45	kHz

RC Oscillator						
FRCNCAL	Frequency	If no calibration is performed	25	32.768	45	kHz
FRCCAL32		If calibration with 32.768 kHz reference signal is performed	31	32.768	34.5	
FRCCALMAX		Maximum achievable frequency after calibration		45		
FRCCALMIN		Minimum achievable frequency after calibration		23.75		
TRC	Start-up time	From RC enable (R1<1> = 0)			1	s
TCALRC	Calibration time		65			Periods of reference clock
IRC	Current consumption			730		nA
LC Oscillator						
FLCOMIN	Minimum Frequency	L=47mH，C=2.3nF		15		kHz
FLCOMAX	Maximum Frequency	L=7.2mH，C=150pF		150		kHz
RPARMIN	Minimum Eq. Parallel			10		kΩ
Tuning Caps						
LF1Ptuning	Capacitance	Maximum internal capacitance (in step of 1pF) on LF1P		31		pF
LF2Ptuning		Maximum internal capacitance (in step of 1pF) on LF2P		31		pF
LF3Ptuning		Maximum internal capacitance (in step of 1pF) on LF3P		31		pF

5 Operating Modes

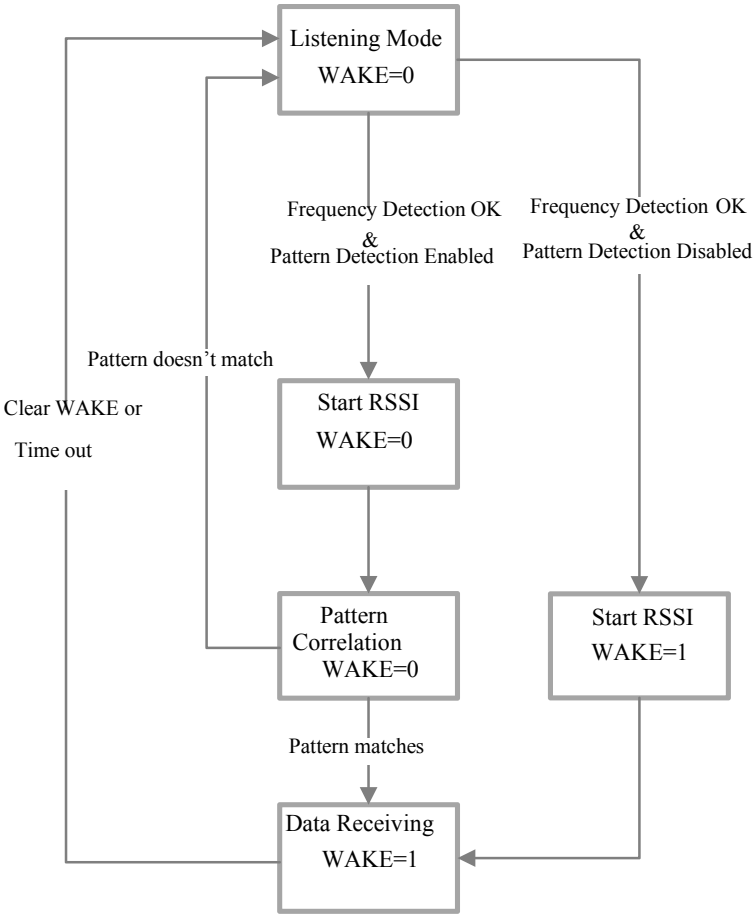


Figure 5-1 Si3933 Operating Modes Flow Chart

5.1 Listening Mode

In listening mode, the chip is active and looks continuously for the presence of the carrier on the input of all active channels. In case the carrier is detected, then the RSSI measurements get started on all three channels and the result is stored in the memory.

If the three dimensional detection is not required, then it is possible to deactivate one or more channels. In case only two channels are required, then the deactivated channel must be the number two;while in case only one channel is needed, then the active channel must be the number one.

Inside the listening mode, it is possible to distinguish the following three modes:

1.Standard Listening Mode. All channels are active at the same time.

2.Scanning Mode (Low Power Mode 1). In this sub-mode, a time slot T=1ms is defined and in each time slot only one channel can be active. As shown in Figure 5-2 when a certain time slot is over, the current active channel is switched OFF and the next channel becomes active and so on. If, for example all three channels are enabled, in the first time slot the only active channel is the number one. When the first time slot is over, the channel one is switched OFF and the channel three becomes active. During the third time slot, the channel two is active while the other two are OFF. This channel rotation starts back from the channel one and goes on until the presence of the carrier is detected by any channel. The Scanning mode (channel rotation) is managed internally by the Si3933 and doesn't need any activity from the host system (MCU). As soon as one channel detects the frequency, all three channels become immediately active at the same time. The Si3933 can perform a simultaneous multidirectional evaluation (on all three channels) of the field and evaluate which channel has the strongest RSSI. The channel with the highest RSSI will be put through to the demodulator. In this way it is possible to perform multidirectional monitoring of the field with a current consumption of a single channel, keeping the sensitivity as good as if all channels are active at the same time.

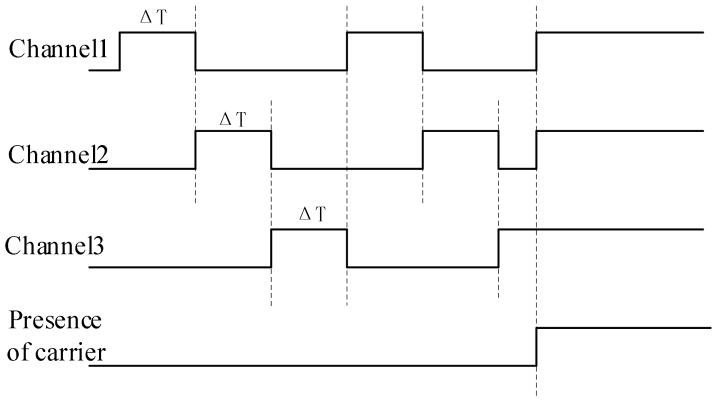


Figure 5-2 Scanning Mode

3. ON/OFF Mode (Low Power Mode 2). In this low power sub-mode the chip sets the receiving channels in polling mode; all active channels are on at the same

time only for a certain time T (where T is 1 ms). The OFF-time can be defined with the bits R4<7:6>. If, for example, R4<7:6>=11 (see Figure 5-3) the active channels will be 1ms ON and 8ms OFF.

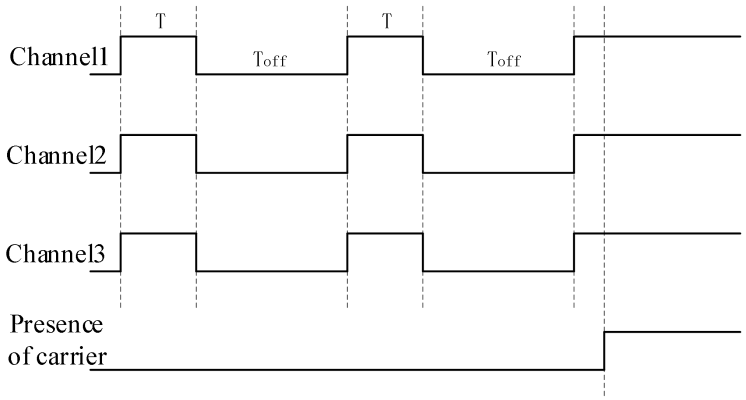


Figure 5-3 ON/OFF Mode

5.2 Artificial Wake-Up

For each of these sub modes it is possible to enable a further feature called Artificial Wake-up. The Artificial Wake-up is a counter based on the used Clock Generator. Three bits define a time window (see R8<2:0>). If no activity is seen within this time window, the chip will produce an interrupt on the WAKE pin that lasts 128 µs. With this interrupt the microcontroller (µC) can get feedback on the surrounding environment (e.g. read the false wake-up register R13<7:0>) and/or take actions in order to change the setup.

5.3 Preamble Detection / Pattern Correlation

The chip can go in to this mode after detecting a LF carrier only if the data correlation is enabled (R1<1>=1). The correlator searches first for preamble bits and then for data pattern. Should the pattern correlation be disabled (R1<1>=0), the Si3933 goes directly in Data receiving mode.

In this mode,if the received pattern matches, then the wake-up interrupt is displayed on the WAKE output (Wake goes high) and the chip goes in Data receiving mode. If the pattern fails, then the internal wake-up (on all active channels) is terminated and no interrupt is produced.

Having per default DAT_MASK disabled (R0<6>=0), the DAT pin shows the entire demodulated incoming signal (carrier burst+preamble+pattern+data). If DAT_MASK is enabled (R0<6>=1), the data will be displayed only after the generation of the WAKEUP interrupt.

5.4 Data Receiving

After a successful wake-up the chip enters the data receiving mode. In this mode the chip can be retained a normal OOK receiver. The data is provided on the DAT pin and in case the Manchester decoder is enabled (see R1<3>=1), the recovered clock is present on the CL_DAT. It is possible to set the chip back to listening mode either with a direct command CLEAR_WAKE or by using the timeout feature. This feature automatically sets the chip back to listening mode after a certain time defined by the bits R7<7:5>.

6 Register and SPI

6.1 Register

Table 6-1 Register Overview

	7	6	5	4	3	2	1	0
R0	PATT32	DAT_MASK	ON_OFF	MUX_123	EN_A2	EN_A3	EN_A1	EN_IV
R1	ABS_HY	AGC_TLIM	AGC_UD	ATT_ ON	EN_MAN CH	EN_PAT2	EN_ WPAT	EN_ XTAL
R2	S_ABS	EN_EXT_ CLK	G_BOOST	VB3_D	DISPLAY_CLK		S_WU1	
R3	HY_20m	HY_POS	FS_SLC			FS_ENV		
R4	T_OFF		D_RES		GR			
R5	PATT2B							
R6	PATT1B							
R7	T_OUT			T_HBIT				
R8	BAND_SEL					T_AUTO		
R9	BLOCK_ AGC							
R10				RSSI1				
R11				RSSI2				
R12				RSSI3				
R13	F_WAKE							
R14	RC_CAL _OK	RC_CAL_KO	RC_OSC_TAPS					
R15				LC_CAL_ OK	LC_CAL_ KO			
R16	CLOCK_ GEN_DIS		RC_OSC_ MIN	RC_OSC_ MAX		LC_OSC_MUX		
R17				CAP_CH1				
R18				CAP_CH2				
R19				CAP_CH3				
R20								
R21				GBOOST	START_ I_XTAL	I_XTAL		
R22					RC_OSC_TAPS_EXTD			

Table 6-1 Register Description and Default Value

Register	Name	Type	Default Value	Description
R0<7>	PATT32	R/W	0	Pattern extended to 32 bits (PAT32=0 16 bits, PAT32=1 32bits)
R0<6>	DAT_MASK	R/W	0	Masks data on DAT pin before wake-up (DAT_MASK = 0 → data not masked; DAT_MASK = 1 → data masked)
R0<5>	ON_OFF	R/W	0	ON/OFF operation mode.
R0<4>	MUX_123	R/W	0	Scan mode enable
R0<3>	EN_A2	R/W	1	Channel 2 enable
R0<2>	EN_A3	R/W	1	Channel 3 enable
R0<1>	EN_A1	R/W	1	Channel 1 enable
R0<0>	EN_IV	R/W	0	Current/voltage offset enable,0 effective
R1<7>	ABS_HY	R/W	0	Enable Data slicer absolute reference
R1<6>	AGC_TLIM	R/W	0	AGC acting within the limited time(256us)
R1<5>	AGC_UD	R/W	0	0，AGC only reduce gain note:R1<5>can't be set to 1, otherwise there will be a phenomenon of arousal discontinuity
R1<4>	ATT_ON	R/W	0	Antenna damper enable
R1<3>	EN_MANCH	R/W	0	Manchester decoder enable
R1<2>	EN_PAT2	R/W	0	Double wake-up pattern correlation
R1<1>	EN_WPAT	R/W	1	Correlator enable
R1<0>	EN_XTAL	R/W	1	Crystal oscillator enable
R2<7>	S_ABS	R/W	0	Data slicer absolute threshold reduction
R2<6>	EN_EXT_ CLK	R/W	0	Enables external clock generator
R2<5>	G_BOOST	R/W	0	Amplifier Gain Boost
R2<4>	VB3_D	R/W	0	Bias voltage vb3 reduction
R2<3:2>	DISPLAY_ CLK	R/W	00	Set to 11 in case the clock generator's frequency is shown on pin CL_DAT,R16<7>=1
R2<1:0>	S_WU1	R/W	00	Tolerance setting for the Frequency detection
R3<7>	HY_20m	R/W	0	Data slicer hysteresis

				0:comparator hysteresis = 40mV 1:comparator hysteresis = 20mV
R3<6>	HY_POS	R/W	0	Data slicer hysteresis only on positive edges (HY_POS=0, hysteresis on both edges, HY_POS=1, hysteresis only on positive edges)
R3<5:3>	FS_SLC	R/W	100	Data slicer time constant
R3<2:0>	FS_ENV	R/W	000	Envelop detector time constant
R4<7:6>	T_OFF	R/W	00	OFF time in ON/OFF operation mode 00:1ms 01:2ms 10:4ms 11:8ms
R4<5:4>	D_RES	R/W	01	Antenna damping resistor
R4<3:0>	GR	R/W	0000	Gain reduction
R5<7:0>	PATT2B	R/W	01101001	2nd Byte of wake-up pattern
R6<7:0>	PATT1B	R/W	10010110	1st Byte of wake-up pattern
R7<7:5>	T_OUT	R/W	000	Automatic time-out
R7<4:0>	T_HBIT	R/W	01011	Bit rate definition
R8<7:5>	BAND_SEL	R/W	000	Band selection
R8<2:0>	T_AUTO	R/W	000	Artificial wake-up （000，No artificial wake-up；001:1s；010:5s；011:20s；100:2min；101:15min；110:1h；111:2h）
R9<7>	BLOCK_AGC	R/W	0	Disables AGC
R10<4:0>	RSSI1	R		RSSI channel 1
R11<4:0>	RSSI2	R		RSSI channel 2
R12<4:0>	RSSI3	R		RSSI channel 3
R13<7:0>	F_WAKE	R		False wake-up register
R14<7>	RC_CAL_OK	R		Successful RC calibration
R14<6>	RC_CAL_KO	R		Unsuccessful RC calibration
R14<5:0>	RC_OSC_ TAPS	R		RC-Oscillator taps setting
R15<4>	LC_CAL_OK	R		LC-Oscillator working
R15<3>	LC_CAL_KO	R		LC-Oscillator not working
R16<7>	CLOCK_GEN _DIS	R/W	0	The Clock Generator output signal displayed on CL_DAT pin,R2<3:2>=11
R16<5>	RC_OSC_MIN	R/W	0	Sets the RC-oscillator to minimum frequency
R16<4>	RC_OSC_ MAX	R/W	0	Sets the RC-oscillator to maximum frequency
R16<2>	LC_OSC_ MUX3	R/W	0	Displays the resonance frequency of LF3P on DAT pin
R16<1>	LC_OSC_	R/W	0	Displays the resonance frequency of

	MUX2			LF2P on DAT pin
R16<0>	LC_OSC_ MUX1	R/W	0	Displays the resonance frequency of LF1P on DAT pin
R17<4:0>	CAP_CH1	R/W	00000	Capacitor banks on the channel1
R18<4:0>	CAP_CH2	R/W	00000	Capacitor banks on the channel2
R19<4:0>	CAP_CH3	R/W	00000	Capacitor banks on the channel3
R21<4>	GBOOST	R/W	0	The amplifier gain increases when 1 （R2<5> must be 1）
R21<3>	START_I_XTA L	R/W	0	Sets the oscillator current of the crystal oscillator
R21<2:0>	I_XTAL	R/W	000	Sets the current loss of the crystal oscillator
R22<3:0>	RC_OSC_ TAPS_EXTD	R	0000	The extended RC oscillator calibration control bit

6.2 SPI

This 4-wire interface is used by the Microcontroller to program the Si3933. The maximum clock operation frequency of the SPI is 6MHz.

Table 6-3 Serial Peripheral Interface (SPI) Pins

Name	Signal	Description
CS	Digital Input	Chip Select
SDI	Digital Input	Serial Data input for writing registers, data to transmit and/or writing addresses to select readable register
SDO	Digital Output	Serial Data output for received data or read value of selected registers
SCLK	Digital Input	Clock for serial data read and write

SDO is set to tristate if CS is low. In this way more than one device can communicate on the same SDO bus.

6.2.1 SDI Command Structure

To program the SPI the CS signal has to go high. A SPI command is made up by a two bytes serial command and the data is sampled on the falling edge of SCLK. The Figure 6-4 shows how the command looks like, from the MSB (B15) to LSB (B0). The command stream has to be sent to the SPI from the MSB (B15) to the LSB (B0).

Table 6-4 SDI Command Structure

Mode		Register Address / Direct Command						Register Data							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

The first two bits (B15 and B14) define the operating mode. There are three modes available (write, read, direct command) plus one spare (not used), as shown in Figure 6-5.

Table 6-5 SDI Command Structure Mode

B15	B14	Mode
0	0	WRITE
0	1	READ
1	0	NOT ALLOWED
1	1	DIRECT COMMAND

In case a write or read command happens the next 6 bits (B13 to B8) define the register address which has to be written respectively read, as shown in Figure 6-6.

Table 6-6 SDI Command Structure Register Address

B13	B12	B11	B10	B9	B8	Read/Write Register
0	0	0	0	0	0	R0
0	0	0	0	0	1	R1
0	0	0	0	1	0	R2
0	0	0	0	1	1	R3
0	0	0	1	0	0	R4
0	0	0	1	0	1	R5
0	0	0	1	1	0	R6
0	0	0	1	1	1	R7
0	0	1	0	0	0	R8
0	0	1	0	0	1	R9
0	0	1	0	1	0	R10
0	0	1	0	1	1	R11
0	0	1	1	0	0	R12

0	0	1	1	0	1	R13
0	0	1	1	1	0	R14
0	0	1	1	1	1	R15
0	1	0	0	0	0	R16
0	1	0	0	0	1	R17
0	1	0	0	1	0	R18
0	1	0	0	1	1	R19
0	1	0	1	0	0	R20
0	1	0	1	0	1	R21
0	1	0	1	1	0	R22

The last 8 bits are the data that has to be written respectively read. A CS toggle high-low-high terminates the command mode.

If a direct command is sent (B15-B14=11) the bits from B13 to B8 defines the direct command while the last 8 bits are omitted. Figure 6-7 shows all possible direct commands:

Table 6-7 List of Direct Commands

B13	B12	B11	B10	B9	B8	Direct Commands	Description
0	0	0	0	0	0	clear_wake	clears the wake state of the chip. In case the chip has woken up (WAKE pin is high) the chip is set back to listening mode.
0	0	0	0	0	1	reset_RSSI	resets the RSSI measurement.
0	0	0	0	1	0	Calib_RCosc	starts the trimming procedure of the internal RC oscillator.
0	0	0	0	1	1	clear_false	resets the false wake-up register. (R13<7:0>=00)
0	0	0	1	0	0	preset_default	resets all register in the default mode.
0	0	0	1	0	1	Calib_RCO_LC	calibration of the RC-oscillator with the external LC tank.

6.2.2 WRITE Mode

SPI is sampled at the falling edge of SCLK (as shown in the following diagrams).

A CS toggling high-low-high indicates the end of the WRITE command after register has been written. The following example shows a write command.

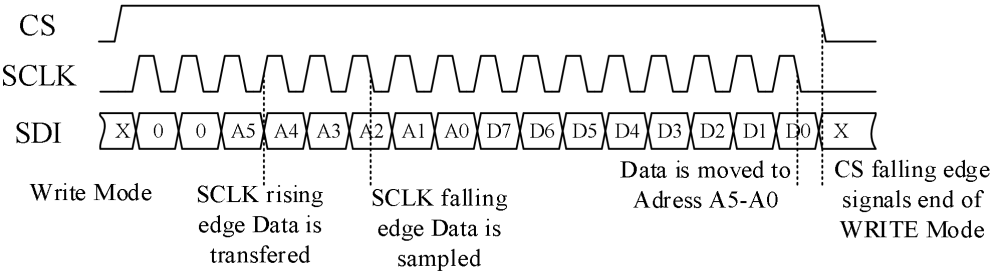


Figure 6-1 Writing of a Single Byte

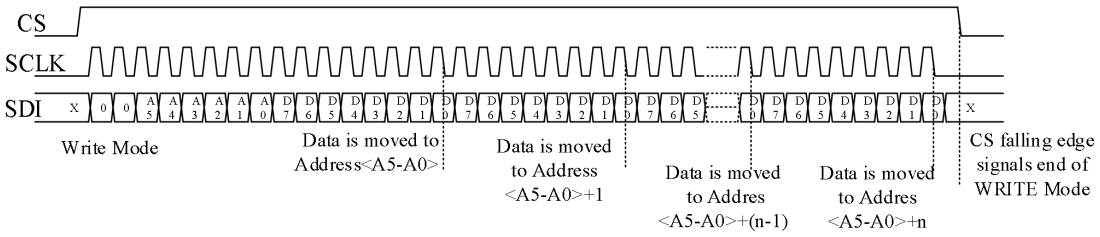


Figure 6-2 Writing of Register Data with Auto-Incrementing Address

6.2.3 READ Mode

Once the address has been sent through SPI, the data can be fed through the SDO pin out to the microcontroller.

A CS LOW toggling high-low-high has to be performed after finishing the read mode session.

To transfer bytes from consecutive addresses, SPI master has to keep the CS signal high and the SCLK clock has to be active as long as data need to be read.

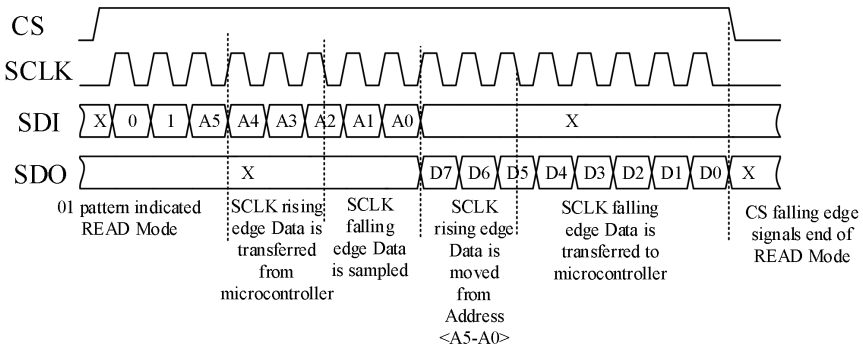


Figure 6-3 Reading of Single Register Byte

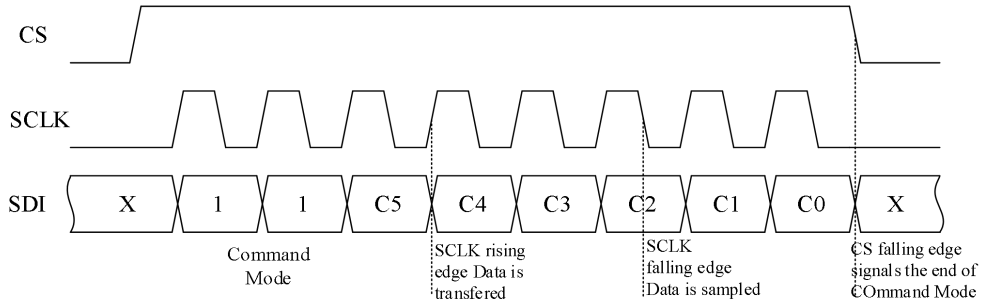


Figure 6-4 Send Direct Command Byte

6.2.4 SDI Timing

Table 6-8 SDI Timing Parameters

Symbol	Parameter	Min	Unit
TCSCLK	Time CS to Sampling Data	150	ns
TDCLK	Time Data to Sampling Data	100	ns
THCL	SCLK High Time	70	ns
TCLK	SCLK period	166	ns
TCLKCS	Time Sampling Data to CS down	150	ns
TCST	CS Toggling time	500	ns

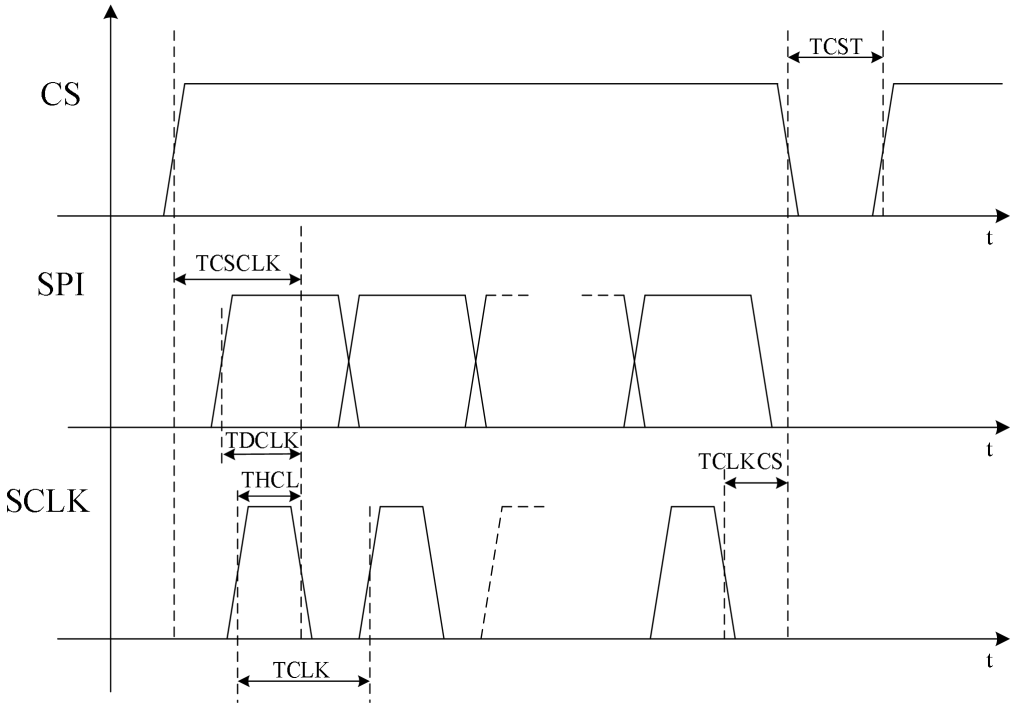


Figure 6-5 SDI Timing Diagram

7 Channel Amplifier

Each of the 3 channels consists of a variable gain amplifier (VGA) with automatic gain control (AGC) and a frequency detector. When the Si3933 is in listening mode (waiting for RF signal) the gain of all channel amplifiers is set to maximum. The frequency detector counts the zero crossing of the amplified RF signal to detect the presence of the wanted carrier. After the frequency detection is complete, the AGC starts working. The RSSI (Received Signal Strength Indicator) represents how strong the input signal is and it is the inverse representation of the gain of the VGA. In fact, if for example the input signal is very strong the AGC will reduce the gain of the VGA and the RSSI will be larger.

The Si3933 is a pretty wide LF wake-up receiver and can work between 15 kHz and 150 kHz. Once the carrier frequency has been chosen the user must set the amplifier working in the appropriate frequency band using the bits R8<7:5>, as described in the table 7-1.

It is possible to boost the gain of the amplifiers, as R2<5>=1. In case the lowest frequency band is used (15kHz-40 kHz) the gain boost is automatically enabled from the logic.

The amplifier gain continues to increase when R21<4>=1（The premise is R2<5> must be 1）.

It is possible to enable/disable individual channels, in case not all three channels are needed. This enables to reduce the current consumption by 1.6μA(typ.) per channel.

7.1 Frequency Detector

The frequency detection is based on a zero crossing counter and uses the Clock Generator as time base. The Clock Generator generates time windows equal to N times its period. The frequency detection is successful if in two consecutive time windows the zero threshold counter detects M zero crossing(Because the frequency of

the clock is determined by the carrier frequency, the number of the zero threshold in a time window is certain). N depends on the operating frequency band, as shown in the Table 7-1. M depends also on the operating frequency range,the frequency detection criteria can be tighter or more relaxed according to the setup described in R2<1:0> (see Table 7-2,7-3).

Table 7-1 Operating Frequency Range And N

R8<7>	R8<6>	R8<5>	N	Operating Frequency Range/kHz
0	0	0	4	95-150
0	0	1	6	65-95
0	1	0	10	40-65
0	1	1	18	23-40
1	1	1	14	15-23

Table 7-2 M for Frequency Detection in the Bands 23 kHz-150kHz

R2<1>	R2<0>	M
0	0	16±6
0	1	16±4
1	0	16±2
1	1	N.A.

Table 7-3 M for Frequency Detection in the Bands 15-23 kHz

R2<1>	R2<0>	M
0	0	8±3
0	1	8±2
1	0	8±1
1	1	N.A.

7.2 RSSI

The AGC starts working after the frequency detection. At the beginning the gain in the VGA is set to maximum and the AGC reduce it according to the received signal input level. The AGC needs maximum 35 carrier periods to settle, getting a stable RSSI.

The AGC can operate in two modes: AGC down only (R1<5>=0), AGC up and down (R1<5>=1).If the AGC down only mode is selected, the AGC can only decrease the gain for the whole duration of the data reception.In this mode the system holds the RSSI peak.When the AGC up and down mode is selected, the RSSI can dynamically follow the input signal strength variation in both directions.

The RSSI is available for all 3 channels at the same time and it is stored in 3 registers (R10<4:0>、R11<4:0>、R12<4:0>). Once the RSSI gets stable,the channel selector compares which channel receives the strongest RSSI and freezes the channels which have the smaller RSSI. From this time on the AGC is active only on the selected channel.

Both AGC modes (only down or down and up) can also operate with time limitation. This option allows AGC operation only in time slot of 256μs after the frequency detection (during carrier burst), then the RSSI is frozen till the wake-up or RSSI reset occurs (direct command clear_wakeup or reset_RSSI).

The RSSI is reset either with the direct command 'clear_wakeup' or 'reset_RSSI'. The 'reset_RSSI' command resets only the VGA setting but does not terminate wake-up frequency detection condition. This means that if the signal is still present the new AGC setting (RSSI) will appear not later than 35 LF carrier periods after the command was received. The AGC setting is reset during data receiving if for duration of 3 Manchester half symbols no carrier is detected.

In case the maximum amplification at the beginning is a drawback (e.g. in noisy environment) it is possible to set a smaller starting gain on the amplifier, according to the Table 7-4. In this way it is possible to reduce the false frequency detection.

Table 7-4 Bit Setting of Gain Reduction

R4<3>	R4<2>	R4<1>	R4<0>	Gain Reduction
0	0	0	0	0
0	0	0	1	N.A.
0	0	1	0 or 1	N.A.
0	1	0	0 or 1	-4dB
0	1	1	0 or 1	-8dB
1	0	0	0 or 1	-12dB
1	0	1	0 or 1	-16dB
1	1	0	0 or 1	-20dB
1	1	1	0 or 1	-24dB

In case the chip needs to deal with higher field strengths the antenna damper can be enabled(R1<4>=1). The antenna damper consists of internal resistors which can be connected in parallel to the external resonator as shown in Figure 7-1. The value of the resistor can be adjusted with the bits R4<5:4> as shown in Table 7-5. The shunt resistors degrade the quality factor of the external resonator by reducing the signal at the input of the amplifier. In this way the resonator sees a smaller parallel resistance (in the band of interest) which degrades its quality factor in order to increase the linear range of the channel amplifier (the amplifier doesn't saturate in presence of bigger signals).

Table 7-5 Antenna Damper Bit Setup

R4<5>	R4<4>	Shunt Resistor
0	0	1 kΩ
0	1	3 kΩ
1	0	9 kΩ
1	1	27 kΩ

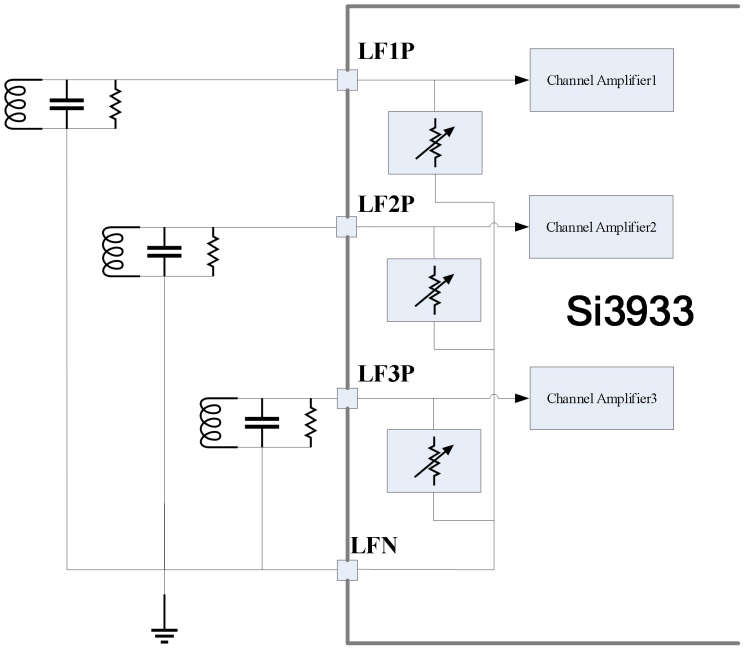


Figure 7-1 Antenna Damper

8 Demodulator / Data Slicer

As soon as the Si3933 detects successfully the frequency and the RSSI has got stable (not later than 35 LF carrier periods) the channel selector compares the RSSI on all active channels and connects the channel amplifier which has the biggest RSSI to the demodulator. The channel selector needs 32 RF carrier periods to take this decision. The output signal (amplified LF carrier) of selected channel is connected to the input of the demodulator.

A concept block diagram is shown in the Figure 8-1.The demodulator takes the signal to base-band and recovers two signals from the amplified RF signal; a fast and a slow envelop. Those two signals are fed to the data slicer, which is a comparator with programmable hysteresis. At the output of the data slicer are streamed the digital received bits as shown in Figure 8-2.

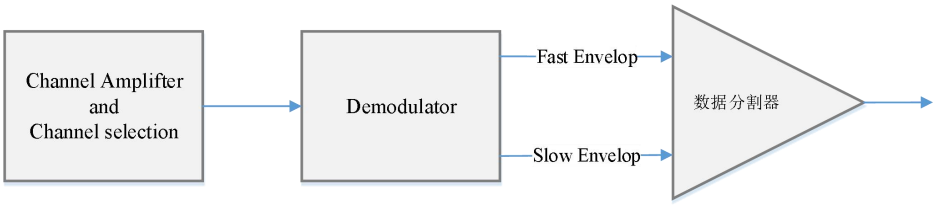


Figure 8-1 Concept Block Diagram

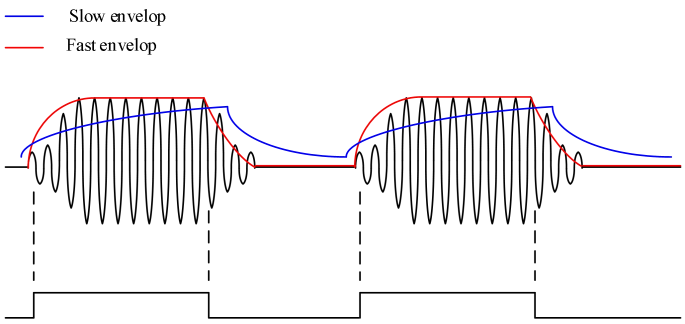


Figure 8-2 Envelop Detector Signals - Dynamic Threshold

The performance of the demodulator can be optimized according to bit rate and preamble length. On one hand the fast envelope's time constant (R3<2:0>) needs to be adjusted to the desired symbol rate as shown in Table 8-1. However, decreasing the fast envelope's time constant also means that more noise will be injected due to the

wider band. On the other hand, the slow envelop signal acts as an average of the incoming data. Therefore, the bigger its time constant is, the better will be the noise rejection. Yet, a bigger time constant of the slow envelop (R3<5:3>) requires a longer preamble in order to settle to the correct value. The minimum preamble length as a function of the slow envelope's settings is given in Table 8-2.

Table 8-1 Bit Setup of the Fast Envelope for Different Symbol Rates

R3<2>	R3<1>	R3<0>	Symbol Rate（Manchester Symbols/s）
0	0	0	4096
0	0	1	2184
0	1	0	1490
0	1	1	1130
1	0	0	910
1	0	1	762
1	1	0	655
1	1	1	512

Table 8-2 Minimum Required Preamble Lengths as Function of Slow Envelop Settings

R3<5>	R3<4>	R3<3>	Minimum Preamble Length（ms）
0	0	0	0.8
0	0	1	1.15
0	1	0	1.55
0	1	1	1.9
1	0	0	2.3
1	0	1	2.65
1	1	0	3
1	1	1	3.5

With the bits R3<7:6> it is possible to change the hysteresis on the data slicer comparator.If R3<7>=0,then the comparator hysteresis is 40mV else comparator hysteresis is 20mV. If R3<6>=0, then data slicer hysteresis on both edges else data slicer hysteresis only on positive edges.

The slow envelop signal (blue signal in Figure 8-2) represents the average of the demodulated signal, therefore acts as a reference signal for the data slicer. In case the chosen protocol has a duty cycle far away from 50% (for example in the NRZ protocol there can be several consecutive ones or zeros) the slow envelop signal

would not be a stable reference signal for the data slicer. In this case the data slicer can also work with an absolute threshold R1<7>=1), as shown in the Figure 8-3. It is even possible to reduce the absolute threshold in case the environment is not particularly noisy (R2<7>=1).

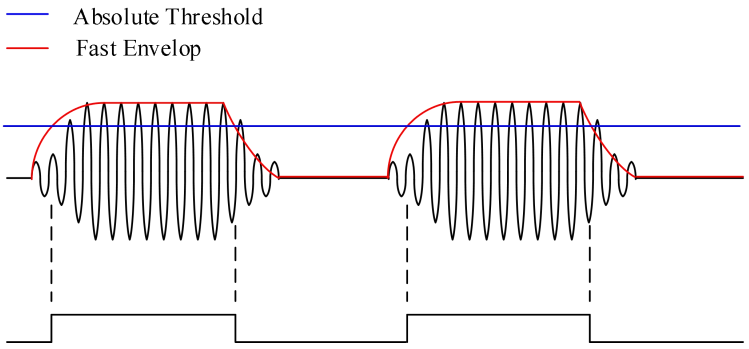


Figure 8-3 Envelop Detector Signals - Absolute Threshold

As the input signal may be damped due to physical influences of the transmitter environment, the symbol rate needs to be adapted (lowered) if absolute threshold is enabled to ensure a proper detection of the wake-up signal. The peak level of the signal should be reached within 1/3 of the symbol duration which is defined as two times the bit duration. The bit duration is defined in register R7<4:0> as a function of the Clock Generator periods,as shown in the Table 8-3.

Table 8-3 Bit Rate Setup

R7<4>	R7<3>	R7<2>	R7<1>	R7<0>	Bit Duration in RTC Clock Periods
0	0	0	1	1	4
0	0	1	0	0	5
0	0	1	0	1	6
0	0	1	1	0	7
0	0	1	1	1	8
0	1	0	0	0	9
0	1	0	0	1	10
0	1	0	1	0	11
0	1	0	1	1	12
0	1	1	0	0	13
0	1	1	0	1	14
0	1	1	1	0	15
0	1	1	1	1	16
1	0	0	0	0	17
1	0	0	0	1	18

1	0	0	1	0	19
1	0	0	1	1	20
1	0	1	0	0	21
1	0	1	0	1	22
1	0	1	1	0	23
1	0	1	1	1	24
1	1	0	0	0	25
1	1	0	0	1	26
1	1	0	1	0	27
1	1	0	1	1	28
1	1	1	0	0	29
1	1	1	0	1	30
1	1	1	1	0	31
1	1	1	1	1	32

9 Wake-Up Protocol And Manchester Decoder

9.1 Wake-Up Protocol

The Si3933 can support different protocols:

1.Frequency detection only (no pattern correlation);

2.Single pattern detection,include 16-bit pattern and 32-bits pattern;

3.Double pattern detection,include 16-bit pattern and 32-bits pattern.

The wake-up state can be terminated either by the host system (MCU) with the direct command ‘clear_wake’ sent over SPI or with a time-out option. In case the latter is used the host system (MCU) does not need to take any action to terminate the wake-up state and the chip is set back to listening mode automatically after a predefined time. It is possible to set the duration of the time-out with the register R7<7:5>, as shown in the Table 9-1.

Table 9-1 Timeout Setup

R7<7>	R7<6>	R7<5>	Time Out
0	0	0	disabled
0	0	1	50ms
0	1	0	100ms
0	1	1	150ms

1	0	0	200ms
1	0	1	250ms
1	1	0	300ms
1	1	1	350ms

In case the pattern correlation is disabled (R1<1>=0) the Si3933 wakes up upon detection of the carrier frequency only as shown in Figure 9-1. The minimum duration of the carrier burst in order to ensure that Si3933 wakes up and the RSSI is settled is specified in the Table 9-2. In addition the carrier burst does not have to be longer than 155 periods of the Clock Generator (Crystal oscillator or RCO or External Clock). As shown in the Figure 5-1, the Si3933 after the detection of the carrier goes directly from the Listening mode to Data receiving mode after settling the RSSI.

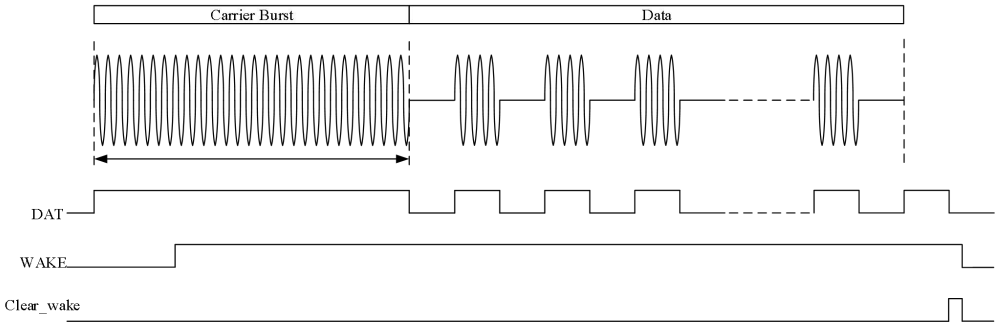


Figure 9-1 Wake-Up Protocol Overview Without Pattern Detection

Table 9-2 Minimum Duration of the Carrier Burst

Operating Frequency Range（kHz）	Minimum Duration of the Carrier Burst
95-150	16Tclk+16Tcarr
65-95	28Tclk+16Tcarr
40-65	52Tclk+16Tcarr
23-40	96Tclk+16Tcarr
15-23	92Tclk+8Tcarr

In case the pattern correlation is enabled (R1<1>=1) the Si3933 generates a wake-up interrupt if the wake-up protocol is fulfilled, as shown in the Figure 9-2. The communication protocol consists of a carrier burst, a preamble (0101010…) and the 16-bit pattern. In case the double pattern option is enabled (R1<2>=1) the 16-bit pattern has to be repeated 2 times consequentially (2 times the same pattern). The

signal on the WAKE pin goes high one bit after the end of the pattern and the data transmission can get started.

The minimum length for the carrier burst depends on the operating frequency range and is described in the Table 9-2.If the carrier burst is shorter than what has been specified in the Table 9-2, then the frequency detection is not guaranteed. In order to fulfill the protocol the carrier burst must be shorter than 155 periods of the clock generator (crystal oscillator or RCO or external clock). The carrier burst must be followed by a separation bit and at least 6 bits preamble (101010). The separation bit must last as half Manchester symbol. The preamble and the pattern cannot be longer than 30 symbols in sum in case 16-bit pattern detection is enabled and 46 symbols if the 32-bit pattern detection is enabled.

In case the ON/OFF option is enabled (R0<5>=1) the minimum duration of the carrier burst must be prolonged by the OFF time defined in the R4<7:6>.

Should the carrier burst be longer than what is defined in the Table 9-2 or the number of preamble bits longer than what has been specified above a false wake-up event might be recorded in the register R13<7:0>.

If the Scan Mode be enabled (R0<4>=1) the minimum duration of the carrier burst is defined in the Table 9-3.

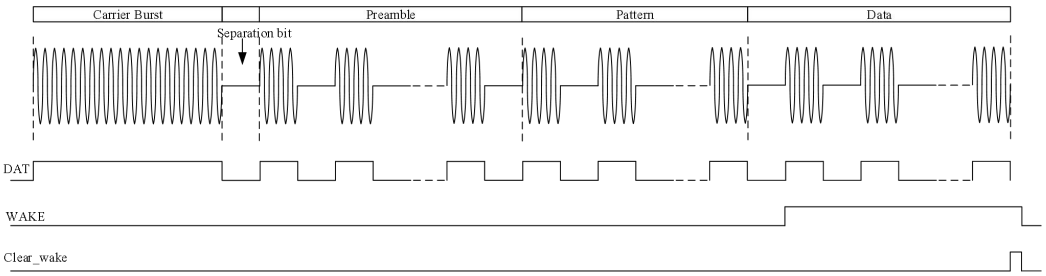


Figure 9-2 Wake-Up Protocol Overview if Pattern Detection is Enabled

Table 9-3 Minimum Duration of the Carrier Burst in Case the Scanning Mode is Enabled

Operating Frequency Range（kHz）	Minimum Duration of the Carrier Burst
95-150	80Tclk+16Tcarr
65-95	92Tclk+16Tcarr
40-65	180Tclk+16Tcarr
23-40	224Tclk+16Tcarr
15-23	220Tclk+8Tcarr

9.2 Correlator

In order to prevent that the Si3933 wakes up the host system (MCU) from noise or disturbers the internal correlator checks that the bit sequence delivered from the data slicer corresponds to stored pattern. The wanted pattern can be stored in the registers R5<7:0> and R6<7:0>. The data correlation is performed only if the correlator is enabled (R1=1) and can start only after frequency detection.

The pattern correlation is successful (Wake goes high) only if the bits sequence (pattern) and its timing (duration of the single bit) matches.

The Si3933 can correlate the incoming pattern without the help of an external unit (MCU). The chosen pattern must be Manchester encoded. In the Manchester code each “Symbol” is defined by a transition (high-to-low for 1 and low-to-high for 0), therefore consists of two “bits”. In the Figure 9-3 it is shown, as an example, how the encoding technique works. In this sequence a simple message made up by 3 symbols (1 0 1) is Manchester encoded. In the Manchester encoded bit stream there can not be three consecutive zeros or ones (in each symbol there is always a transition). This helps the receiver to recover the clock.

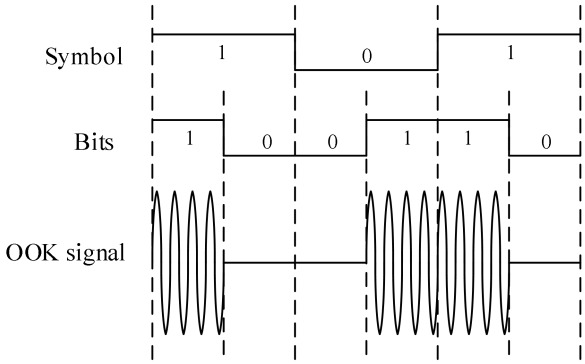


Figure 9-3 Manchester Encoding

The user can define the pattern to correlate in the registers R5<7:0>and R6<7:0> and can decide whether the stored pattern is a bit representation (16 Manchester bits corresponds to 8 Symbols) if R0<7>=0 or the symbol representation (16 symbols corresponds to 32 bits) of the pattern if R0<7>=1. The number of different pattern is 2^SYM, where SYM is the number of Manchester symbols. In case the R5 and R6

represent the bit sequence of the pattern there are 256 different possible combinations, while in case they are the symbol representation there are 65536 different patterns.

9.3 False Wake-Up Register

The wake-up strategy in the Si3933 is based on 2 steps: 1. Frequency Detection: In this phase the frequency of the received signal is checked. 2. Pattern Correlation: Here the pattern is demodulated and checked whether it corresponds to the valid one.

If there is a disturber or noise capable to overcome the first step (frequency detection) without producing a valid pattern, then a false wake-up call happens. Each time this event is recognized a counter is incremented by one and the respective counter value is stored in a memory cell (false wake-up register). Thus, the microcontroller can periodically look at the false wake-up register, to get a feeling how noisy the surrounding environment is and can then react accordingly (e.g. reducing the gain of the LNA during frequency detection, set the Si3933 temporarily to power down etc.), as shown in the Figure 9-4. The false wake-up counter is a useful tool to quickly adapt the system to any changes in the noise environment and thus avoid false wake-up events.

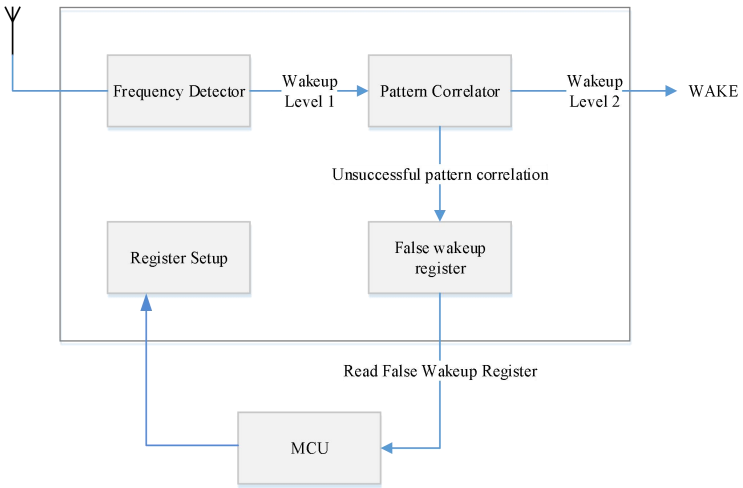


Figure 9-4 Concept of the False Wake-Up Register Together with the System

9.4 Manchester Decoder and Clock Recovery

In case the Manchester decoder is enabled (R1<3>=1) the Si3933 decodes the

incoming Manchester bits automatically and the Manchester decoded data are displayed on the DAT pin and the Manchester recovered clock on the CL_DAT. The data coming out from the DAT pin are stable on the rising edge of the CL_DAT clock, as shown in Figure 9-5.

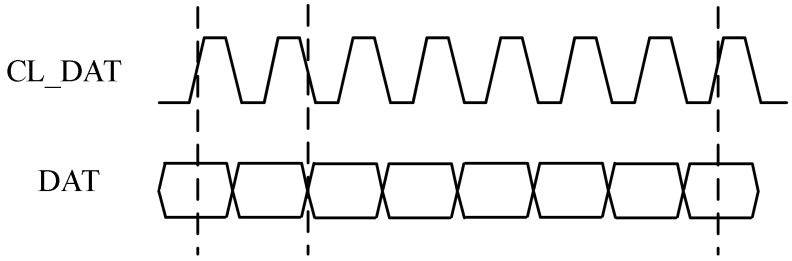


Figure 9-5 Synchronization of Data with the Manchester Recovered Clock

In case a Manchester timing violation happens, the signal on SPO goes high for a duration of 4 periods of internal clock (either crystal oscillator or RCO or external clock).

In case the Manchester decoder is disabled (R1<3>=0), the Manchester undecoded data are displayed on the DAT pin.

10 Clock Generator

10.1 Overview

The Clock Generator can be based on a crystal oscillator (R1<0>=1), the internal RC-oscillator (R1<0>=0), or an external clock source (R1<0>=1). The crystal oscillator has higher precision of the frequency with higher current consumption and needs three external components (crystal plus two capacitors). The RC-oscillator is completely integrated and can be calibrated to increase its precision. Should a digital clock already be available it can be applied directly to the XOUT pin (XIN to VDD).

Regardless which clock generator is chosen, the frequency of the Clock Generator must be set according to the carrier frequency. Table 10-1 shows the dependency of the Clock Generator frequency from the carrier frequency and operating frequency band.

Table 10-1 Clock Generator Frequency vs Frequency Band

Carrier Frequency（kHz）	Clock Generator Frequency
95-150	$f = f_{carr} \times \frac{1}{8}$
65-95	$f = f_{carr} \times \frac{3}{8}$
40-65	$f = f_{carr} \times \frac{5}{8}$
23-40	$f = f_{carr} \times \frac{9}{8}$
15-23	$f = f_{carr} \times \frac{14}{4}$

It is possible to display the frequency of the clock generator on the CL_DAT pin writing R2<3:2>=11 and R16<7>=1.

10.2 Crystal Oscillator

In case the user decides to use the Crystal Oscillator as reference clock a 32.768kHz quartz can be used in case the tolerance setting for the frequency detection

is relaxed (R2<1:0>=00). Should this not be the case, then Table 10-2 shows how the frequency of the quartz has to be chosen.

If the Si3933 works in the bandwidth 23-40kHz, then it is recommended not to use the XTAL oscillator to avoid any coupling between the input antennas and the quartz.

Table 10-2 Characteristics of XTAL

Parameter	Conditions	Min	Typ	Max	Unit
Crystal motional resistance		-	-	60	K Ω
Minimum Frequency	For 32.768kHz crystal	-	25	-	kHz
Typical Frequency		-	32.768	-	kHz
Maximum Frequency		-	45	-	kHz
Start-up Time	Crystal dependent	-	1	-	s
Calibration time		45	50	55	%
Current consumption		-	560	-	nA

10.3 RC-Oscillator

Table 10-3 Characteristics of RCO

Parameter	Conditions	Min	Typ	Max	Unit
Calibration time	Periods of reference clock	65	-	-	cycles
Current consumption		-	730	-	nA

In case the pattern detection and the Manchester decoder are not enabled (R1<1>=0 and R1<3>=0) the calibration on the RC-oscillator is not needed. Should this not be the case, the RC-oscillator has to be calibrated. The calibration of the RC-oscillator can be done in two different ways:

1. Over SPI, the host system (MCU) has to be able to provide 65 clock pulses of a reference clock. In this case the host has to have a precise reference clock (quartz, resonator etc.).

2. Using the internal calibration procedure based on the antenna resonator. Using this calibration method the RC-oscillator is automatically trimmed to the proper frequency, according to the operating frequency band. The precision of the calibration depends on the tolerances of the resonator of the first channel (LC connected to

LF1P).

RC-Oscillator: Calibration via SPI. The calibration gets started with the Calib_RCosc direct command. Since no non-volatile memory is available on the chip, the calibration must be done every time after battery replacement. Since the Clock Generator defines the time base of the frequency detection, the selected frequency depends on the carrier frequency. The choice of the reference clock frequency delivered by the host (MCU) is the same as the choice of the frequency in case the crystal oscillator is used and it is shown in the Table 10-1.

To trim the RC-Oscillator, set the chip select (CS) to high before sending the direct command Calib_RCosc over SPI. Then 65 digital clock cycles of the reference clock (e.g. 125kHz/4=31.25kHz) have to be sent on the clock bus (SCLK), as shown in Figure 10-1. After that the signal on the chip select (CS) has to be pulled down.

The calibration is effective after the 65th reference clock edge and it will be stored in a volatile memory. In case the RC-oscillator is switched OFF or a power-on-reset happens (e.g. battery change) the calibration has to be repeated.

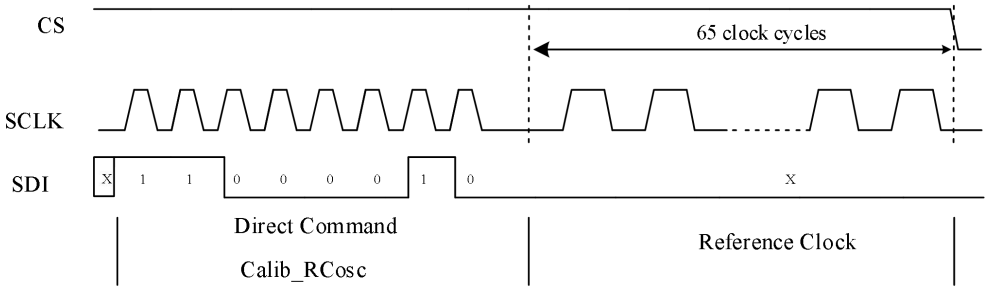


Figure 10-1 RC-Oscillator Calibration via SPI

RC-Oscillator: Self Calibration. This procedure uses the LC-tank (antenna) connected to the channel 1 (LF1P) not as antenna but as resonator for an oscillator. The internal LC oscillator is therefore connected through a multiplexer to the external tank.

The LC-oscillator generates a clock which corresponds to the resonance frequency of the LC-tank. In a typical application the user designs the external resonators such to set the resonance frequency of the external LC-tank as close as

possible to the carrier frequency. The mathematical relation between the oscillation frequency and the LC time constant is: $f_{LC} = \frac{1}{2\pi\sqrt{LC}}$

To start the calibration the direct command Calib_RCO_LC must be sent over the SPI and as soon as the bit R14<7> is high, the RC-oscillator will be calibrated. The calibrated frequency of the RC-oscillator depends on the carrier frequency and is automatically set to better perform the frequency detection, according to the Table 10-1.

10.4 External Clock Source

To clock the Si3933 with an external signal, the external clock generator (R2<6>=1) and the crystal oscillator (R1<0>=1) need to be enabled. As shown in the Figure 1-3 the clock can be directly applied on the pin XOUT while the pin XIN must be connected to VDD. The clock characteristics are summarized in Table 10-4.

Table 10-4 Characteristics of External Clock

Parameter	Min	Typ	Max	Unit
Low level	0	-	0.1*VCC	V
High level	0.9*VCC	-	VCC	V
Rise-time	-	-	3	μs
Fall-time	-	-	3	μs

11 Antenna Tuning

The Si3933 offers the possibility to implement a fine antenna tuning. A block diagram shows how the tuning can be implemented with the help of the host system (MCU).

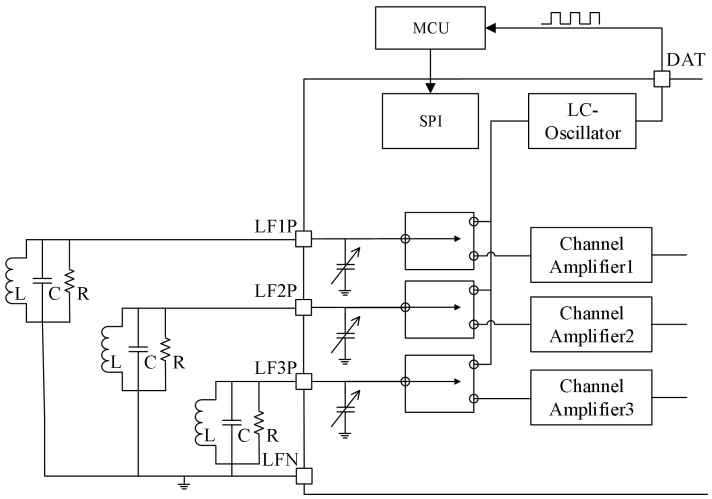


Figure 11-1 Tuning Implementation

Each of the three antennas can be tuned with the internal capacitor banks. The capacitor can be connected or disconnected (adding or subtracting parallel capacitance to the external resonator) through registers R17<4:0>, R18<4:0> and R19<4:0>.The capacitance tuning range is 0~ 31pF and step into 1pF.

Table 11-1 Parallel Tuning Capacitance on the LF1P

R17	Capacitance on LF1P
R17<0>=1	Adds 1pF
R17<1>=1	Adds 2pF
R17<2>=1	Adds 4pF
R17<3>=1	Adds 8pF
R17<4>=1	Adds 16pF

Table 11-2 Parallel Tuning Capacitance on the LF2P

R18	Capacitance on LF2P
R18<0>=1	Adds 1pF
R18<1>=1	Adds 2pF
R18<2>=1	Adds 4pF
R18<3>=1	Adds 8pF
R18<4>=1	Adds 16pF

Table 11-3 Parallel Tuning Capacitance on the LF3P

R19	Capacitance on LF3P
R19<0>=1	Adds 1pF
R19<1>=1	Adds 2pF
R19<2>=1	Adds 4pF
R19<3>=1	Adds 8pF
R19<4>=1	Adds 16pF

The Three channels can be tuned separately. The host system (MCU) has to connect the LC-oscillator to the antenna to measure the resonance frequency on the pin DAT. The host should measure the frequency on this pin and just changing register setting fine tune it to get it as close as possible to the nominal value of the carrier frequency. With the bits R16<2:0> it is possible to connect the LC-oscillator to the three different antennas.

Table 11-4 LC Display Channel Selection

Register bit	Parameter	Read-write type	Default	Description
R16<2>	LC_OSC_ MUX3	R/W	1’b0	Output LF3P resonance frequency at the DAT pin
R16<1>	LC_OSC_ MUX2	R/W	1’b0	Output LF3P resonance frequency at the DAT pin
R16<0>	LC_OSC_ MUX1	R/W	1’b0	Output LF3P resonance frequency at the DAT pin

12 Package Drawings

12.1 TSSOP Package

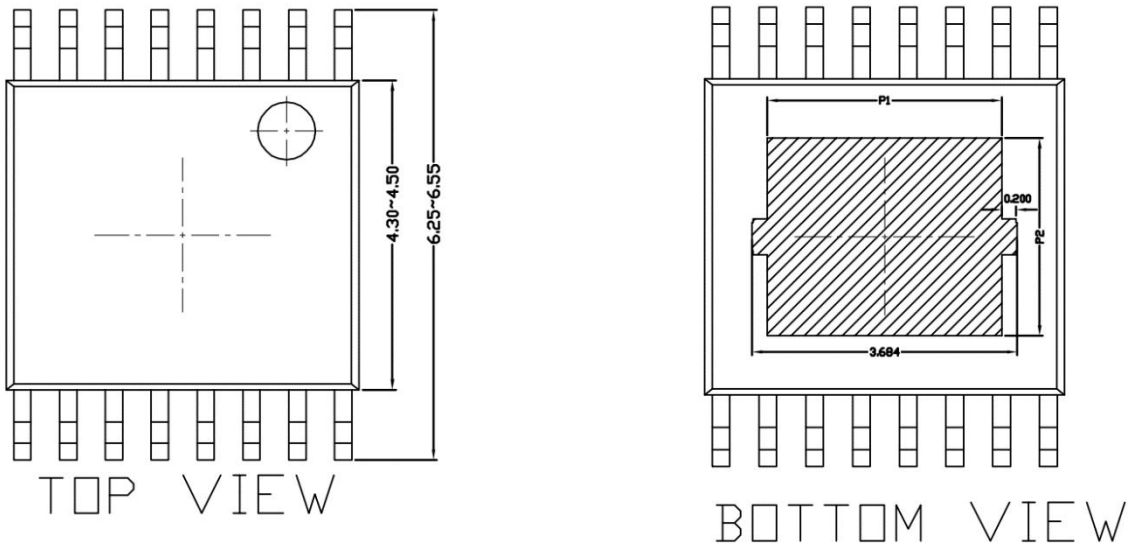
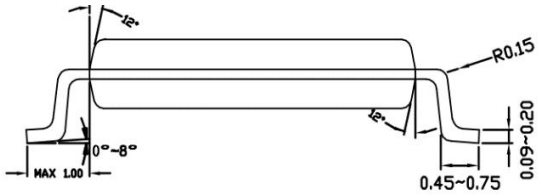


Figure 12-1 Si3933 TSSOP-16 Package Drawing



NOTES:

1) LEAD FRAME : C7025(THICKNESS :0.127MM)
2) LEAD FINISH : SOLDER PLATED
3) BOTH PACKAGE LENGTH AND WIDTH DO NOT INCLUDE FLASH.
4) FORMED LEAD SHALL BE PLANAR WITH RESPECT TRO ONE ANOTHER WITHIN 0.10(0.004)
5) CONTROLLING DIMENSION : MM .
6)UNREMOVED FLASH BETWEEN LEADS&PACKAGE END FLASH SHALL NOT EXCEED 0.15MM FROM BOTTOM BODY PER SIDE.
7)EDP PACKAGE:EXPOSED PAD SIZE P1&P2 ARE VARIATIONS DEPENDING ON DEVICE FUNCTION(DIE PADDLE SIZE).

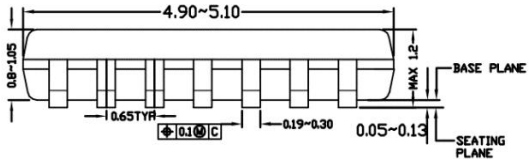
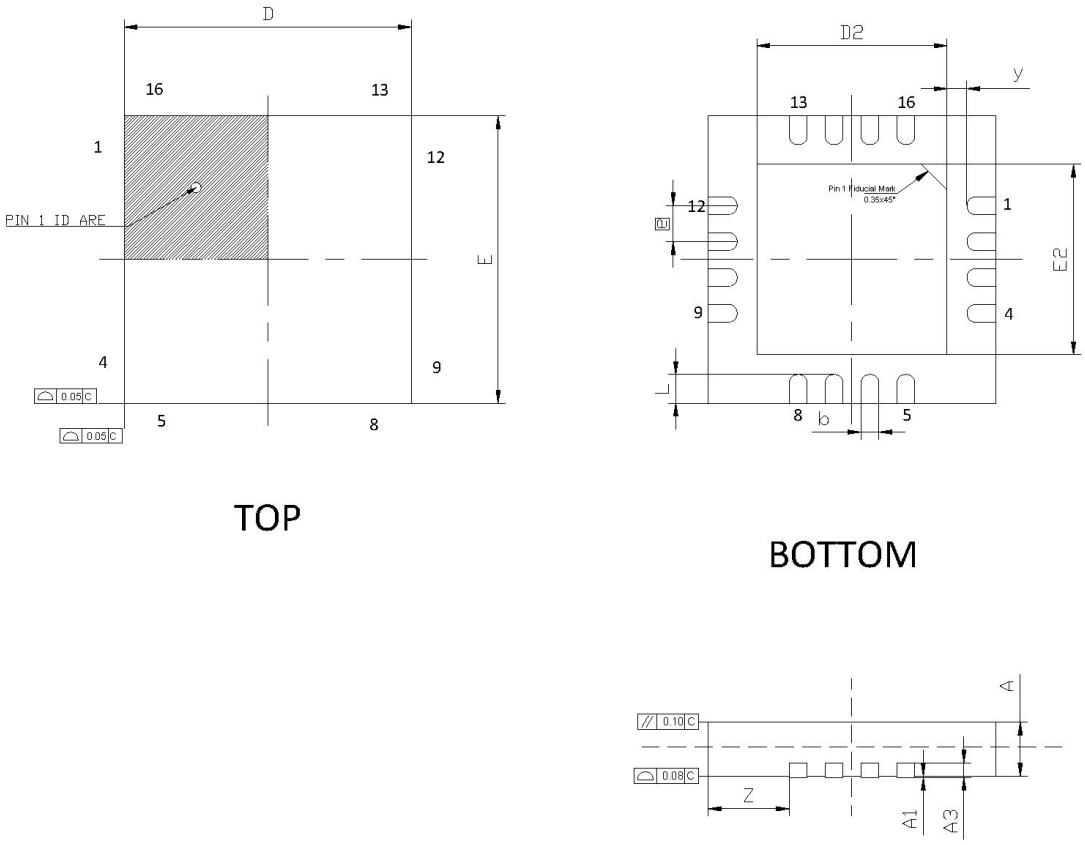


Table for TSSOP-EP/16 of exposed die pad size

Pad Size	Symbol	Min	Nom	Max
120*140	P1	3.156	3.256	3.356
	P2	2.648	2.748	2.848

12.2 QFN Package



Dimensions

Unit	D	E	D2	E2	A	A1	A3	b	e	K	L	y	Z
mm	4.10 (4.00) 3.90	4.10 (4.00) 3.90	2.75 (2.65) 2.55	2.75 (2.65) 2.55	0.80 (0.75) 0.70	0.05 (0.02) 0.00	0.203 REF	0.30 (0.25) 0.20	0.50 BSC	-	0.45 (0.40) 0.35	0.275 REF	1.125 REF

Notes

1. All Dimensions are in Millimeters.
2. Dimensions Do Not include Burrs, Mold Flash, and Tie-bar Extrusions.

Figure 12-2 Si3933 QFN-16 Package Drawing

13 Typical application principle diagram

13.1 TSSOP Package

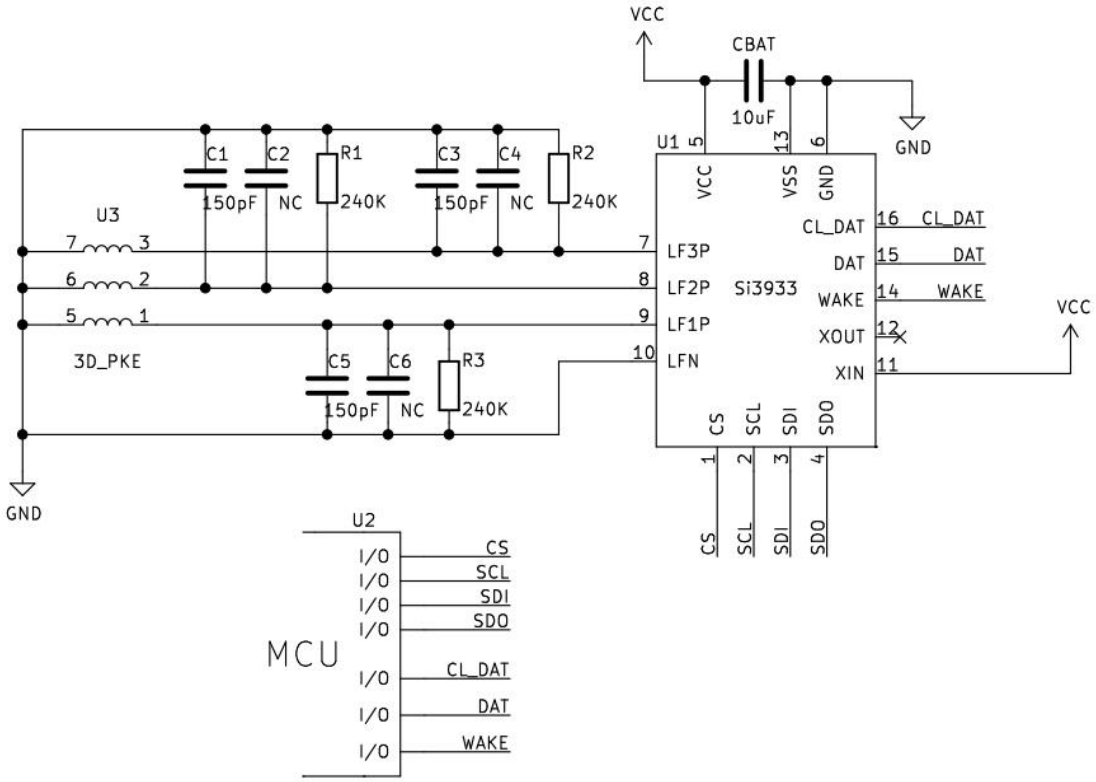


Figure 13-1 Typical application principle diagram (TSSOP-16 Package)

13.2 QFN Package

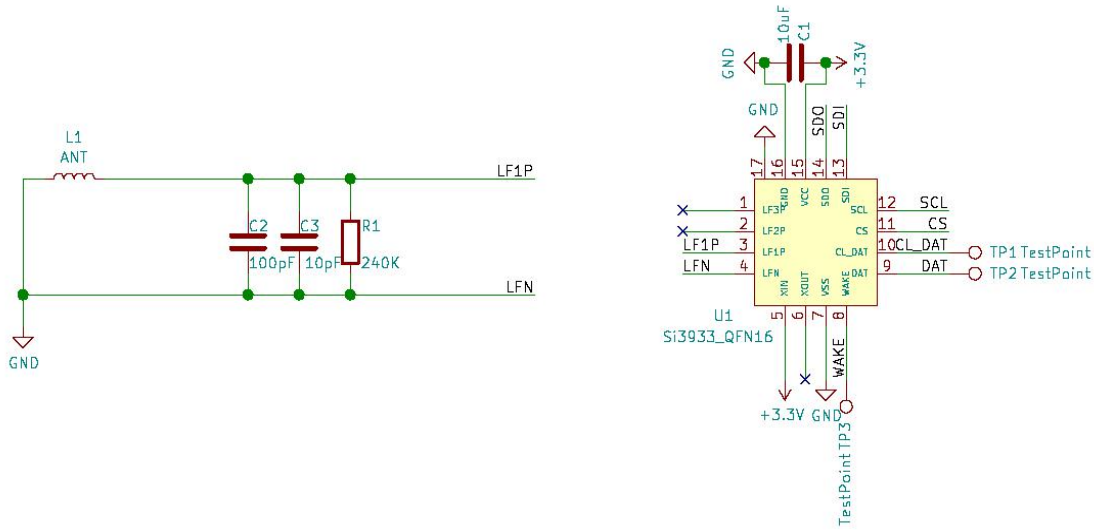


Figure 13-2 Typical application principle diagram (QFN-16 Package)

14 Version information

Version	Modified date	Modified content
V1.0	2023/11/13	First draft

15 Order Information

Package marking

Si24R1 ABBCDEE

Si24R1: chip code

A: package date code, 5 represents year 2020

BB: week of sending out processing, 42 represents in the year A the 42th week

C: package factory code, A、HT、NJ or WA, can also abbreviated as A、H、N or W

D: test factory code, A、Z or H

EE: production batch code

Table 15-1 Order information sheet

order code	package	container	minimum
Si3933-Sample		Box/Tube	5
Si3933	TSSOP-16	Tape and reel	4K
Si3933	QFN-16	Tape and reel	4K

16 Technical Support and Contact Information

Nanjing Zhongke Microelectronics Co., LTD Technical Support Center
Phone: 025-68517780
Address: Room 201, Building B, Research Zone 3, Xuzhuang Software Park, Xuanwu District, Nanjing, Jiangsu, China
Website: http://www.csm-ic.com

Sales and Marketing
Phone: 13645157034, 13645157035
Email: sales@csmic.ac.cn

Technical Support
Phone: 13645157034
Email: supports@csmic.ac.cn