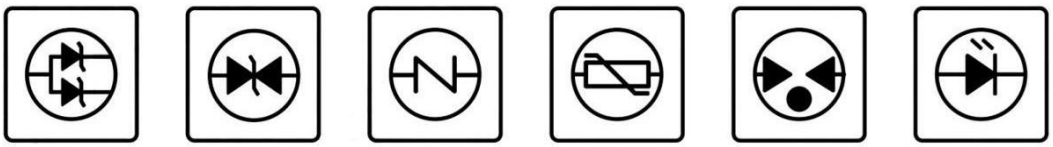
MSKSEMI 美森科
SEMICONDUCTOR



MS8541

Product specification

GENERAL DESCRIPTION

The MS8541 is a CMOS operational amplifier that uses the proprietary auto-calibration techniqu to simultaneousl provide very low offset voltage,near-zero drift over time and temperature.This miniature,high-precision,low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 200mV beyond the rails,and rai-to-rail output that swings within 50mV of the rails, single or dual supplies as low as 2.1V(±1.05V)and up to 5.5V(±2.75V)can be used.This device is optimized for low voltage,single supply operation.

The MS8541 offers excellent CMRR without the crossover associated with traditional complementary input stages.This d esign results in superior performance for driving analog-to-digital converters (ADC)without degradation of differential lin earity.

The MS8541 is available in the 5-pin SOT-23-5 and SC70-5 packages,and specified for operation from -25℃ to 125℃.

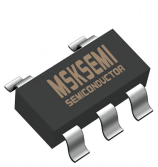
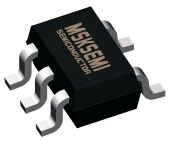
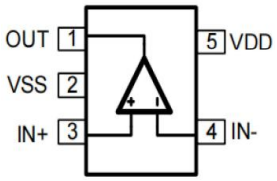
FEATURES

- VDD range:2.1V to 5.5V
- Low Ofset Voltage:0.5mV (Typical)
- Low Drift:0.65μV/C(Typical)
- Low Noise
- Quiescent Current:28μA
- Rail to Rail Input/Output
- MicroSize Packages:SC70-5 and SOT23-5

Applications

- Transducers
- Temperature Measurement
- Electronic Scales
- Medical instrumentation
- Handheld Test Equipment

Reference News

PACKAGE OUTLINE		PIN CONFIGURATION	Marking	
				
SOT-23-5	SC70-5	SOT-23-5/SC70-5	SOT-23-5	SC70-5

PIN DESCRIPTION

Pin Name	Pin Numbel	Description
IN+	3	Noninverting inpu
VSS	2	Negative(lowest)power supply
IN-	4	Inverting inpu
OUT	1	Output
VDD	5	Positive (highest)power supply

REEL SPECIFICATION

P/N	PKG	QTY
MS8541ARTZ-REEL	SOT-23-5	3000
MAD8541AKSZ-REEL7	SC70-5	3000

SIMPLIFIED SCHEMATIC

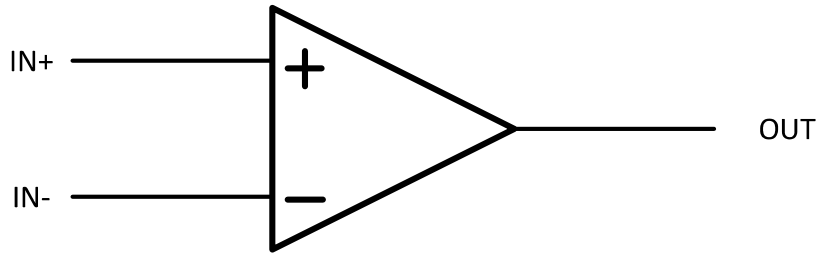


Figure 1.Simpliied Schematic

ABSOLUTE MAXIMUM RATINGS

Thermal Resistance 0 Jc……..…130°C/W
Supply Voltage…….2.1to 5.5V
Signal Input Terminals Voltage…-0.1 to (V+)+0.1V
Operating Junction Temperature……150℃
Operating Temperature Range……-25°C to 85°C
Storage Temperature ……..-65°℃ to 150℃

ELECTRICAL CHARACTERISTICS

(At TA=25° C, RL=10k connected to Vs/2, and Vour=Vs/2, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	Vs=±2.5V	-3	0.5	3	mV
nput Offset Voltage Drift	TA=-25° ℃ to 125° ℃		0.65		μV/℃
Power Supply Rejection Ratio	Vs =2.1V to 5.5V TA=-25℃ to 125 ℃	80	90		dB
Input Bias Curren	TA=25℃		2.0		pA
Input Offset Current			1.0		pA
Common-mode Voltage Range		(V-)-0.1		(V+)+0.1	V
Common-mode Rejection Ratio	V-)-0.1<Vcm<(V+)+0.1 TA=-25℃ to 125℃	80	95		dB
Open Loop Voltage Gain	(V-)+100mV<Vo<(V+)-100mV, RL=10k TA=-25° ℃ to 125℃	80	100		dB
Gain-bandwidth product	CL=120pF		1.5		MHz
Slew Rate	G=+1		1.2		V/μs
Specified Voltage Range		2.1		5.5	V
Quiescent Current			28	40	μA
Operating Temperature Range		-25		85	℃
Storage Temperature Range		-65		150	℃

TYPICAL PERFORMANCE CHARACTERISTICS

(At T_A = 25°C, V_S=5V, C_L=20pF, unless otherwise noted.)

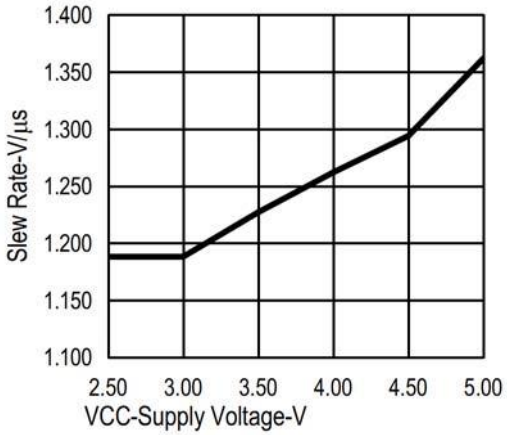


Figure 2. Slew Rate vs Supply Voltage

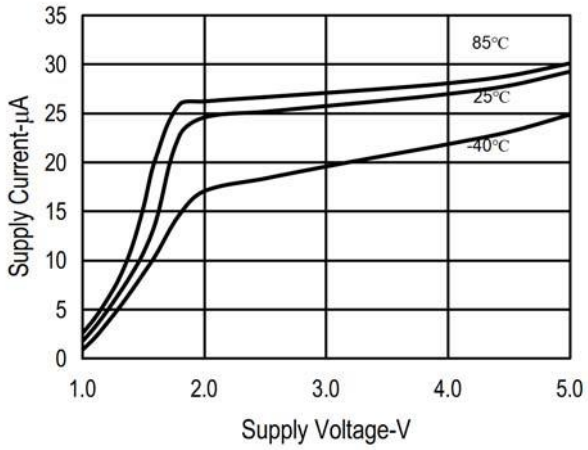


Figure 3. Supply Current vs Supply Voltage

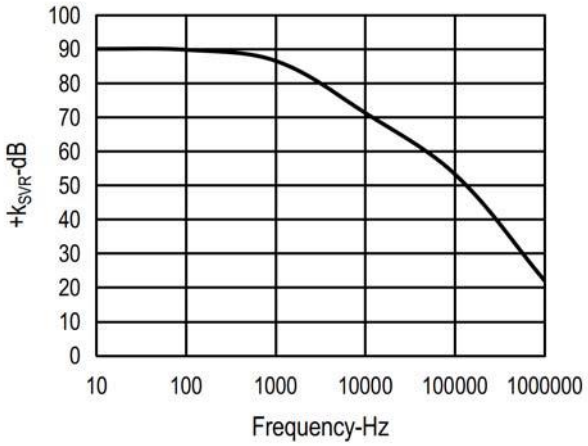


Figure 4. +kSVR vs Frequency

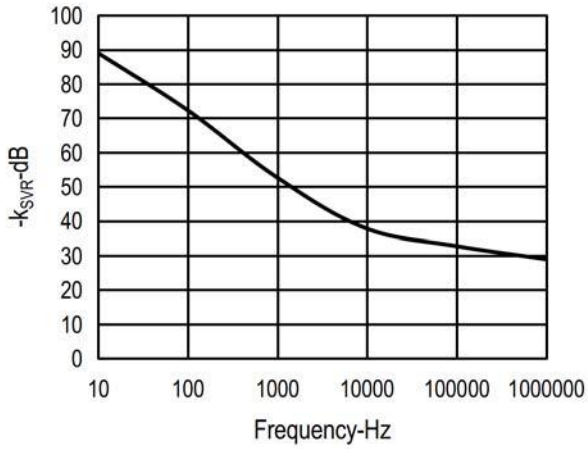


Figure 5. -kSVR vs Frequency

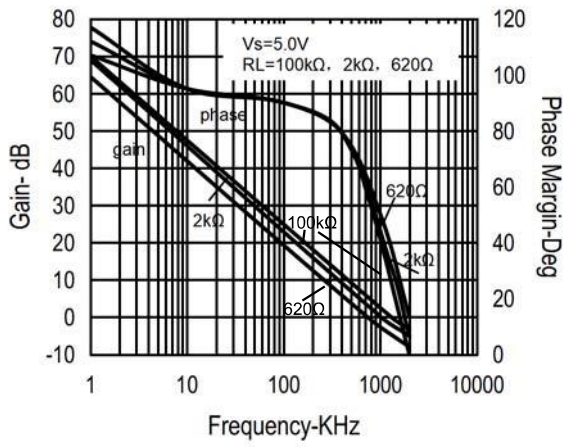


Figure 6. Frequency Response vs Resistive Load

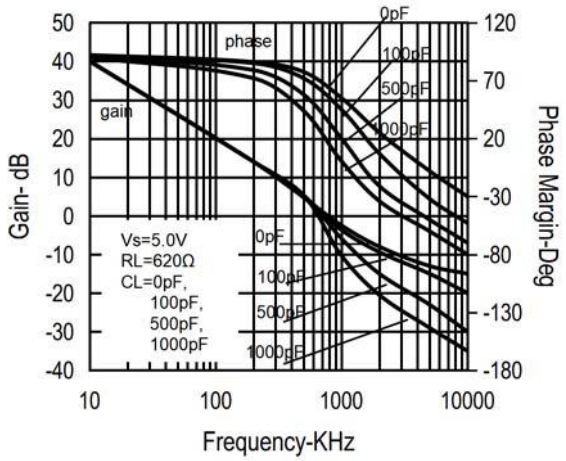


Figure 7. Frequency Response vs Capacitive Load

TYPICAL PERFORMANCE CHARACTERISTICS

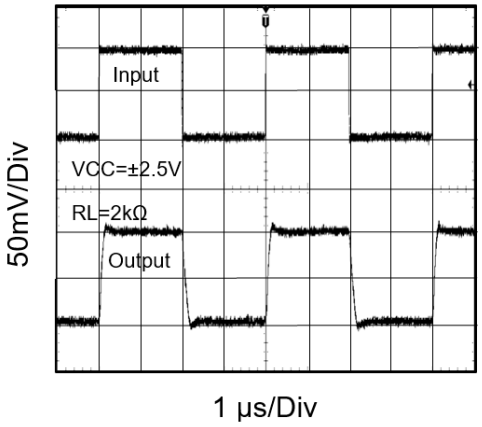


Figure 8. Noninverting Small-Signal Pulse Response

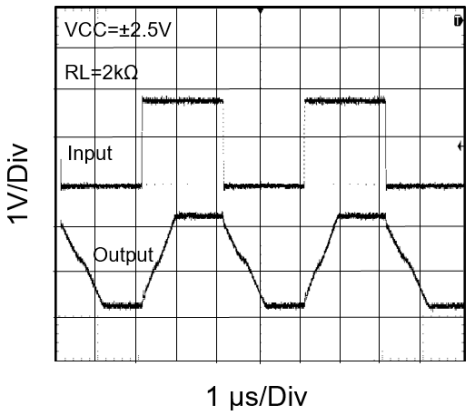


Figure 9. Noninverting Large-Signal Pulse Response

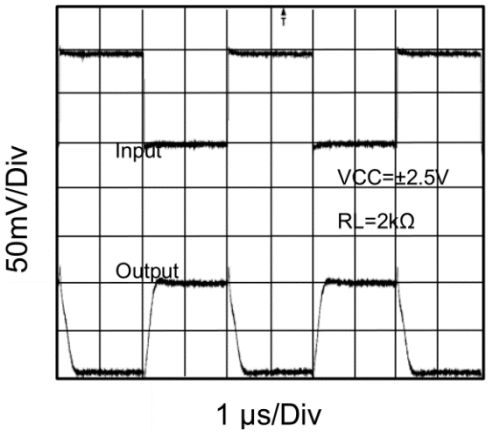


Figure 10. Inverting Small-Signal Pulse Response

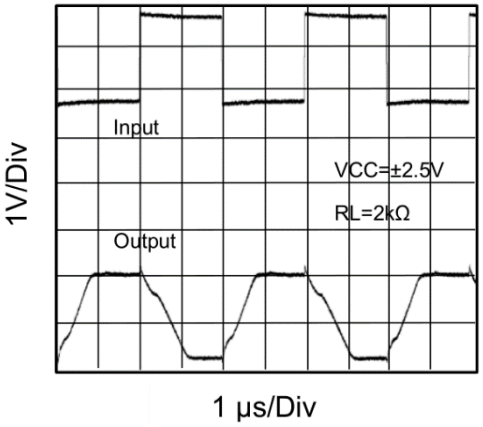


Figure 11. Inverting Large-Signal Pulse Response

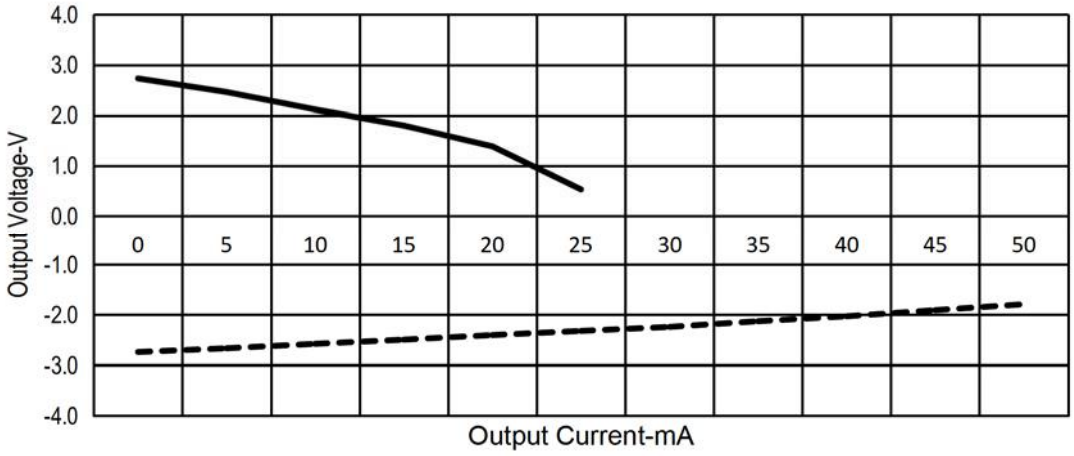


Figure 12. Output Voltage vs Output Current

FUNCTIONAL DESCRIPTION

Operating Voltage

The MS8541 devices are fully specified and ensured for operation from 2.1V to 5.5 V.In addition,many specifications apply from -25℃to 125℃. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics graphs.

Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal.The MS8541 device has a 1.5-MHz unity-gain bandwidth.

Slew Rate

The slew rate is the rate at which an operational amplifier canchange its output when there is a change on the input.The MS8541 devices have a1 .2-V/μ s slew rate.
MS8541 is characterized toperform with this.technique;the recommended resistor value is approximately 20 k.

Device Functional Modes

The MS8541 device has a single functional mode. The device is powered on as long as the power supply voltage is between 2.1V(±1.05V)and 5.5V(±2.75V)

APPLICATIONS INFORMATION

The MS8541 is a unity-gain stableprecision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal.Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins.In most cases, 0.1μF capacitors are adequate.

Typical Application

Figure 13 shows a simple circuit to convert a single-ended input into differential output.The MS8541 could be used to build this circuit.The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage,VouT+. The second amplifier inverts the input and adds a reference voltage to generate Vour-.Both Vour+ and Vour-range from 0 .5 to 2 V.The diference, VDIFF,is the difference between Vour+and VouT-.

Detailed Design Procedure

Linearity over the input range is key for good dcaccuracy. The common mode input range and the outputswing limitations determine the linearity.In general,anamplifier with rail-to-rail input and output swing isrequired.Bandwidth is a key concern for this design.Because MS8541 has a bandwidth of 1MHz,thiscircuit will only be able to process signals with frequencies ofless than 1 MHz.

Because the transfer function of Vour-is heavily reliant on resistors(R1,R2,R3,and R4),use resistors with low tolerances to maximize performance and minimize error.This design used resistors with resistance values of 36 k with tolerances measured to be within 2%.If the noise of the system is a key parameter,the user can select smaller resistance values (6 k or lower)to keep the overall system noise low.This ensures that the noise from the resistors is lower than the amplifier noise.

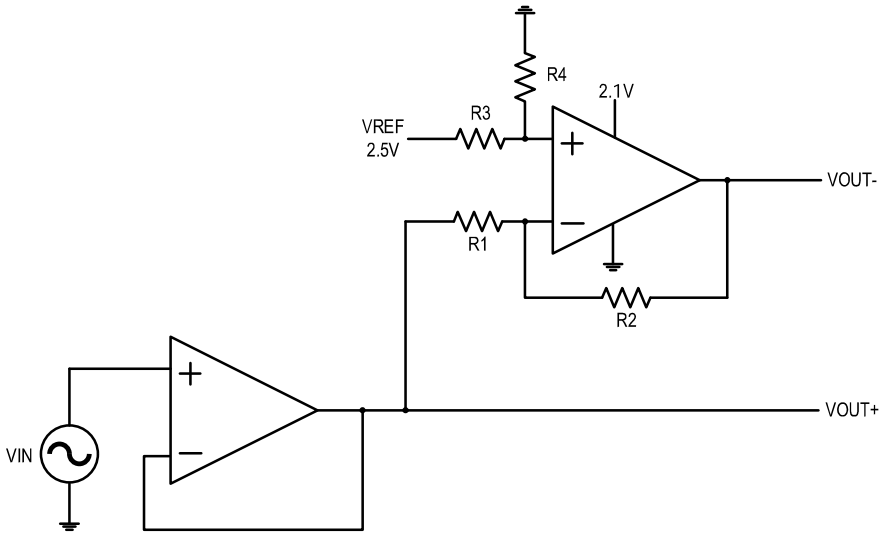
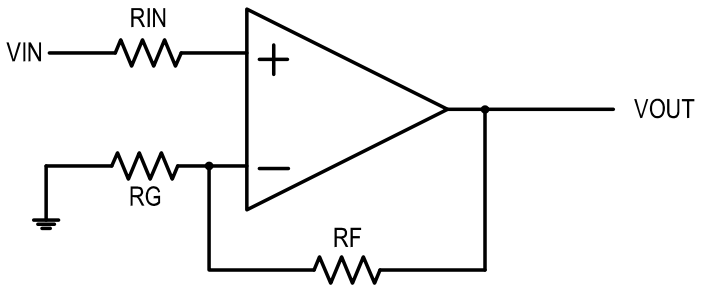


Figure 13. Schematic for Single-Ended Input to Differential Output Conversion

LAYOUT

Use good PCB layout practices for best operational performance of the device, including:

- Keep the length of input traces as short as possible.
- Run the input traces as far away from the supply lines as possible to reduce parasitic coupling.
- Place components close to device and to each other to reduce parasitic capacitance and parasitic errors.
- Use low-ESR, ceramic bypass capacitors to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Grounding for analog and digital portions of circuitry separately to suppresse the noise.



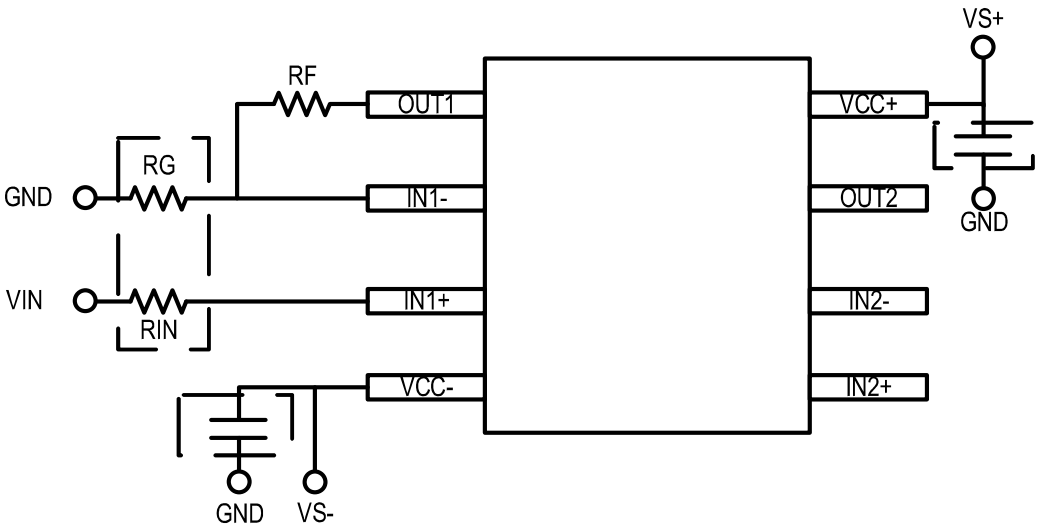
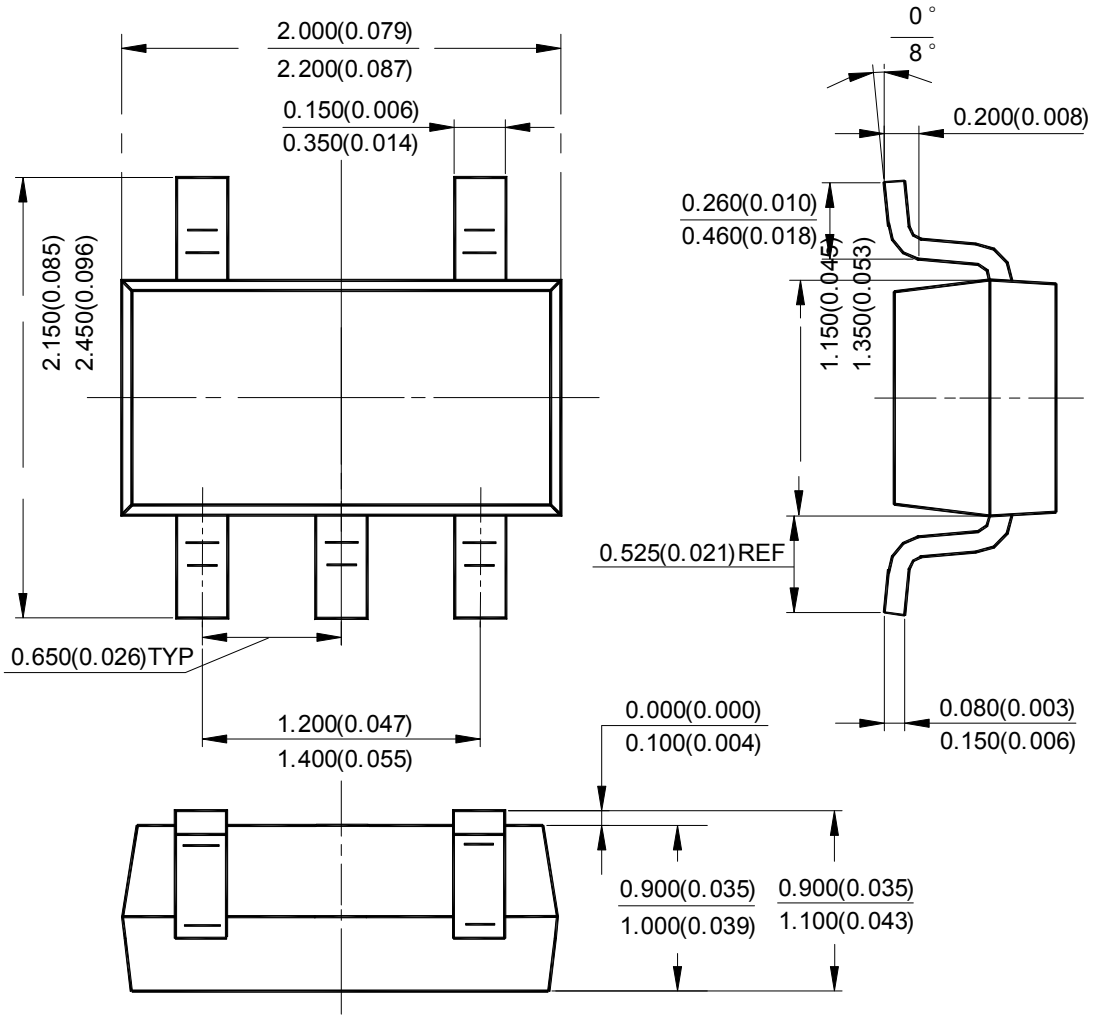


Figure 14. Operational Amplifier Schematic and Board Layout for Noninverting Configuration

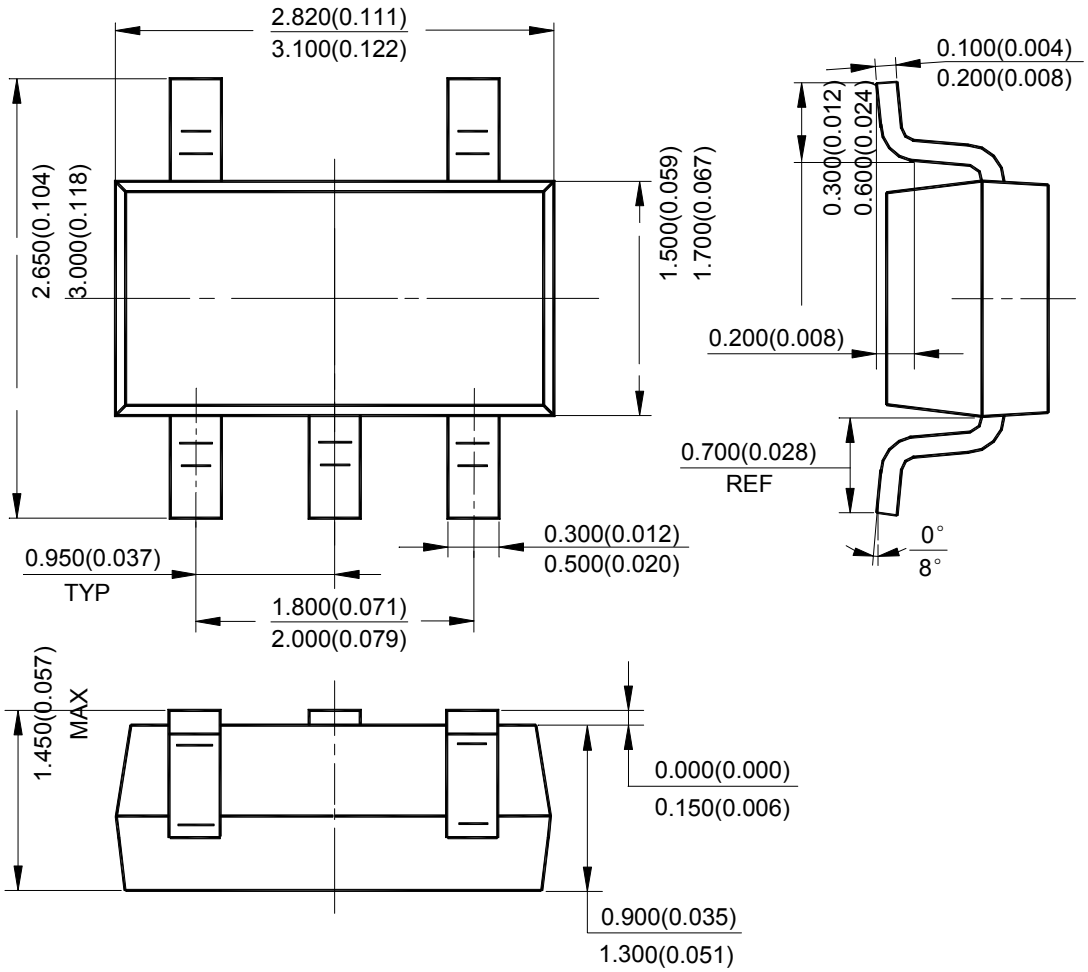
Package Outline Dimensions (All dimensions in mm(inch).)

SC-70-5



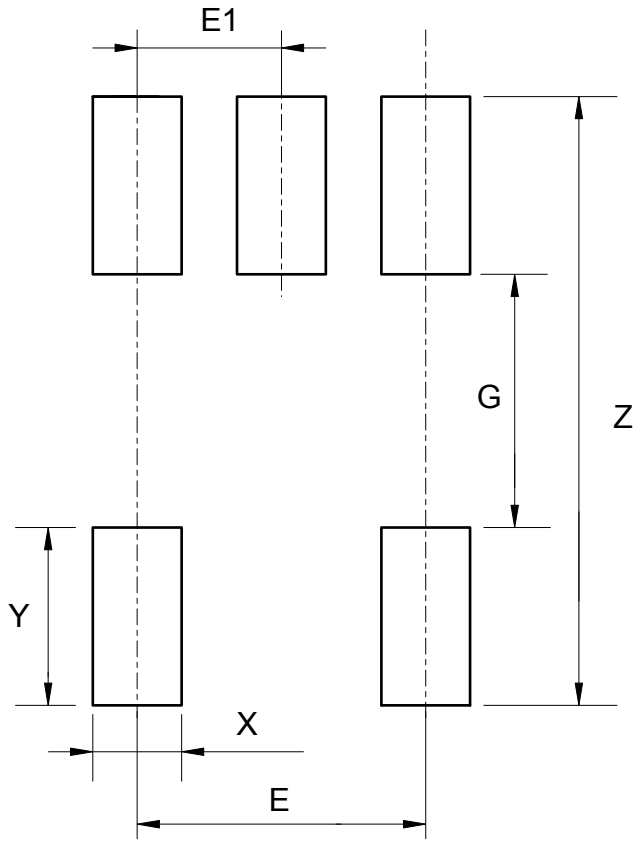
Package Outline Dimensions (Cont. All dimensions in mm(inch).)

SOT-23-5



Suggested Pad Layout

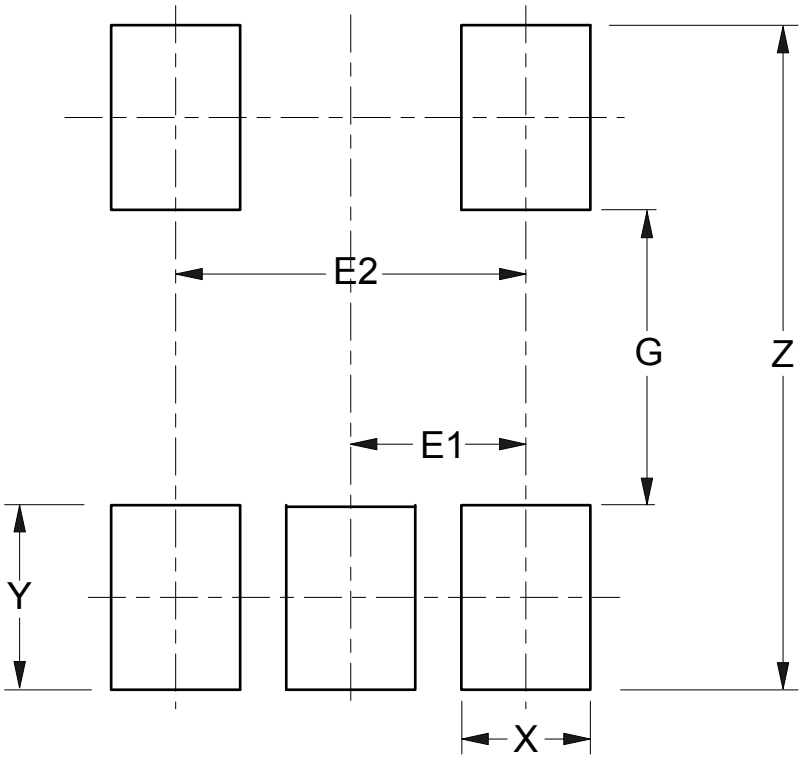
SC-70-5



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)	E1 (mm)/(inch)
Value	2.740/0.108	1.140/0.045	0.400/0.016	0.800/0.031	1.300/0.051	0.650/0.026

Suggested Pad Layout (Cont.)

SOT-23-5



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E1 (mm)/(inch)	E2 (mm)/(inch)
Value	3.600/0.142	1.600/0.063	0.700/0.028	1.000/0.039	0.950/0.037	1.900/0.075

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