



兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	1 of 51

Specification For HINK 5.83"EPD

Model NO.: HINK-E0583A51

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
ZHOU xiaoyuan	Cheng wei Zhou yufeng Zhu shengyuan	Hu ziping



兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	2 of 51

Version	Content	Date	Producer
A0	New release	2023/8/30	ZXY



兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	3 of 51

CONTENTS

1 General Description	4
2 Features	4
3 Application	4
4 Mechanical Specification	4
5 Mechanical Drawing of EPD Module	5
6 Input/Output Terminals	6
7 COMMAND TABLE... ..	8
8 Electrical Characteristics	35
9 Optical Characteristics.....	41
10 Handling Safety And Environment Requirements... ..	43
11 Reliability Test.....	45
12 PartA/PartB specification.....	46
13 Point and line standard.....	47
14 Barcode.....	49
15 Packing.. ..	50

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	4 of 51

1. General Description

HINK-E0583A51 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 5.83" active area contains 648×480 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel

2.Features

- 648×480 pixels disp
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in flash memory
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C Signal Master Interface to read external temperature sensor/ built-in temperature sensor
- Available in COG package IC thickness 280um

3. Application

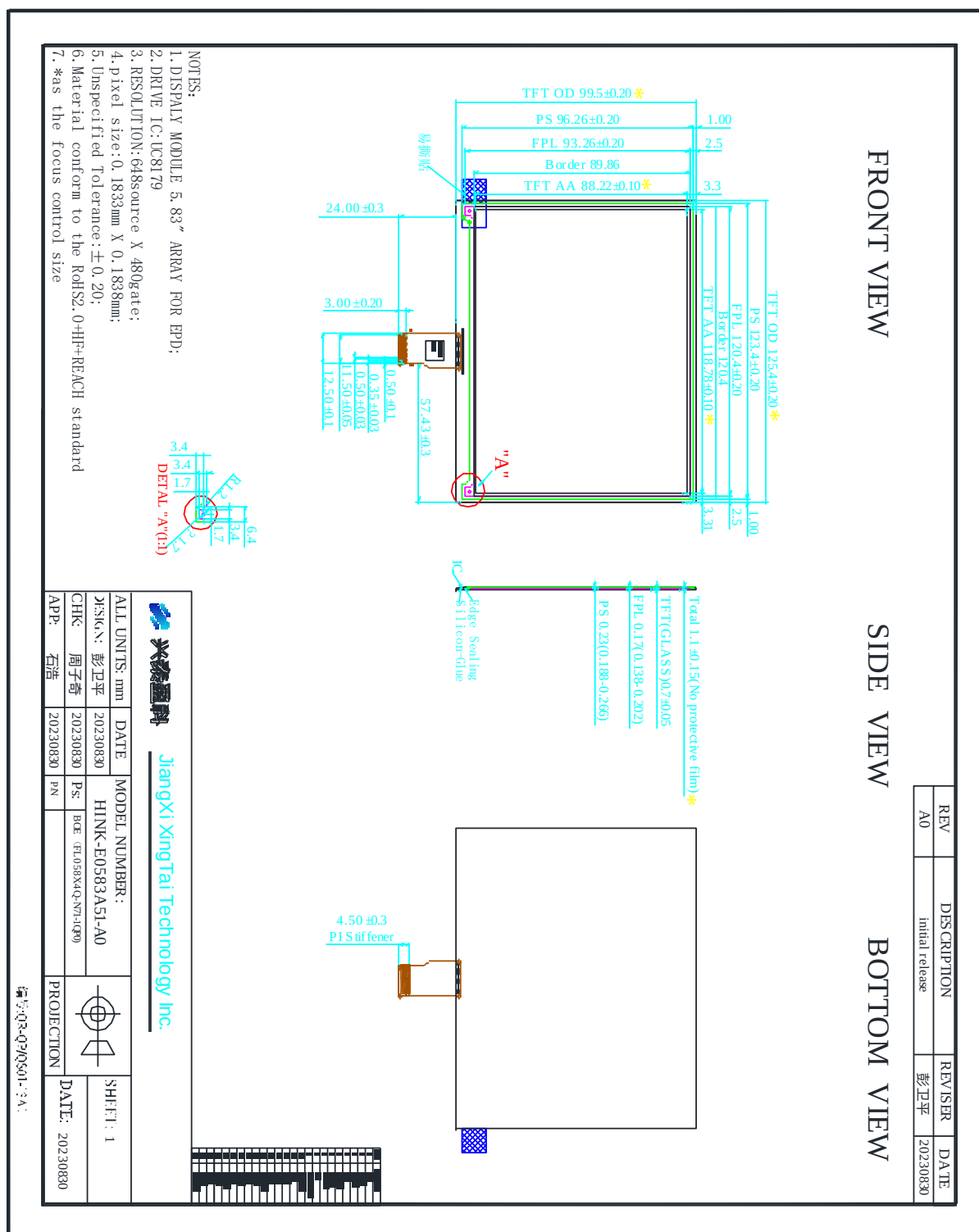
Electronic Shelf Label System

4.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	5.83	Inch	
Display Resolution	648(H)×480(V)	Pixel	Dpi:138
Active Area	118.78(H)×88.22(V)	mm	
Pixel Pitch	0.1833×0.1833	mm	
Pixel Configuration	Square		
Outline Dimension	125.4(H)×99.5(V) ×1.10	mm	Without mask
Weight	27±0.5	g	

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	5 of 51

5. Mechanical Drawing of EPD module





File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	6 of 51

6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pinss	Keep Open
2	GDR	This pin is N-MOS gate control.	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	
5	VSHR	Positive source voltage for Red	
6	TSCL	GND	
7	TSDA	GND	
8	BS	Input interface setting. Select 3 wire/ 4 wire SPI interface	Note 6-5
9	BUSY_N	This pin indicates the driver status	Note 6-4
10	RST_N	Global reset pin. Low reset	Note 6-3
11	DC	Serial communication Command/Data input	Note 6-2
12	(CSB)CS-N	Serial communication chip select	Note 6-1
13	(SCL)CLK	serial clock pin (SPI)	
14	(SDA)DATA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VDDA(VDD)	Power Supply pin for the chip	
17	VSS	Digital ground	
18	VDDD	Core logic power pin	
19	(FMSDO)VPP	OTP program power	
20	VSH	Positive Source driving voltage	
21	VGH	Positive Gate driving voltage	
22	VSL	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 6-2: TThis pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted asdata. When the pin is pulled Low, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active Low

Note 6-4: This pin (BUSY_N) is BUSY_N state output pin. When BUSY_N is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put BUSY_N pin low when the driver IC is working such as:
- Outputting display waveform; or
- Programming with OTP



兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	7 of 51

- Communicating with digital temperature sensor

Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low” , 4-line SPI is selected. When it is “High” , 3-line SPI (9 bits

SPI) is selected. Please refer to below Table..

Table: Bus interface selection

BS	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

**兴泰盈科****江西兴泰科技有限公司**

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	8 of 51

7. COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle

C/D: 0: Command / 1: Data

D7~D0: -: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	--	--	#	#	#	#	#	#	REG, KW/R, UD, SHL, SHD_N, RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	#	--	#	#	#	BD_EN, VSR_EN, VS_EN, VG_EN	07H
		0	1	--	--	--	#	--	#	#	#	VCOM_SLEW, VG_LVL[2:0]	17H
		0	1	--	--	#	#	#	#	#	#	VDH_LVL[5:0]	3AH
		0	1	--	--	#	#	#	#	#	#	VDL_LVL[5:0]	3AH
		0	1	--	--	#	#	#	#	#	#	VDHR_LVL[5:0]	03H
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC1[5:0]	17H
		0	1	#	--	#	#	#	#	#	#	PHC2_EN, BT_PHC2[5:0]	17H
8	Deep sleep (DSLTP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data (800x600):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-7:n]	-



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	9 of 51

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (800x600):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-7:n]	-
13	Dual SPI	0	0	0	0	0	1	0	1	0	1		15H
		1	1	--	--	#	#	--	--	--	--	MM_EN, DUSPI_EN	00H
14	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-

**兴泰盈科****江西兴泰科技有限公司**

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	10 of 51

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
16	K2W LUT (LUTKW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
17	W2K LUT (LUTWK / LUTW) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
18	K2K LUT (LUTKK / LUTK) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
19	Border LUT (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1		25H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
20	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	#	--	--	--	--	--	--	STATE_XON[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
21	KW LUT option (KWOPT)	0	0	0	0	1	0	1	0	1	1		2BH
		0	1	--	--	--	--	--	--	#	#	ATRED, NORED	00H
		0	1	#	#	--	--	--	--	--	--	KWE[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	KWE[7:0]	00H
22	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H

**兴泰盈科****江西兴泰科技有限公司**

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	11 of 51

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		0	1	--	--	--	--	#	#	#	#	FRS[3:0]	06H
23	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
24	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
25	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
26	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43H
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
27	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44H
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
28	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50H
		0	1	#	--	#	#	--	--	#	#	BDZ, BDV[1:0], DDX[1:0]	31H
		0	1	--	--	--	--	#	#	#	#	CDI[3:0]	07H
29	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	--	--	--	--	--	--	--	#	LPD	01H
30	End Voltage Setting (EVS)	0	0	0	1	0	1	0	0	1	0		52H
		0	1	--	--	--	--	#	--	#	#	VCEND, BDEND[1:0]	02H
31	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
32	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	--	--	--	--	--	--	#	#	HRES[9:8]	03H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	20H
		0	1	--	--	--	--	--	--	#	#	VRES[9:0]	02H
		0	1	#	#	#	#	#	#	#	#		58H
33	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	--	--	--	--	--	--	#	#	HST[9:8]	00H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	#	#	VST[9:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
34	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		1	1	#	#	#	#	#	#	#	#	PROD_REV[23:16]	FFH
		1	1	#	#	#	#	#	#	#	#	PROD_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	PROD_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:16]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	0CH
35	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	12 of 51

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG,I ² C_ERR, I ² C_BUSYN,DATA_FLAG, PON,POF,BUSY_N	13H
36	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
37	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
38	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	13 of 51

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
39	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	--	--	--	--	--	--	#	#	HRST[9:8]	00H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	--	--	--	--	--	--	#	#	HRED[9:8]	03H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	1FH
		0	1	--	--	--	--	--	--	#	#	VRST[9:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	#	#	VRED[8:0]	02H
		0	1	#	#	#	#	#	#	#	#		57H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
40	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
41	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
42	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
43	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
44	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
45	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
46	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
47	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
48	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H
50	Temperature Boundary Phase-C2 (TSBDY)	0	0	1	1	1	0	0	1	1	1		E7H
		0	1	#	#	#	#	#	#	#	#	TSBDY_PHC2[7:0]	00H

(1) Panel Setting (PSR) (Register: R00h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00H
	0	1	-	-	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

REG: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)

1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	14 of 51

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → ... → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → ... → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → ... → Sn-1

SHD_N: Booster Switch

0: Booster OFF

1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) Power Setting (PWR) (R01h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	BD_EN	-	VSR_EN	VS_EN	VG_EN	07H
	0	1	-	-	-	VCOM_SLEW	-	VG_LVL[2:0]			17H
	0	1	-	-	VDH_LVL[5:0]						3AH
	0	1	-	-	VDL_LVL[5:0]						3AH
	0	1	-	-	VDHR_LVL[5:0]						03H

BD_EN: Border LDO enable

0 : Border LDO disable (Default)

Border level selection: 00b: VCOM 01b: VDH

10b: VDL

11b: VDHR

1 : Border LDO enable

Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b: VBL(VCOM-VDH) 11b: VDHR

VSR_EN: Source LV power selection

0 : External source power from VDHR pins

1 : Internal DC/DC function for generating VDHR. (Default)

VS_EN: Source power selection

0 : External source power from VDH/VDL pins

1 : Internal DC/DC function for generating VDH/VDL. (Default)

VG_EN: Gate power selection

0 : External gate power from VGH/VGL pins

1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_SLEW: VCOM slew rate selection for voltage transition. The value is fixed at "1".

VG_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
-------------	-----------------------



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	15 of 51

000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 (Default)	VGH=20V, VGL= -20V

VDH_LVL[5:0]: Internal VDH power selection for K/W pixel. (Default value: 111010b)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

VDL_LVL[5:0]: Internal VDL power selection for K/W pixel. (Default value: 111010b)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	100110	-10.0 V	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	111010	-14.0 V
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

VDHR_LVL[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	16 of 51

VDHR_LV L	Voltage	VDHR_LV L	Voltage	VDHR_LV L	Voltage	VDHR_LV L	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

(3) Power OFF (POF) (R02h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence. This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) Power OFF Sequence Setting (PFS) (R03h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) Power ON (PON) (Register: R04h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence. This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	17 of 51

(6) Power ON Measure (PMES) (R05h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Internal Bandgap Set	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Booster Software Start Set	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA[7:6]		BT_PHA[5:3]			BT_PHA[2:0]		
	0	1	BT_PHB[7:6]		BT_PHB[5:3]			BT_PHB[2:0]		
	0	1	-		BT_PHC1[5:3]			BT_PHC1[2:0]		
	0	1	PHC2EN		BT_PHC2[5:3]			BT_PHC2[2:0]		

BT_PHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
 100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
 100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHC1[5:3]: Driving strength of phase C1

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
 100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHC1[2:0]: Minimum OFF time setting of GDR in phase C1

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

PHC2EN: Booster phase-C2 enable

0: Booster phase-C2 disable

Phase-C1 setting always is applied for booster phase-C.

1: Booster phase-C2 enable

If temperature > temperature boundary phase-C2(RE7h[7:0]), phase-C1 setting is applied for booster phase-C.

If temperature <= temperature boundary phase-C2(RE7h[7:0]), phase-C2 setting is applied for booster phase-C.

BT_PHC2[5:3]: Driving strength of phase C2

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
 100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	18 of 51

BT_PHC2[2:0]: Minimum OFF time setting of GDR in phase C2

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

07H
A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

10H
--
--
--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "OLD" data to SRAM.

In KWR mode, this command writes "K/W" data to SRAM.

In Program mode, this command writes "OTP" data to SRAM for programming

(10) Data Stop (DSP) (R11h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

11H
00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

(11) Display Refresh (DRF) (R12h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	19 of 51

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts

(12) Data Start Transmission 2 (DTM2) (R13h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “NEW” data to SRAM.

In KWR mode, this command writes “RED” data to SRAM.

(13) Dual SPI Mode (DUSPI) (R15h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	1	0	1	15H
	0	1	-	-	MM_EN	DUSPI_EN	-	-	-	-	00H

This command sets dual SPI mode.

MM_EN: MM input pin definition enable.

0: MM input pin definition disable

1: MM input pin definition enable.

DUSPI_EN: Dual SPI mode enable.

0: Dual SPI mode disable (single SPI mode)

1: Dual SPI mode enable

(14) Auto Sequence (AUTO) (R17h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(15) KW LUT Option (KWOPT) (R2Bh)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
KW LUT Option	0	0	0	0	1	0	1	0	1	1	2BH
	0	1	-	-	-	-	-	-	ATRED	NORED	00H
	0	1	KWE[9:8]		-	-	-	-	-	-	00H
	0	1	KWE[7:0]								00H

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	20 of 51

This command sets KW LUT mechanism option in KWR mode's LUT and only valid in K/W/R mode.

{ATRED, NORED}: KW LUT or KWR LUT selection control

ATRED	NORED	Description
0	0	KWR LUT always
0	1	KW LUT only
1	0	Auto detect by red data
1	1	KW LUT only

KWE[9:0]:

KW LUT enable control bits. Each bit controls one state, KWE[0] for state-1, KWE[1] for state-2,

At least 1 Enable Control bit should be set when KW LUT only is selected in KWR mode.

00 0000 0001b: KW LUT enable in State-1

00 0000 0011b: KW LUT enable in State-1 and State2

00 0000 1011b: KW LUT enable in State-1, State2 and State-4

(16) PLL Control (PLL) (R30h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	-	-	FRS[3:0]			

30H

06H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

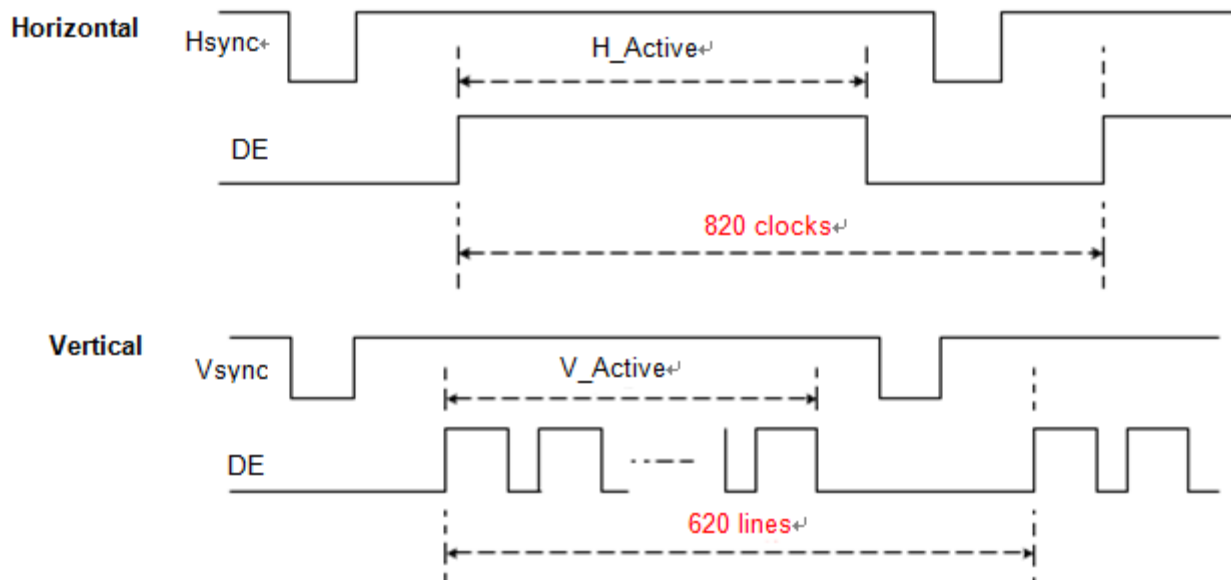
FMR[3:0]: Frame rate setting

FRS	Frame rate
0000	5Hz
0001	10Hz
0010	15Hz
0011	20Hz
0100	30Hz
0101	40Hz
0110	50Hz
0111	60Hz

FRS	Frame rate
1000	70Hz
1001	80Hz
1010	90Hz
1011	100Hz
1100	110Hz
1101	130Hz
1110	150Hz
1111	200Hz



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	21 of 51



(17) Temperature Sensor Calibration (TSC) (R40h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43

**兴泰盈科****江西兴泰科技有限公司**

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	22 of 51

1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

(18) Temperature Sensor Enable (TSE) (R41h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature Sensor	0	0	0	1	0	0	0	0	0	1
/Offset	0	1	TSE	-	-	-	TO[3:0]			

41H
00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calibration
0000 b	+0 (Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calibration
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(19) Temperature Sensor Write (TSW) (R42h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

42H
00H
00H
00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	23 of 51

(20) Temperature Sensor Read (TSR) (R43h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(21) Panel Glass Check (PBC)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	0	0	0	1	0	0	0	1	0	0	44H
	1	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(22) VCOM and Data interval Setting (CDI) (R50h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	BDZ	-	BDV[1:0]		N2OCP	-	DDX[1:0]		31h
	0	1	-	-	-	-	CDI[3:0]				07H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

BDZ: Border Hi-Z control

0: Border output Hi-Z disabled (default) 1: Border output Hi-Z enabled

BDV[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
--------	----------	-----



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	24 of 51

0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

N2OCP: Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default) 1: Copy NEW data to OLD data enabled

DDX[1:0]: Data polarity.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.

DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,

DDX[1]=1 is for KW mode without NEW/OLD.

DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)

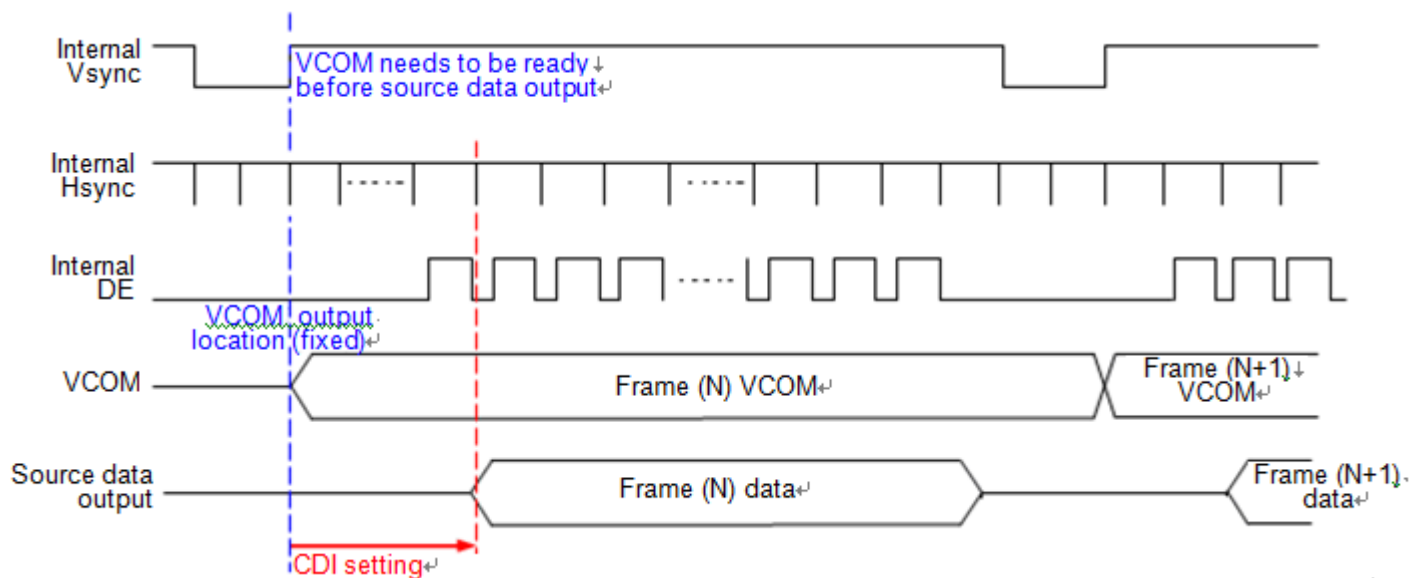
DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	25 of 51

	01	LUTWK (1 → 0)			
	10	LUTKW (0 → 1)			
	11	LUTWW (1 → 1)			
			1		LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval	CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync	1000	9
0001	16	1001	8
0010	15	1010	7
0011	14	1011	6
0100	13	1100	5
0101	12	1101	4
0110	11	1110	3
0111	10 (Default)	1111	2



(23) Low Power Detection (LPD) (R51h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

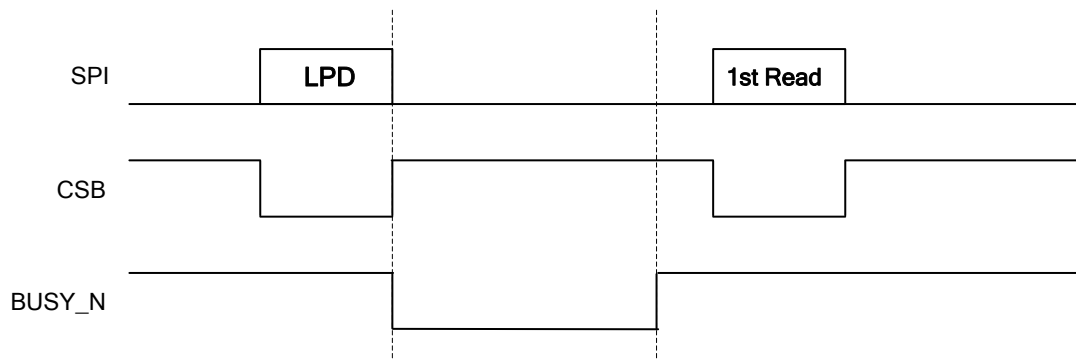
This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (VDD < 2.5V, 2.4V, 2.3V, or 2.2V, selected by LVD_SEL[1:0] in command LVSEL)

1: Normal status (default)

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	26 of 51



(24) End Voltage Setting (EVS) (R52h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
End Voltage Setting	0	0	0	1	0	1	0	0	1	0	52h
	0	1	-	-	-	-	VCEND	-	BDEND[1:0]		02h

This command selects source end voltage and border end voltage after LUTs are finished.

VCEND: VCOM end voltage selection

0b: VCOM_DC **1b:** floating

BDEND[1:0]: Border end voltage selection

00b: 0V **01b:** 0V **10b:** VCOM_DC **11b:** floating

(25) TCON Setting (TCON) (R60h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

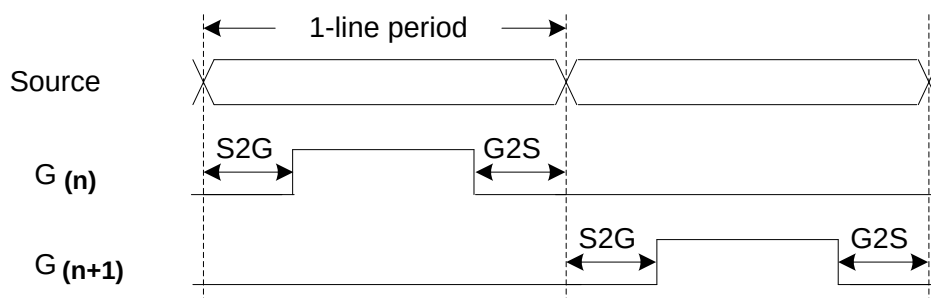
S2G[3:0] or G2S[3:0]	Period	S2G[3:0] or G2S[3:0]	Period
0000 b	4	1000 b	36
0001	8	1001	40
0010	12 (Default)	1010	44
0011	16	1011	48
0100	20	1100	52
0101	24	1101	56
0110	28	1110	60
0111	32	1111	64

Period Unit = 667 nS.

**兴泰盈科****江西兴泰科技有限公司**

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	27 of 51

**(26) Resolution Setting (TRES) (R61h)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	-	-	-	-	-	-	HRES[9:8]		03h
	0	1	HRES[7:3]					0	0	0	20h
	0	1	-	-	-	-	-	-	VRES[9:8]		02h
	0	1	VRES[7:0]								58h

This command defines resolution setting.

HRES[9:3]: Horizontal Display Resolution (Value range: 01h ~ 64h)

VRES[9:0]: Vertical Display Resolution (Value range: 001h ~ 258h)

Active channel calculation, assuming HST[9:0]=0, VST[9:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[9:0] - 1

Source: First active source = S0;
Last active source = HRES[9:3]*8 - 1

Example: 128 (source) x 272 (gate), assuming HST[9:0]=0, VST[9:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[9:0] = 272, 272 - 1 = 271)

Source: First active source = S0,
Last active source = S127; (HRES[9:3]=16, 16*8 - 1 = 127)

(27) Gate/Source Start Setting (GSST) (R65h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	-	-	-	-	-	-	HST[9:8]		00h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	VST[9:8]		00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[9:3]: Horizontal Display Start Position (Source). (Value range: 00h ~ 63h)

VST[9:0]: Vertical Display Start Position (Gate). (Value range: 000h ~ 257h)

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	28 of 51

Example : For 128(Source) x 240(Gate)

HST[9:3] = 4 (HST[9:0] = 4*8 = 32),

VST[9:0] = 32

Gate: First active gate = G32 (VST[9:0] = 32),

Last active gate = G271 (VRES[9:0] = 240, VST[9:0] = 32, 240-1+32=271)

Source: First active source = S32 (HST[9:0] = 32),

Last active source = S239 (HRES[9:0] = 128, HST[9:0] = 32, 128-1+32=239)

(28) Revision (REV) (R70h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	PROD_REV[23:16]								FFh
	1	1	PROD_REV[15:8]								FFh
	1	1	PROD_REV[7:0]								FFh
	1	1	LUT_REV[23:16]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[7:0]								FFh
	1	1	CHIP_REV[7:0]								0Ch

The command reads the product revision, LUT revision and chip revision.

PROD_REV[23:0]: Product Revision. PROD_REV[23:0] is read from OTP address 0x0BDD ~ 0X0BDF or 0x17DD ~ 0x17DF.

LUT_REV[23:0]: LUT Revision. LUT_REV[23:0] is read from OTP address 0x0BE0 ~ 0X0BE2 or 0x17E0 ~ 0x17E2.

CHIP_REV[7:0]: Chip Revision, fixed at 00001100b.

(29) Get Status (FLG) (R71h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_Flag	I ² C_ERR_R	I ² C_BUSYN	Data_Flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_Flag: Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

Data_Flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(30) Auto Measure VCOM (AMV) (R80h)



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	29 of 51

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

80h

10h

This command triggers auto VCOM sensing mechanism.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s **01b: 5s (default)**

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)

1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)

1: Trigger auto VCOM sensing.

(31) VCOM Value (VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV[6:0]						

81h

00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	30 of 51

000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(32) VCOM_DC Setting (VDCS) (R82h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	31 of 51

000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(33) Partial Window (PTL) (R90h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	1	0	0	0	0	90h
	0	1	-	-	-	-	-	-	HRST[9:8]		00h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	HRED[9:8]		03h
	0	1	HRED[7:3]					1	1	1	1Fh
	0	1	-	-	-	-	-	-	VRST[9:8]		00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	VRED[9:8]		02h
	0	1	VRED[7:0]								57h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[9:3]: Horizontal start channel bank. (Value range: 00h~63h)

HRED[9:3]: Horizontal end channel bank. (Value range: 00h~63h). HRED must be greater than HRST.

VRST[9:0]: Vertical start line. (Value range: 000h~257h)

VRED[9:0]: Vertical end line. (Value range: 000h~257h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

(34) Partial In (PTIN) (R91h)

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	32 of 51

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

91h

This command makes the display enter partial mode.

(35) Partial Out (PTOUT) (R92h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Out	0	0	1	0	0	1	0	0	1	0

92h

This command makes the display exit partial mode and enter normal mode.

(36) Program Mode (PGM) (RA0h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(37) Active Program (APG) (RA1h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

A1h

After this command is transmitted, the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed

(38) Read OTP Data (ROTP) (RA2h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	:							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

A2h

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.

(39) Cascade Setting (CCSET) (RE0h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Cascade Option	0	0	1	1	1	0	0	0	0	0
	0	1	-	-	-	-	-	-	TSFIX	CCEN

E0h

00h

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	33 of 51

This command is used for cascade.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS_SET[7:0] registers.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

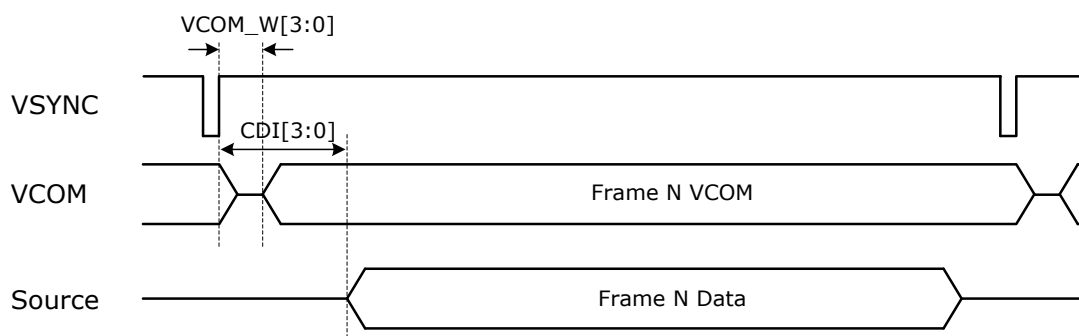
1: Output clock at CL pin to slave chip

(40) Power Saving (PWS) (RE3h)

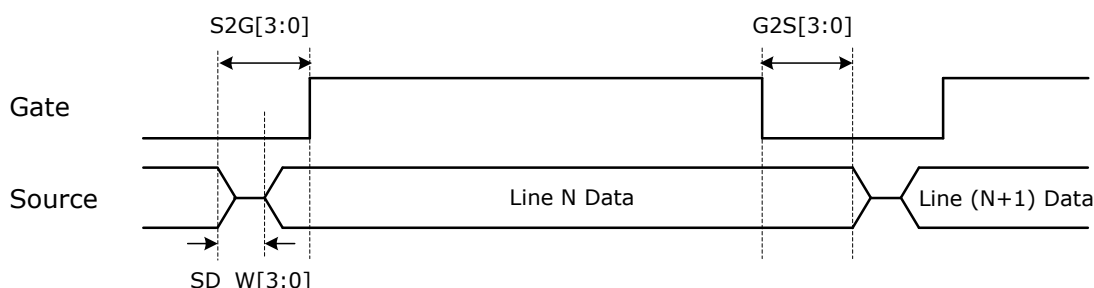
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (Unit: line period)



SD_W[3:0]: Source power saving width (Unit: 660nS)



(41) LVD Voltage Select (LVSEL) (RE4h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

**兴泰盈科****江西兴泰科技有限公司**

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	34 of 51

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(42) Force Temperature (TSSET) (RE5h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

E5h
00h

This command is used for cascade to fix the temperature value of master and slave chip

(43) Temperature Boundary Phase-C2 (TSBDRY) (RE7h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Boundary Phase-C2	0	0	1	1	1	0	0	1	1	1
	0	1	TSBDRY_PHC2[7:0]							

E7h
00h

This command is used to set the temperature boundary to judge whether booster phase-C2 is applied or not.



兴泰盈科

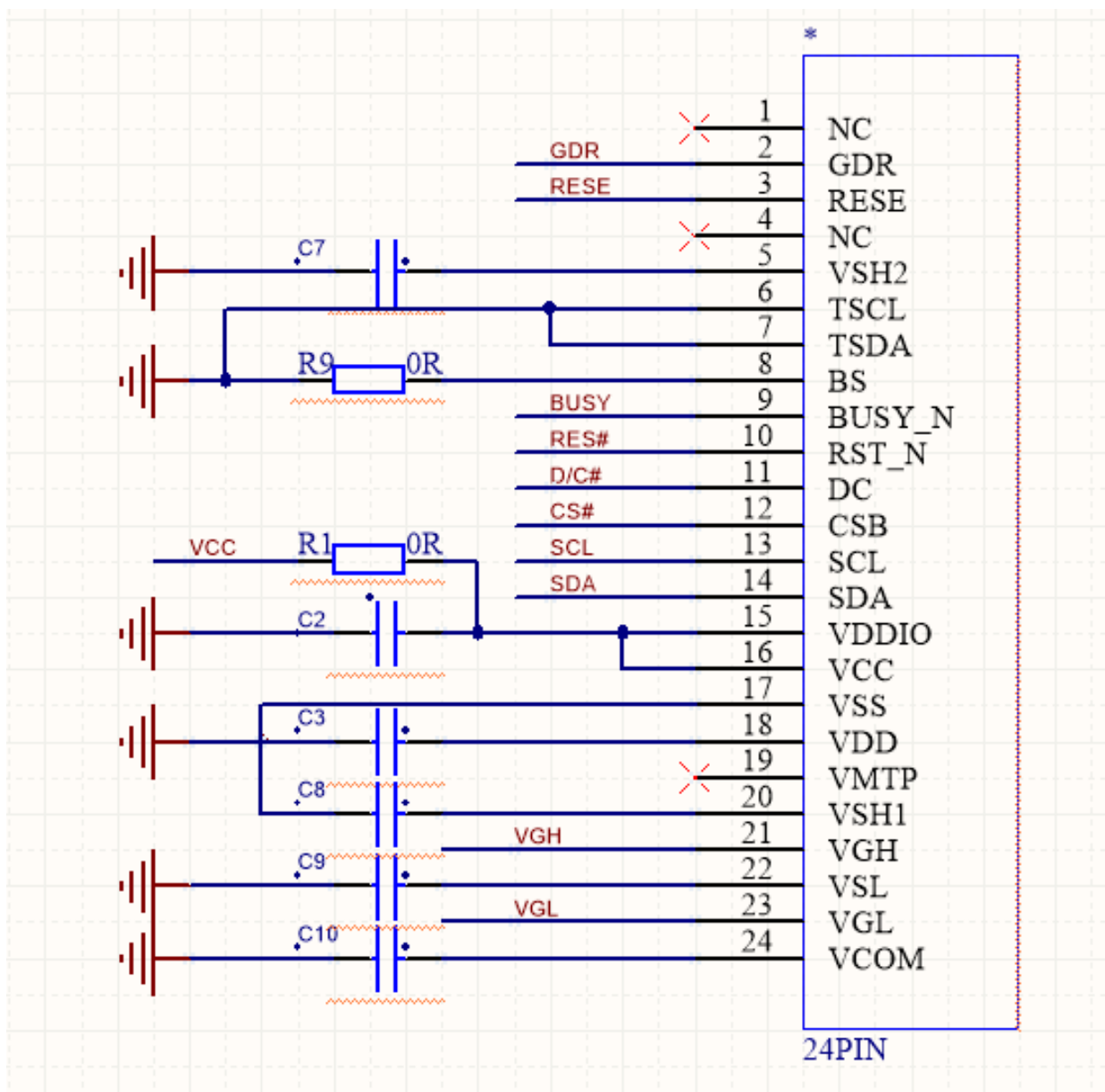
江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	35 of 51

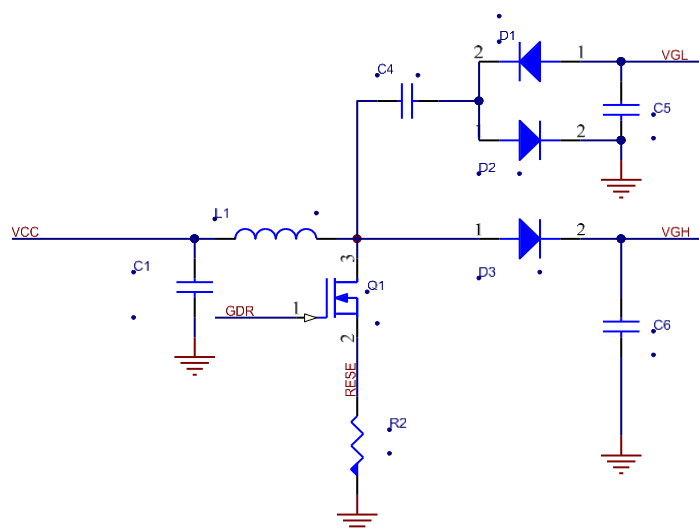
8. Electrical Characteristics

8-1) Reference Circuit





File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	36 of 51



Part Name	UC179c/Value /quirement/Reference Part
C1—C3	1uF/0603;X5R/X7R;Voltage Rating: 25V
C4	4.7uF/0603;X5R/X7R;Voltage Rating: 25V
C5-C6	4.7uF/0603;X5R/X7R;Voltage Rating: 25V
C7-C9	4.7uF/0603;X5R/X7R;Voltage Rating: 25V
C10	1uF/0603;X5R/X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) Forward current $\geq 500mA$ 3)Forward voltage $\leq 430mV$
R2	0.47 Ω /0603: 1% variation
Q1	NMOS:Si1308EDL 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs} (th) = 0.9 (Typ) , 1.3V (Max)$ 3) $R_{ds on} \leq 2.1\Omega @ V_{gs}=2.5V$
L1	10uH/Taiyo Yuden NR4018T100M DCR< 0.5 ohm, Isat $\geq 1.2A @ 25^{\circ}C$

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	37 of 51

8-2) Absolute maximum rating

Table 8-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
VCI	Logic supply voltage	-0.5 to +6.0	V
TOPR	Operation temperature range	0 to 50	°C
TSTG	Storage temperature range	-25 to 60	°C

Note8-1: Tstg is the transportation condition, the transport time is within 10 days for -25°C~0°C or 50°C~60°C

8-3) Panel DC Characteristics

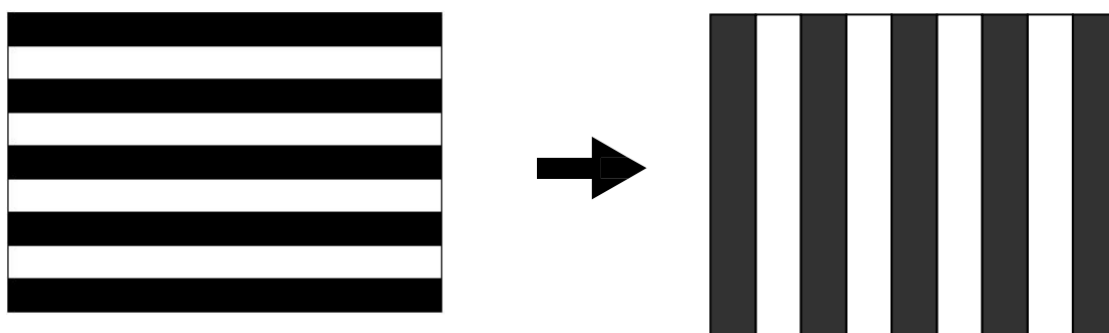
The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Logic Supply Voltage	-	2.5	3.3	3.6	V
VIH	High level input voltage	Digital input pins	0.7xV DDIO	-	V DDIO	V
VIL	Low level input voltage	Digital input pins	GND	-	0.3xV DDIO	V
VOH	High level output voltage	IOH= 400uA	VDDIO-0.4	-	-	V
VOL	Low level output voltage	IOH= -400uA	GND	-	0.4	V
Iupdate	Module operating current	-	-	11	-	mA
Isleep	Deep sleep mode	VDD= 3.3V	-	3	-	uA

- The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 8-3)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 8-3

The Typical power consumption



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	38 of 51

8-4) Panel AC Characteristics

8-4-1) MCU Interface

8-4-1-1) MCU Interface Selection

UC8179 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

8-4-1-2) 3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

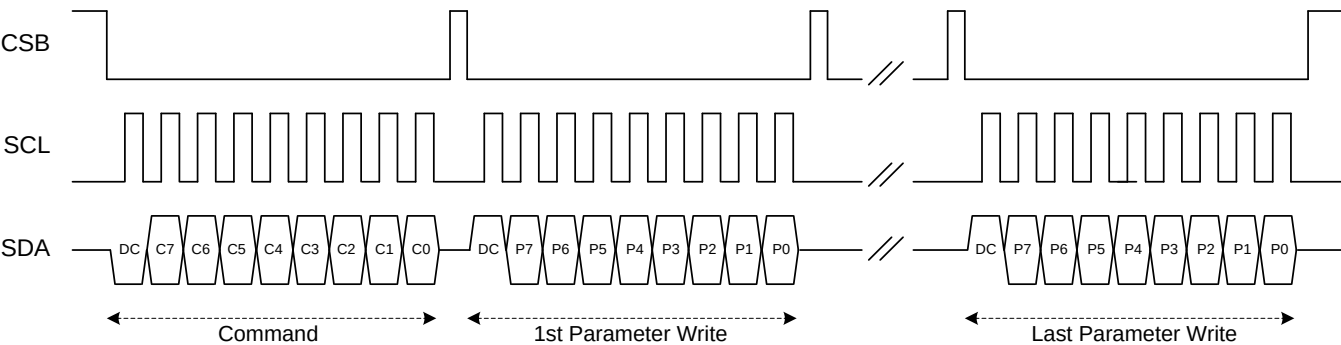


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

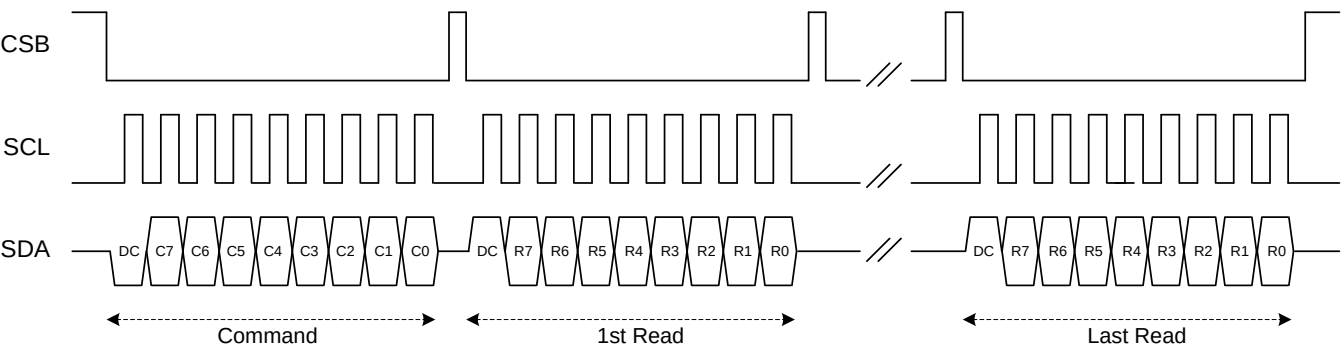


Figure: 3-wire SPI read operation

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	39 of 51

8-4-1-3) 4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

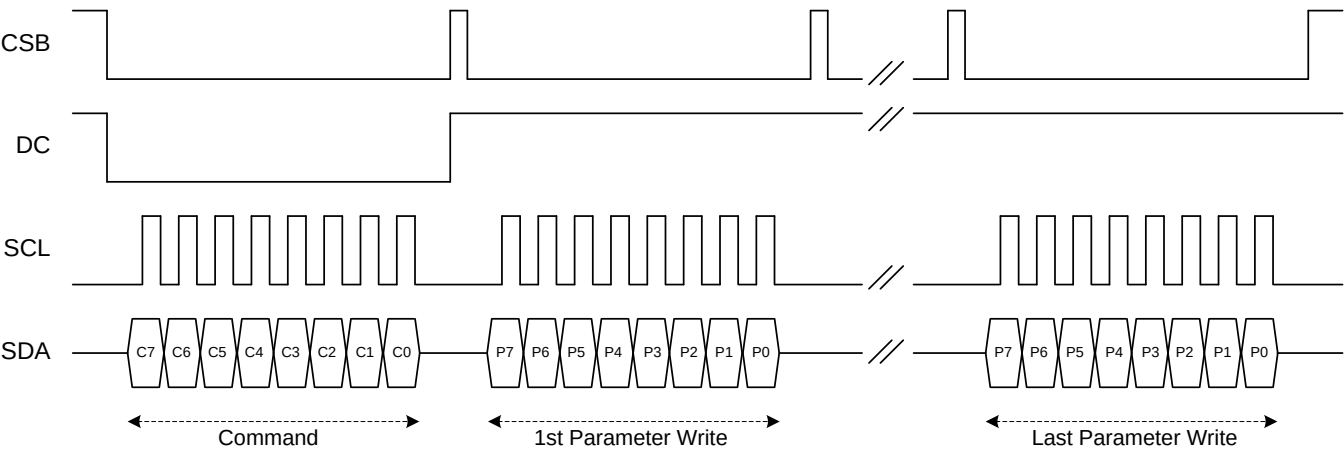


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

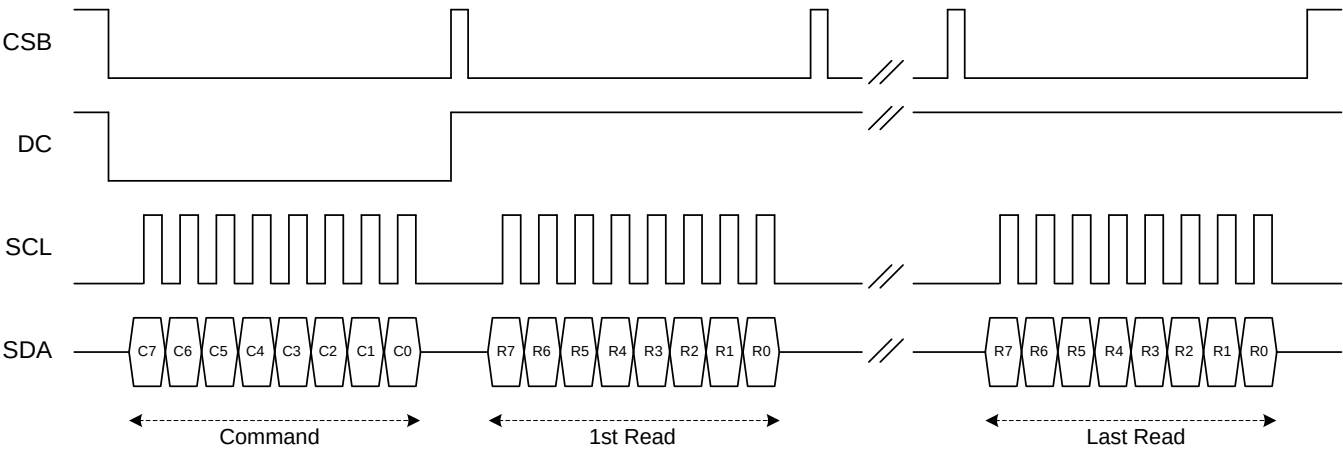


Figure: 4-wire SPI read operation

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	40 of 51

8-4-2) 3 wire dual SPI format

Data / Command is recognized with the first bit transferred at SDA. Data are transferred in the unit of 5 SPI clocks. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 5 SPI clocks. (The serial counter is reset at the rising edge of the CSB signal.) In 3-wire dual SPI mode, SDA and SDA1 are only input mode for data write transmission.

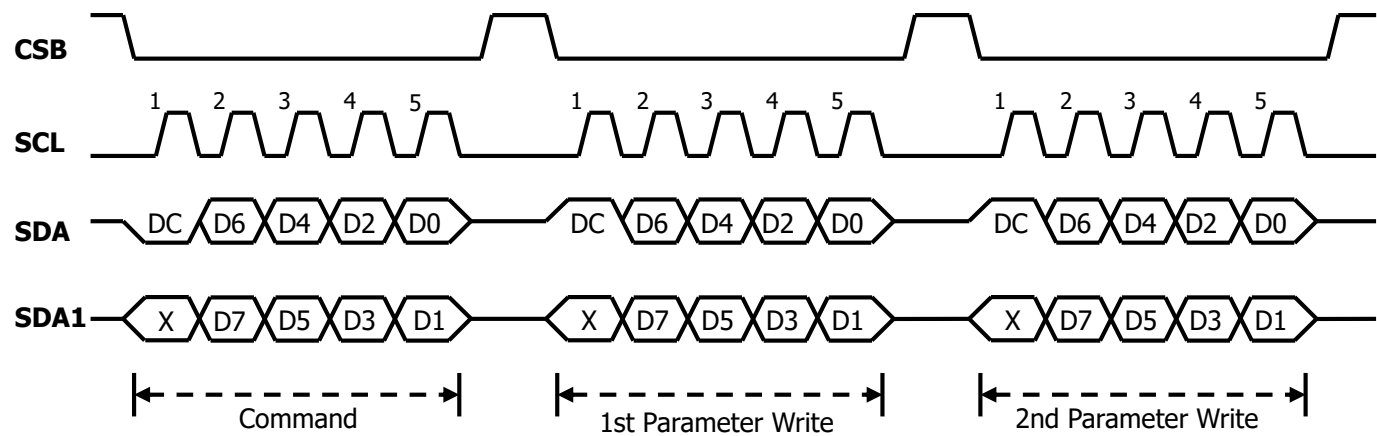


Figure: 3-wire dual SPI write operation

4 wire dual SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 4 SPI clocks. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 4 SPI clocks. (The serial counter is reset at the rising edge of the CSB signal.) In 4-wire dual SPI mode, SDA and SDA1 are only input mode for data write transmission.

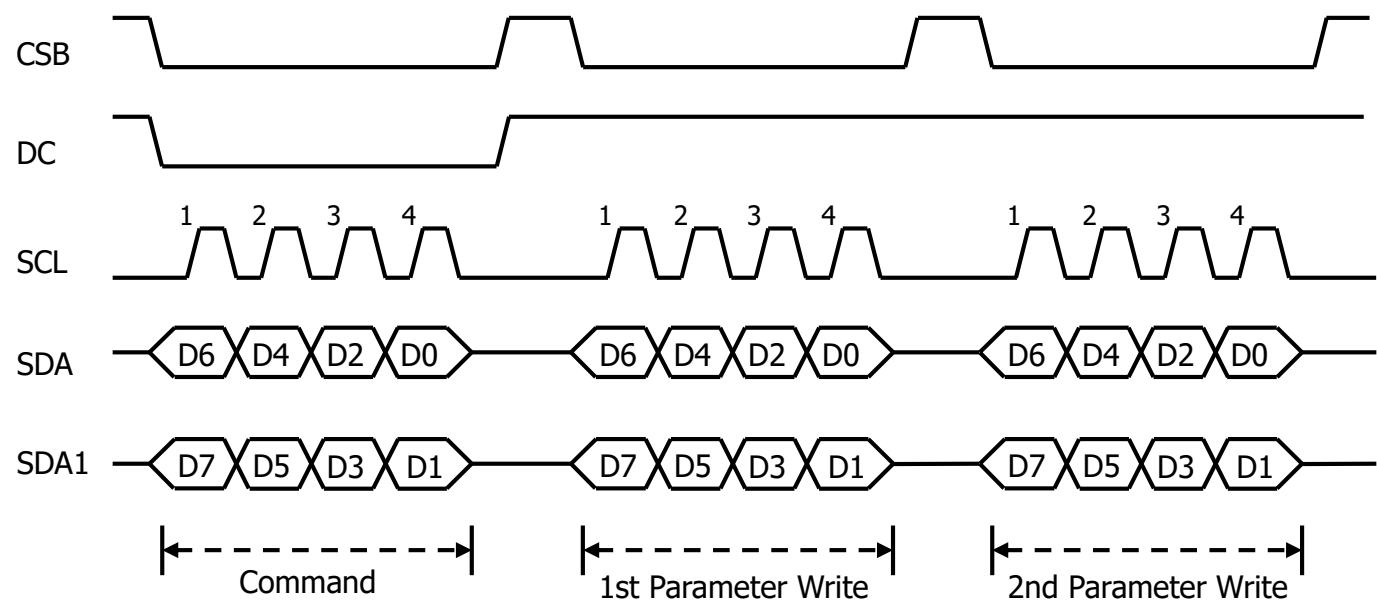


Figure: 4-wire dual SPI write operation



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	41 of 51

8-5) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃		50	mAs	-
Deep sleep mode	-	25℃		3	uA	-

mAs=update Average current ×update time

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	42 of 51

9. Optical characteristics

9.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 9-1
CR	Contrast Ratio	-	10	12	-		-
KS	Monochrome State L* value		--	17	20		
	Monochrome State a* value		--				
WS	Monochrome State L* value		66	67	--		
	Monochrome State a* value				--		
Tupdate_YS	Update time			3		sec	

WS : White state, DS : Dark state, RS: Red state

Note 9-1 : Luminance meter : Eye - One Pro Spectrophotometer

Note 9-2: We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH;

Suggest Updated once a day;

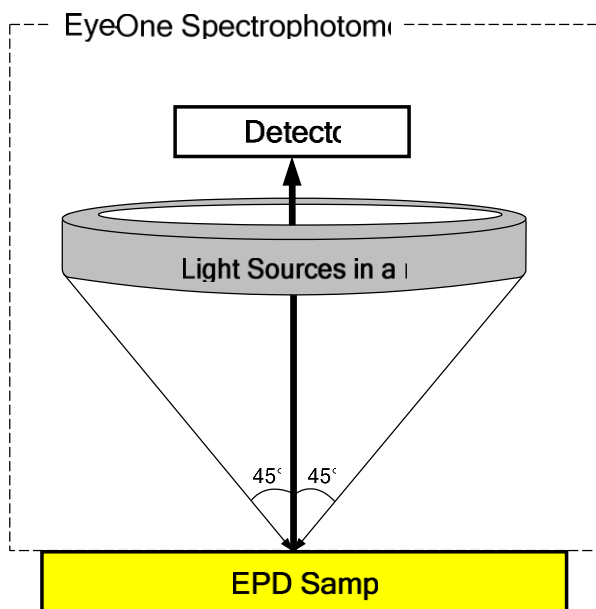


File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	43 of 51

9.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

$$CR = Rl/Rd$$

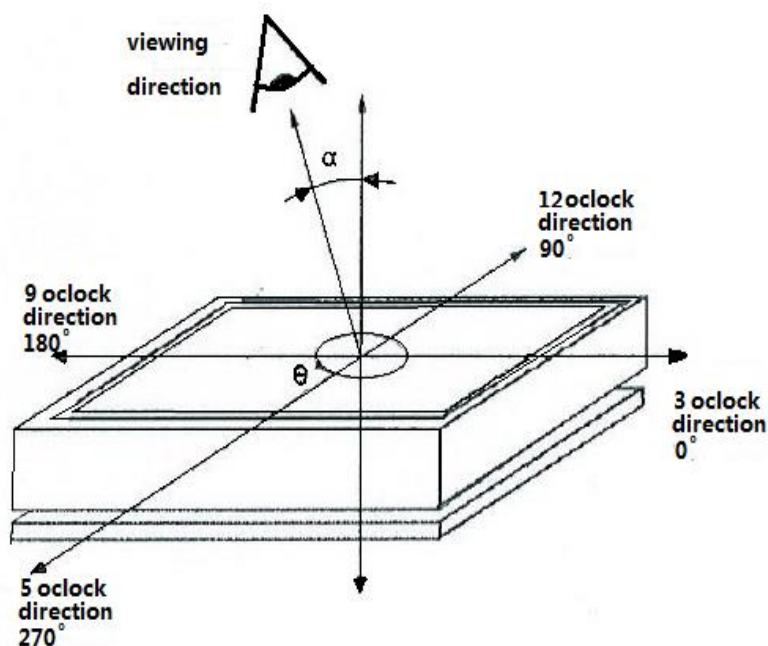


9.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	44 of 51

10. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions

(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.

(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Product specification	The data sheet contains final product specifications.
-----------------------	---

Limiting values



兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	45 of 51

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E0583A51
Version	A0	Page Number	46 of 51

11. Reliability test

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40°C, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0°C for 240 hrs	
3	High-Temperature Storage	T=50°C RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40°C,RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=50°C,RH=90%RH,For 240Hr	Test in white pattern
7	Temperature Cycle	-25°C(30min)~60°C(30min),50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/m ² for 168hrs,40°C	

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white/red pattern , hold time is 150S.

Note3: The function ,appearance, opticals should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20°C-25°C.



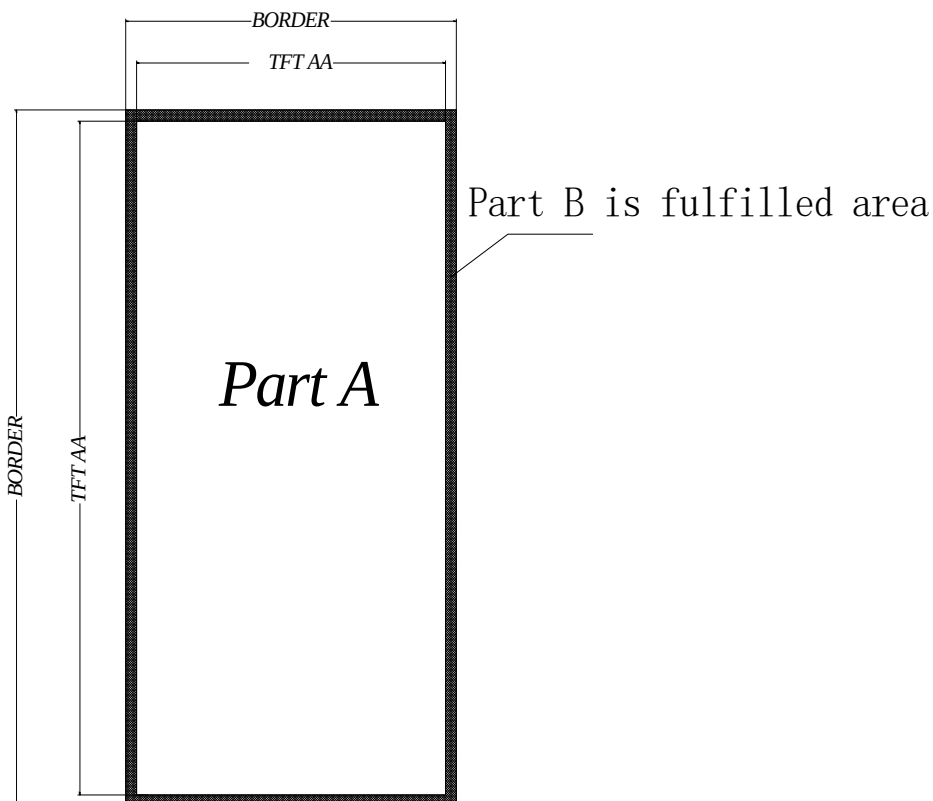
兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E075A32
Version	A0	Page Number	47 of 51

12. PartA/PartB specification





兴泰盈科

江西兴泰科技有限公司

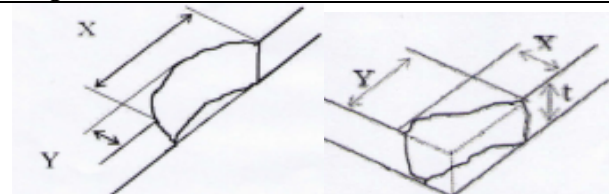
JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E075A32
Version	A0	Page Number	48 of 51

13. Point and line standard

Shipment Inspection Standard

Equipment: Electrical test fixture, Point gauge

Outline dimension	170.20(H)×111.20 (V) ×1.25 (D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 mm	35Sec	
Defet type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.2 mm		Ignore		Ignore
		0.2 mm<D≤0.4 mm		N≤4		Ignore
		0.4 mm<D≤0.6 mm		N≤1		Ignore
		D>0.6 mm		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.1 mm		Ignore		Ignore
		1.0mm<L≤9.0mm, 0.1<W≤0.2mm,		N≤2		Ignore
		L>9.0 mm, W>0.2 mm		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.4mm		Ignore		Ignore
		0.4mm≤D≤0.6mm		N≤4		Ignore
		D>0.6 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	Do not affect the electrode circuit((Corner chipping) X≤8mm, Y≤1mm, Do not affect the electrode circuit, Ignore				
						
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					
	L=long W=wide D=point size N=Defects NO					

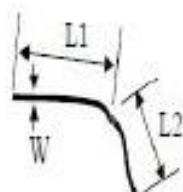


兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E075A32
Version	A0	Page Number	49 of 51



$$L = L1 + L2$$

Line Defect



$$D = (L + W) / 2$$

Spot Defect

L=long W=wide D=point size

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E075A32
Version	A0	Page Number	50 of 51

14.Barcode

14.1 Babel appearance



ABBBBBBBCC
 DDDEEEFGGG

14.2 QR scanned information (Total 28 code number+ 2 blank spaces)

A
 BBBBBBBB
 CC

 DDD
 EEE
 F
 GGG

 H
 III
 J
 KKK

①
 ②
 ③
 ④
 ⑤
 ⑥
 ⑦
 ⑧
 ⑨
 ⑩
 ⑪

- ① A——The factory code
 ② BBBBBBBB——Module name of EPD
 ③ CC——FPL model name
 ④ DDD——Date of production
 ⑤ EEE——Production lot
 ⑥ F——Separator
 ⑦ GGG——FPL Lot
 ⑧ H——Normal Lot
 ⑨ III——TFT、PS、EC.
 ⑩ J——IC
 ⑪ KKK——Serial NO.



File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E075A32
Version	A0	Page Number	51 of 51

15.Packing

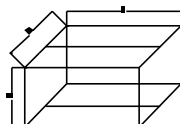
Packing Spec

Sheet No :

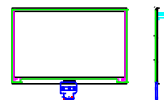
	Part No	HINK-E075A38	DATE	2020. 2. 23	VER	A0	Page	2-1
---	---------	--------------	------	-------------	-----	----	------	-----

一, Package Type: Box

Box No	HINK-E029A01-ZX-A0
Box size	515*322*170
Containment	48PCS



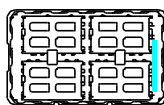
PRODUCT DRAWING



二, Inside package type: Plastic

Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE (inside)	408.17*114.75*2	24 pcs
EPE (Up-Down)	485*145*10	2 pcs
EPE (Left-Right)	285*480*10	2 pcs
EPE (Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	4 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	



Empty tray

Anti-static EPE

Step 1:

Material: Tray, EPE

Put the product in to the tray and keep the display side up. Then put anti-static EPE in to each holes.

Step 2,

1), Must keep the angle 180 degree placed between the neighboring Plastic trays.

2), There are 12 layers product, total 4*12=48 pcs.

3), An empty Plastic tray intersects put on the top of the plastic trays.

Step 5,

1), Seal the box with adhesive tapes .

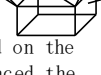
2), Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign.

Step 3,

1), In each case, put 2 bags of desiccant, then seal the trays with adhesive tapes.

2), Put the trays into foil bags.

3), heat seal the foil bags.



Step 4,

1), First put a chip board on the bottom of the box, then placed the down EPE, the left - right and front -back EPE.

2), Placed the sealed products into the box.

3), The last placed the up EPE on the top of the trays, and place a chip board on it.

Design	X. Z. P	Approve	J. P. F	Confirm	X.X.M
Date	2019. 6. 10	Date	2019. 6. 10	Date	2019. 6. 10



兴泰盈科

江西兴泰科技有限公司

JIANGXI XINGTAI TECHNOLOGY CO.,LTD.

File Name	Specification For HINK 5.83" EPD	Module Number	HINK-E075A32
Version	A0	Page Number	52 of 51

Packing Spec

Sheet No

	Part No	HINK-E075A38	Date	2020. 2. 23	VER	A0	Page	2-2
---	---------	--------------	------	-------------	-----	----	------	-----

The label outside the carton print as below

90.00	
Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G.W	E
N.W	F
MFG Date	J
Carton No	
Remark	

NOTE:

- 1."A" Print customer Item No
- 2."B" Print customer Order No
- 3."C" Print MFG Batch No(Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.
- 4."D"Print product qty
- 5."E"Print the G.W
- 6."F"Print the N.W
- 7."J"Print the MFG date
- 8.Before packing make sure the FPL batch ,item and qty are the same as which on the Final passed card.

Design	X. Z. P	Approve	J. P. F	Confirm	X.X.M
Date	2019. 6. 10	Date	2019. 6. 10	Date	2019. 6. 10