



# MP5475

Fully Integrated, 12V, 6A,  
Quad-Buck PMIC with I<sup>2</sup>C, Telemetry,  
and Flexible System Configurations

## DESCRIPTION

The MP5475 is a complete power management IC (PMIC) that integrates four high efficiency step-down DC/DC converters and a flexible logic interface.

The integrated DC/DC converters provide constant-on-time (COT) control to achieve fast transient response. In addition, the 1MHz switching frequency ( $f_{sw}$ ) minimizes the external inductor and capacitor size. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The output voltage ( $V_{OUTx}$ ) (where  $x = A, B, C,$  or  $D$ ) can be adjusted via the I<sup>2</sup>C bus, or it can be preset by the multiple-time programmable (MTP) memory function. The power on/off sequence can also be configured by the MTP, or it can be controlled online via the I<sup>2</sup>C.

The first two rails or the last two rails can work in either independent mode or parallel mode, which can be configured via the MTP. The current-sharing function is implemented in parallel mode.

The MP5475 requires a minimal number of external components, and it is available in a space-saving QFN-35 (5mmx5mm) package.

## FEATURES

- Wide 3V to 16V Input Voltage ( $V_{INx}$ ) (where  $x = A, B, C,$  or  $D$ ) Range
- Adaptive Constant-On-Time (COT) Control for Ultra-Fast Transient Response
- Four High-Efficiency Step-Down Converters:
  - Buck A: 6A, 15mΩ/5mΩ DC/DC Converter
  - Buck B: 6A, 15mΩ/5mΩ DC/DC Converter
  - Buck C: 6A, 15mΩ/5mΩ DC/DC Converter
  - Buck D: 6A, 15mΩ/5mΩ DC/DC Converter

## FEATURES (continued)

- Buck A/B and Buck C/D Support Up to 12A of Continuous Current in Dual-Phase Mode
- 2 x 50mA Low-Dropout (LDO) Regulators
- Differential Output Voltage ( $V_{OUTx}$ ) (where  $x = A, B, C,$  or  $D$ ) Remote Sense
- I<sup>2</sup>C Slave Address Configurable via the Multiple-Time Programmable (MTP) Memory
- I<sup>2</sup>C-Configurable, 0.3V to 2.048V Reference Voltage ( $V_{REF}$ ) in 2mV Steps with Slew Rate Control
- Configurable 500kHz to 2MHz Switching Frequency ( $f_{sw}$ )
- Open-Drain Power Good (PG) Indication and General Status Interrupt
- MTP-Configurable Soft-Start (SS)/Soft Shutdown and Delay
- Selectable Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) Mode, Adjustable Frequency, and Current Limit via the I<sup>2</sup>C
- Pre-Biased Start-Up
- Over-Current Protection (OCP), Under-Voltage Lockout (UVLO), Under-Voltage Protection (UVP), Over-Voltage Protection (OVP), and Thermal Shutdown Protection
- Available in a QFN-35 (5mmx5mm) Package



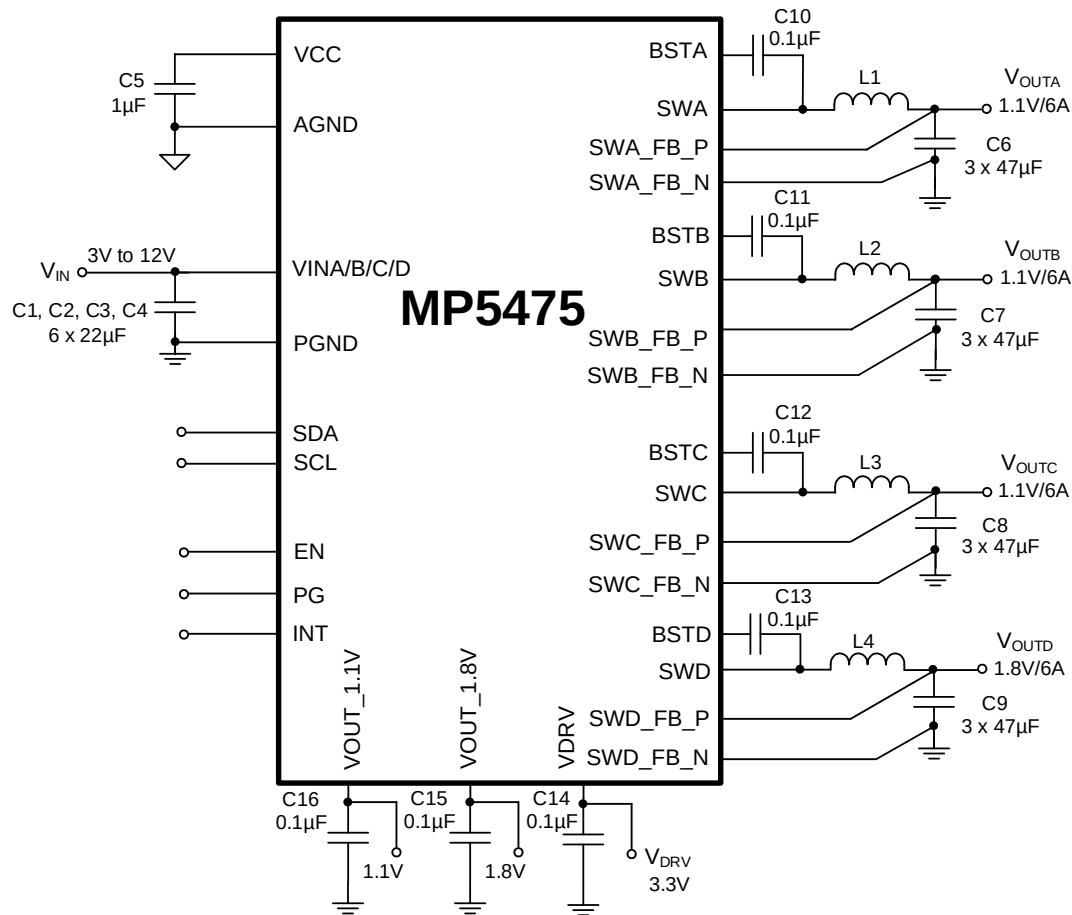
Optimized Performance with  
MPS Inductor MPL4020 Series

## APPLICATIONS

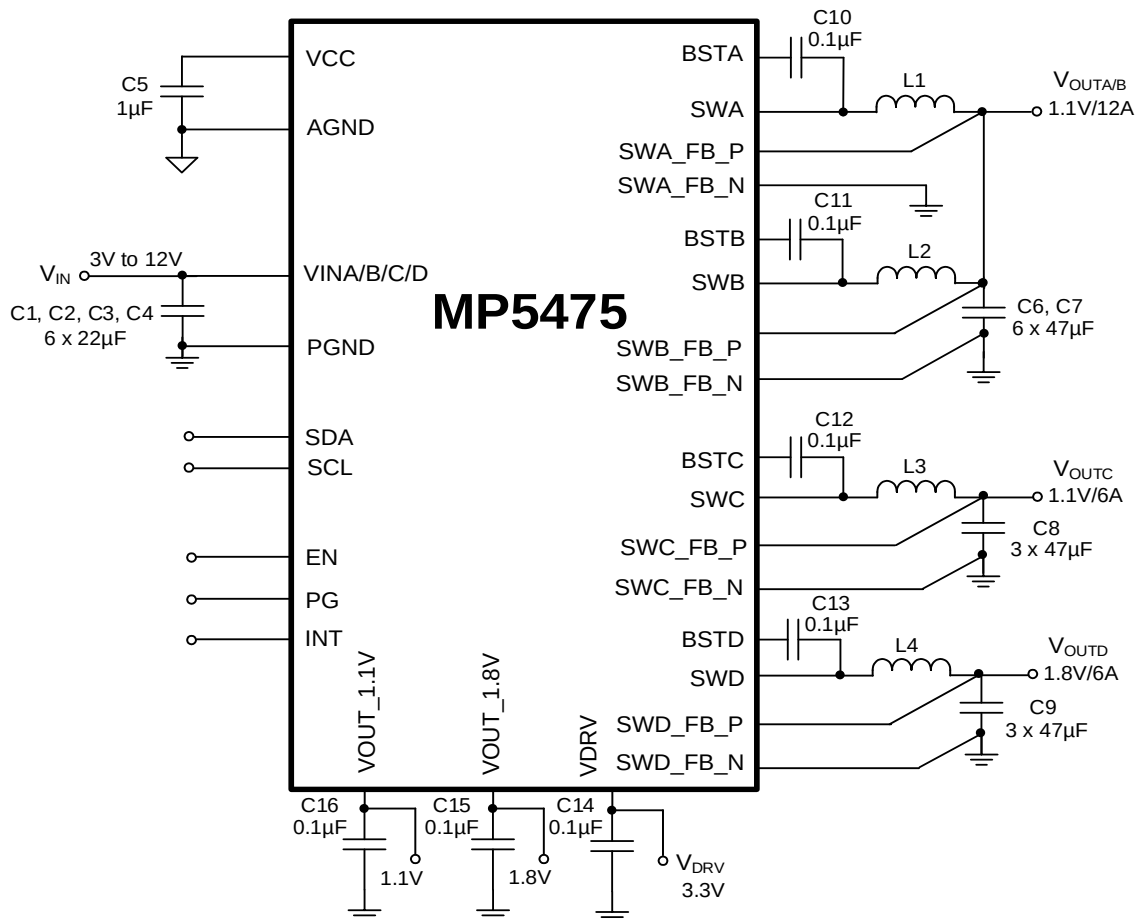
- Storage and Networking
- Enterprise Solid-State Drives (SSDs)
- General Enterprise Applications

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## TYPICAL APPLICATIONS

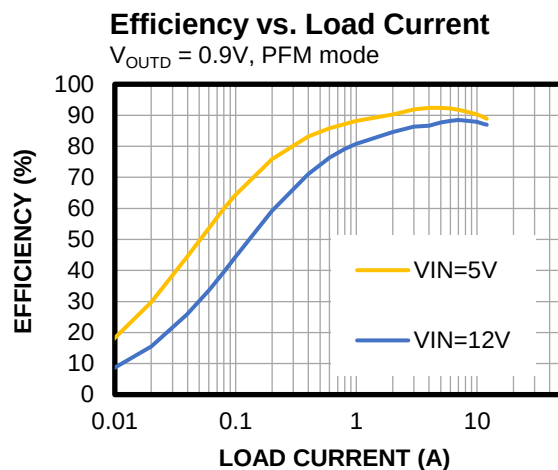
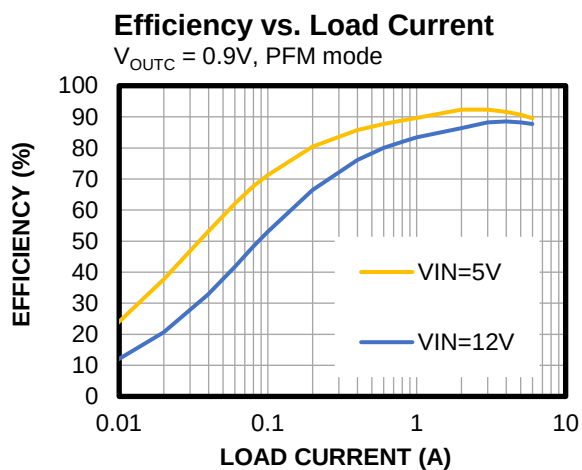
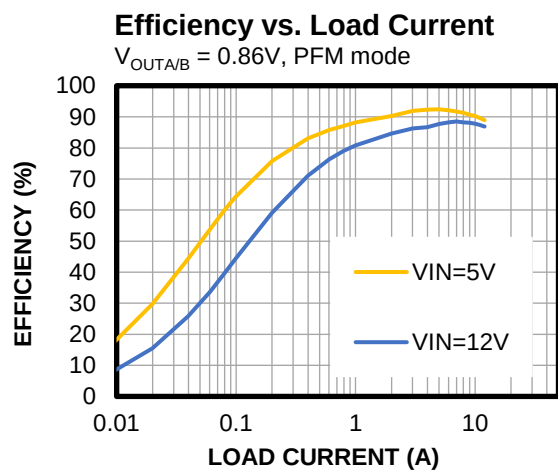


## TYPICAL APPLICATIONS *(continued)*



**Figure 2: Typical Application (Buck A and Buck B in Dual-Phase Regulator Mode)**

## TYPICAL APPLICATIONS *(continued)*



## DEFAULT MULTIPLE-TIME PROGRAMMABLE (MTP) SELECTION

| OTP Items                                                     | Buck A       | Buck B     | Buck C       | Buck D     |
|---------------------------------------------------------------|--------------|------------|--------------|------------|
| Output voltage (V <sub>OUT</sub> )                            | 1.1V         | 1.1V       | 1.1V         | 1.8V       |
| Initial on/off                                                | On           | On         | On           | On         |
| Mode                                                          | Forced PWM   | Forced PWM | Forced PWM   | Forced PWM |
| Start-up delay/time slot number                               | 15ms/3       | 10ms/2     | 5ms/1        | 0ms/0      |
| Switching frequency (f <sub>sw</sub> )                        | 750kHz       | 750kHz     | 750kHz       | 750kHz     |
| Low-power mode (LPM)                                          | Disabled     | Disabled   | Disabled     | Disabled   |
| Active voltage positioning (AVP) mode                         | Disabled     |            | Disabled     |            |
| Buck parallel mode                                            | Unparalleled |            | Unparalleled |            |
| Software initial I <sup>2</sup> C slave address               | 0x60         |            |              |            |
| V <sub>IN</sub> under-voltage lockout (UVLO) rising threshold | 2.85V        |            |              |            |
| Multiple-time programmable (MTP) configuration code           | 0000         |            |              |            |

## ORDERING INFORMATION

| Part Number*    | Package          | Top Marking | MSL Rating |
|-----------------|------------------|-------------|------------|
| MP5475GU-xxxx** | QFN-35 (5mmx5mm) | See Below   | 1          |
| MP5475GU-0000   |                  |             |            |

\* For Tape & Reel, add suffix -Z (e.g. MP5475GU-xxxx-Z).

\*\* “xxxx” is the configuration code identifier for the register setting stored in the multiple-time programmable (MTP) memory. The default code is “0000”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. The MP5475GU-0000 is the default version.

## TOP MARKING

**MPSYYWW**

**MP5475**

**LLLLLLL**

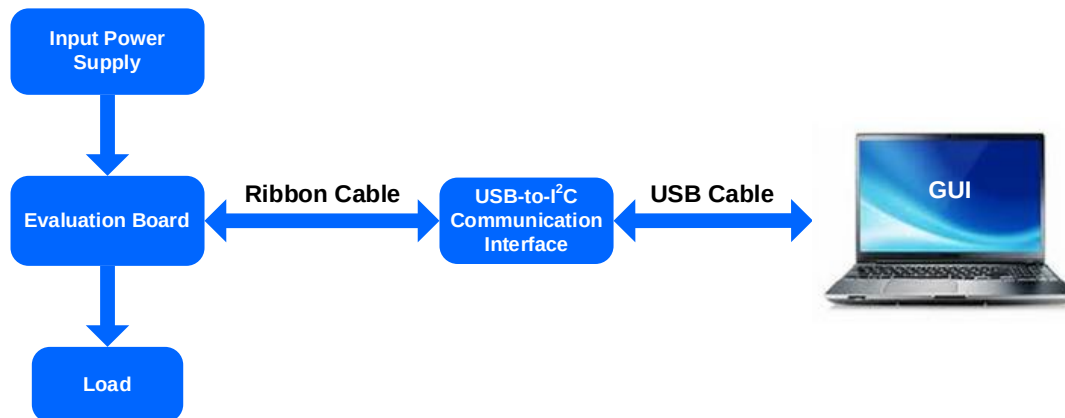
MPS: MPS prefix  
 YY: Year code  
 WW: Week code  
 MP5475: part number  
 LLLLLLL: Lot number

## EVALUATION KIT (EVKT-5475)

EVKT-5475 kit contents (items below can be ordered separately):

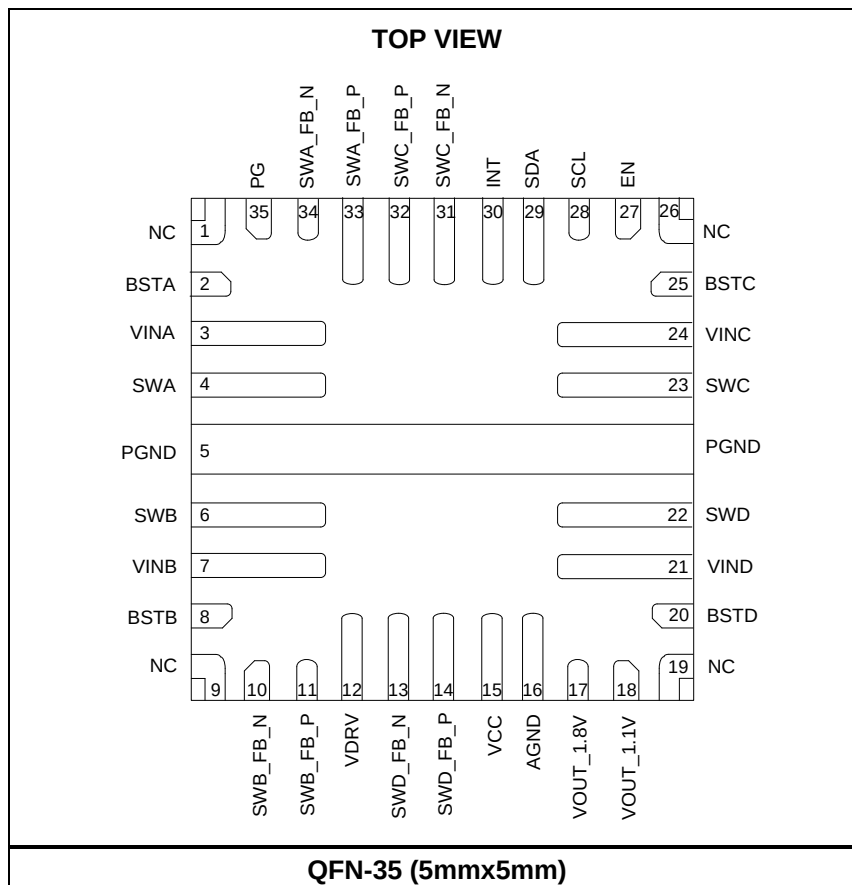
| # | Part Number      | Item                                                                                                     | Quantity |
|---|------------------|----------------------------------------------------------------------------------------------------------|----------|
| 1 | EVL5475-U-00B    | MP5475 evaluation board                                                                                  | 1        |
| 2 | EVKT-USBi2C-02   | Includes one USB-to-I <sup>2</sup> C communication interface device, one USB cable, and one ribbon cable | 1        |
| 3 | MP5475GU-0018    | MP5475 IC (can be used for MTP configuration)                                                            | 2        |
| 4 | Online resources | Includes the datasheet, user guide, product brief, and GUI                                               | 1        |

Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.



**Figure 3: EVKT-5475 Evaluation Kit Set-Up**

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #        | Name      | Description                                                                                                                                                                                                                                                                                                                               |
|--------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 9, 19, 26 | NC        | <b>No connection.</b>                                                                                                                                                                                                                                                                                                                     |
| 2            | BSTA      | <b>Buck converter A (buck A) bootstrap.</b> Connect a capacitor between the SWA and BSTA pins to form a floating supply across buck A's high-side (HS) switch driver.                                                                                                                                                                     |
| 3            | VINA      | <b>Supply voltage input for buck A.</b> A ceramic capacitor is required to decouple the input rail. Connect the VINA pin using a wide PCB trace. VINA, VINB, VINC, and VIND must be connected to the same bus voltage.                                                                                                                    |
| 4            | SWA       | <b>Buck A switch output.</b> Connect the SWA pin using a wide PCB trace.                                                                                                                                                                                                                                                                  |
| 5            | PGND      | <b>Power ground.</b> The PGND pin requires special consideration during PCB layout. Connect the PGND pin with copper traces and vias.                                                                                                                                                                                                     |
| 6            | SWB       | <b>Buck converter B (buck B) switch output.</b> Connect the SWB pin using a wide PCB trace.                                                                                                                                                                                                                                               |
| 7            | VINB      | <b>Supply voltage input for buck B.</b> A ceramic capacitor is required to decouple the input rail. Connect the VINB pin using a wide PCB trace.                                                                                                                                                                                          |
| 8            | BSTB      | <b>Buck B bootstrap.</b> Connect a capacitor between the SWB and BSTB pins to form a floating supply across buck B's HS switch driver.                                                                                                                                                                                                    |
| 10           | SWB_FB_N  | <b>Negative feedback for buck B.</b> Kelvin connect the SWB_FB_N pin to the ground node of the output capacitor (C <sub>OUT</sub> ) on buck B.                                                                                                                                                                                            |
| 11           | SWB_FB_P  | <b>Positive feedback for buck B.</b> Connect buck B's output to the SWB_FB_P pin directly.                                                                                                                                                                                                                                                |
| 12           | VDRV      | <b>3.3V supply input to the power management IC (PMIC).</b> Connect a 3.3V power supply to the VDRV pin. If there is no external 3.3V power supply, connect this pin to VCC.                                                                                                                                                              |
| 13           | SWD_FB_N  | <b>Remote sense ground for buck converter D (buck D).</b> Kelvin connect the SWD_FB_N pin to the ground node of C <sub>OUT</sub> on buck D.                                                                                                                                                                                               |
| 14           | SWD_FB_P  | <b>Positive feedback for buck D.</b> Connect buck D's output to the SWD_FB_P pin directly.                                                                                                                                                                                                                                                |
| 15           | VCC       | <b>Internal 3.3V low-dropout (LDO) output.</b> The driver and control circuits are powered from the VCC pin voltage (V <sub>CC</sub> ). Decouple VCC with a 1μF ceramic capacitor placed as close to the pin as possible. Ceramic capacitors with X7R or X5R dielectrics are recommended due to their stable temperature characteristics. |
| 16           | AGND      | <b>Analog ground.</b> Connect AGND to the power ground pin.                                                                                                                                                                                                                                                                               |
| 17           | VOUT_1.8V | <b>1.8V LDO output from the PMIC.</b>                                                                                                                                                                                                                                                                                                     |
| 18           | VOUT_1.1V | <b>1.1V LDO output from the PMIC.</b>                                                                                                                                                                                                                                                                                                     |
| 20           | BSTD      | <b>Buck D bootstrap.</b> Connect a capacitor between SWD and BSTD pins to form a floating supply across buck D's HS switch driver.                                                                                                                                                                                                        |
| 21           | VIND      | <b>Supply voltage input for buck D.</b> A ceramic capacitor is required to decouple the input rail. Connect the VIND pin using a wide PCB trace.                                                                                                                                                                                          |
| 22           | SWD       | <b>Buck D switch output.</b> Connect the SWD pin using a wide PCB trace.                                                                                                                                                                                                                                                                  |
| 23           | SWC       | <b>Buck converter C (buck C) switch output.</b> Connect the SWC pin using a wide PCB trace.                                                                                                                                                                                                                                               |
| 24           | VINC      | <b>Supply voltage input for buck C.</b> A ceramic capacitor is required to decouple the input rail. Connect the VINC pin using a wide PCB trace.                                                                                                                                                                                          |
| 25           | BSTC      | <b>Buck C bootstrap.</b> Connect a capacitor between the SWC and BSTC pins to form a floating supply across the buck C's HS switch.                                                                                                                                                                                                       |
| 27           | EN        | <b>Enable control.</b> Apply a logic low-to-high transition to the EN pin to enable the PMIC.                                                                                                                                                                                                                                             |



## PIN FUNCTIONS *(continued)*

| Pin # | Name     | Description                                                                                                                                                                                                                                                              |
|-------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28    | SCL      | I <sup>2</sup> C bus clock.                                                                                                                                                                                                                                              |
| 29    | SDA      | I <sup>2</sup> C bus data.                                                                                                                                                                                                                                               |
| 30    | INT      | <b>General status interrupt.</b> The INT pin is an open-drain output. The MP5475 asserts INT low to communicate any single (or more) critical event(s) to the host. INT remains asserted until the appropriate registers are explicitly cleared, or the MP5475 is reset. |
| 31    | SWC_FB_N | <b>Remote-sense ground for buck C.</b> Kelvin connect the SWC_FB_N pin to the ground node of C <sub>OUT</sub> on buck C.                                                                                                                                                 |
| 32    | SWC_FB_P | <b>Positive feedback for buck C.</b> Connect buck C's output to the SWC_FB_P pin directly.                                                                                                                                                                               |
| 33    | SWA_FB_P | <b>Positive feedback for buck A.</b> Connect buck A's output to the SWA_FB_P pin directly. SWA_FB_P is the feedback input of the dual-phase buck when buck A and buck B are set to dual-phase interleaving mode.                                                         |
| 34    | SWA_FB_N | <b>Remote-sense ground of buck A and buck B.</b> Kelvin connect the SWA_FB_N pin to ground node of C <sub>OUT</sub> on buck A and buck B.                                                                                                                                |
| 35    | PG       | <b>Open-drain power good (PG) output.</b> Pull the PG pin low when any enabled regulator falls below its under-voltage (UV) threshold. Pull PG low when all regulators are disabled.                                                                                     |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                        |                                 |
|----------------------------------------|---------------------------------|
| Supply voltage (V <sub>INx</sub> )     | 18V                             |
| V <sub>SWx_DC</sub>                    | -0.3V to V <sub>IN</sub> + 0.3V |
| V <sub>BSTx</sub>                      | V <sub>SW</sub> + 4V            |
| V <sub>CC</sub>                        | 4.3V                            |
| All other pins                         | -0.3V to V <sub>CC</sub>        |
| Junction temperature (T <sub>J</sub> ) | 170°C                           |
| Lead temperature                       | 260°C                           |
| Storage temperature                    | -65°C to +170°C                 |

## ESD Ratings <sup>(2)</sup>

|                            |        |
|----------------------------|--------|
| Human body model (HBM)     | ±2000V |
| Charged-device model (CDM) | ±750V  |

## Recommended Operating Conditions <sup>(3)</sup>

|                                                         |                                       |
|---------------------------------------------------------|---------------------------------------|
| Supply voltage (V <sub>INx</sub> ) (x = A, B, C, or D)  | 3V to 16V                             |
| V <sub>IN_DC</sub> - V <sub>SW_DC</sub> <sup>(4)</sup>  | -0.3V to V <sub>IN</sub> + 0.3V       |
| V <sub>SW_DC</sub> <sup>(4)</sup>                       | -0.3V to V <sub>IN</sub> + 0.3V       |
| Output voltage (V <sub>OUTx</sub> ) (x = A, B, C, or D) | Refer to the I <sup>2</sup> C setting |
| Operating junction temp (T <sub>J</sub> )               | -40°C to +125°C                       |

## Thermal Resistance

 $\theta_{JA}$   $\theta_{JC}$ 

QFN-35 (5mmx5mm)

EV5475-U-00A <sup>(5)</sup> 25.....2.5 .. °C/W

JESD51-7 <sup>(6)</sup> 29.....18.1 . °C/W

### Notes:

- Exceeding these ratings may damage the device.
- HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
- The device is not guaranteed to function outside of its operating conditions.
- The voltage rating can be between -3V and +23V for a period of 25ns or shorter with a maximum repetition rate of 1000kHz when V<sub>IN</sub> is 16V.
- Measured on the EV5475-U-00A, 4-layer PCB.
- Measured on a JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 12V, T<sub>J</sub> = -40°C to +125°C, typical values are tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                                                | Symbol                    | Condition                                                            | Min  | Typ  | Max  | Units                 |
|------------------------------------------------------------------------------------------|---------------------------|----------------------------------------------------------------------|------|------|------|-----------------------|
| Default switching frequency                                                              | f <sub>SW</sub>           |                                                                      | 850  | 1000 | 1150 | kHz                   |
| EN rising threshold                                                                      | V <sub>EN</sub>           |                                                                      | 1.21 | 1.25 | 1.29 | V                     |
| EN hysteresis                                                                            | V <sub>EN_HYS</sub>       |                                                                      |      | 220  |      | mV                    |
| EN pull-down resistor                                                                    | R <sub>EN</sub>           |                                                                      |      | 2.2  |      | MΩ                    |
| <b>Step-Down Regulators</b>                                                              |                           |                                                                      |      |      |      |                       |
| V <sub>INx</sub> under-voltage lockout (UVLO) rising threshold (where x = A, B, C, or D) | V <sub>INx_UVLO_R</sub>   |                                                                      | 2.75 | 2.85 | 2.95 | V                     |
| V <sub>INx</sub> UVLO hysteresis                                                         | V <sub>INx_UVLO_HYS</sub> |                                                                      |      | 250  |      | mV                    |
| V <sub>INx</sub> over-voltage (OV) rising threshold                                      |                           |                                                                      | 16   | 16.6 | 17.5 | V                     |
| V <sub>INx</sub> OV hysteresis                                                           |                           |                                                                      |      | 650  |      | mV                    |
| Feedback (FB) voltage accuracy                                                           | V <sub>FB1</sub>          | Default output of buck converter A (buck A), T <sub>J</sub> = 25°C   | -1%  | 1.1  | +1%  | V                     |
|                                                                                          | V <sub>FB2</sub>          | Default output of buck converter B (buck B), T <sub>J</sub> = 25°C   | -1%  | 1.1  | +1%  | V                     |
|                                                                                          | V <sub>FB3</sub>          | Default output of buck converter C (buck C), T <sub>J</sub> = 25°C   | -1%  | 1.1  | +1%  | V                     |
|                                                                                          | V <sub>FB4</sub>          | Default output of buck converter D (buck D), T <sub>J</sub> = 25°C   | -1%  | 1.8  | +1%  | V                     |
| FB under-voltage (UV) threshold 1 (low to high) <sup>(7)</sup>                           |                           | Hiccup entry (FB UV with OC for 50 cycles)                           |      | 80   |      | % of V <sub>REF</sub> |
| FB UV threshold 2 (high to low) <sup>(7)</sup>                                           |                           | Hiccup entry (FB UV with 2.5μs deglitch)                             |      | 75   |      | % of V <sub>REF</sub> |
| <b>Buck A, Buck B, Buck C, and Buck D</b>                                                |                           |                                                                      |      |      |      |                       |
| High-side MOSFET (HS-FET) on resistance                                                  | R <sub>DS(ON)_HS1</sub>   | For buck A/B/C/D                                                     |      | 15   |      | mΩ                    |
| Low-side MOSFET (LS-FET) on resistance                                                   | R <sub>DS(ON)_LS1</sub>   | For buck A/B/C/D                                                     |      | 5    |      | mΩ                    |
| Switch leakage                                                                           | SW <sub>ILK1</sub>        | T <sub>J</sub> = 25°C                                                |      | 0    | 1    | μA                    |
| Low-side (LS) current limit (source)                                                     | I <sub>LS_VALLEY1</sub>   | Valley limit is independent of the high-side (HS) peak current limit | 6    | 7    | 8    | A                     |
| Negative current limit                                                                   | I <sub>NOCP</sub>         | Forced pulse-width modulation (PWM)/OVP discharge                    |      | -5   |      | A                     |
| Minimum on time <sup>(7)</sup>                                                           | t <sub>ON_MIN1</sub>      |                                                                      |      | 20   |      | ns                    |
| Minimum off time <sup>(7)</sup>                                                          | t <sub>OFF_MIN1</sub>     |                                                                      |      | 100  |      | ns                    |
| Output over-voltage protection (OVP) rising threshold                                    | V <sub>OVP1_H</sub>       |                                                                      | 117  | 122  | 127  | % of V <sub>REF</sub> |
| Output OVP recovery threshold                                                            | V <sub>OVP1_L</sub>       |                                                                      |      | 110  |      | % of V <sub>REF</sub> |
| Buck A soft-start time                                                                   | t <sub>SS_B1</sub>        | Default, V <sub>OUT</sub> = 10% to 90%                               |      | 0.88 |      | ms                    |
| Buck B soft-start time                                                                   | t <sub>SS_B2</sub>        | Default, V <sub>OUT</sub> = 10% to 90%                               |      | 0.88 |      | ms                    |

# ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, T<sub>J</sub> = -40°C to +125°C, typical values are tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                              | Symbol                | Condition                                     | Min | Typ  | Max | Units                 |
|--------------------------------------------------------|-----------------------|-----------------------------------------------|-----|------|-----|-----------------------|
| Buck C soft-start time                                 | t <sub>SS_B3</sub>    | Default, V <sub>OUT</sub> = 10% to 90%        |     | 0.88 |     | ms                    |
| Buck D soft-start time                                 | t <sub>SS_B4</sub>    | Default, V <sub>OUT</sub> = 10% to 90%        |     | 1.44 |     | ms                    |
| <b>Low-Dropout (LDO) Regulator</b>                     |                       |                                               |     |      |     |                       |
| VDRV voltage (V <sub>DRV</sub> ) UVLO rising threshold |                       |                                               | 2.8 | 3    | 3.2 | V                     |
| V <sub>DRV</sub> UVLO falling threshold                |                       |                                               | 2.6 | 2.8  | 3   | V                     |
| V <sub>DRV</sub> OV rising threshold                   |                       |                                               | 3.4 | 3.6  | 3.8 | V                     |
| V <sub>DRV</sub> OV hysteresis                         |                       |                                               |     | 250  |     | mV                    |
| <b>50mA, 1.1V Low-Dropout (LDO) Regulator</b>          |                       |                                               |     |      |     |                       |
| Default output voltage                                 | V <sub>1V1</sub>      | I <sub>OUT</sub> = 0A to 20mA, power-on state | -5% | 1.1  | +5% | V                     |
| Current limit                                          | I <sub>LIM_1V1</sub>  |                                               | 50  | 70   |     | mA                    |
| <b>50mA, 1.8V Low-Dropout (LDO) Regulator</b>          |                       |                                               |     |      |     |                       |
| Default output voltage                                 | V <sub>1V8</sub>      | I <sub>OUT</sub> = 0A to 20mA, power-on state | -5% | 1.8  | +5% | V                     |
| Current limit                                          | I <sub>LIM_1V8</sub>  |                                               | 50  | 70   |     | mA                    |
| <b>Power Good (PG) and Interrupt (INT)</b>             |                       |                                               |     |      |     |                       |
| PG UV rising threshold                                 | V <sub>PG_UV_R</sub>  |                                               | 86  | 90   | 94  | % of V <sub>REF</sub> |
| PG UV falling threshold                                | V <sub>PG_UV_F</sub>  |                                               |     | 78   |     | % of V <sub>REF</sub> |
| PG OV rising threshold                                 | V <sub>PG_OV_R</sub>  |                                               | 117 | 122  | 127 | % of V <sub>REF</sub> |
| PG OV falling threshold                                | V <sub>PG_OV_F</sub>  |                                               |     | 110  |     | % of V <sub>REF</sub> |
| PG rising delay <sup>(7)</sup>                         | t <sub>PG_R_DLY</sub> |                                               |     | 500  |     | μs                    |
| PG falling delay <sup>(7)</sup>                        | t <sub>PG_F_DLY</sub> |                                               |     | 50   |     | μs                    |
| PG output port sink current capability                 | V <sub>PG_SINK</sub>  | Sink 1mA                                      |     |      | 0.4 | V                     |
| INT output port sink current capability                | V <sub>INT_SINK</sub> | Sink 1mA                                      |     |      | 0.4 | V                     |
| <b>VCC Regulator</b>                                   |                       |                                               |     |      |     |                       |
| VCC voltage                                            | V <sub>CC</sub>       | I <sub>CC</sub> = 25mA                        |     | 3.5  |     | V                     |
| VCC voltage regulation                                 | V <sub>CC_RG</sub>    | I <sub>CC</sub> = 0mA to 25mA                 |     | 1    |     | %                     |
| <b>Temperature Protection</b>                          |                       |                                               |     |      |     |                       |
| Thermal shutdown <sup>(7)</sup>                        | T <sub>OTP_R</sub>    |                                               |     | 150  |     | °C                    |
| Thermal hysteresis <sup>(7)</sup>                      | T <sub>HYS</sub>      |                                               |     | 20   |     | °C                    |
| <b>I<sup>2</sup>C Signals</b>                          |                       |                                               |     |      |     |                       |
| Input high voltage (SDA or SCL)                        | V <sub>IH</sub>       |                                               | 1.4 |      |     | V                     |
| Input low voltage (SDA or SCL)                         | V <sub>IL</sub>       |                                               |     |      | 0.4 | V                     |

## I<sup>2</sup>C PORT SIGNAL CHARACTERISTICS <sup>(7)</sup>

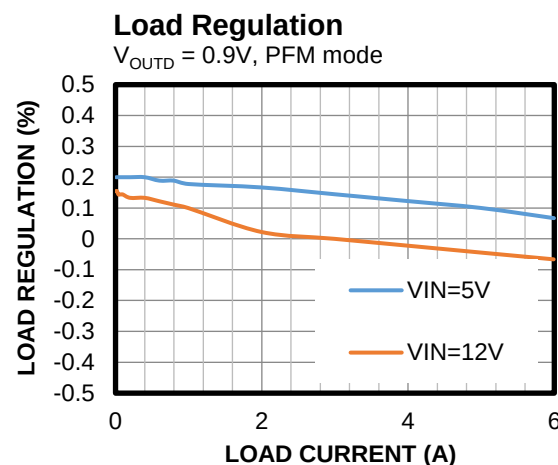
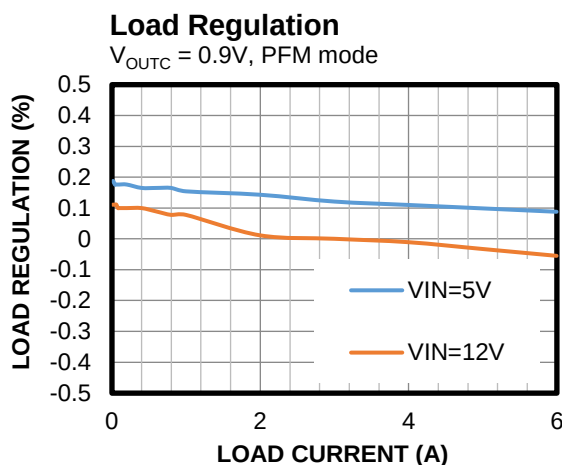
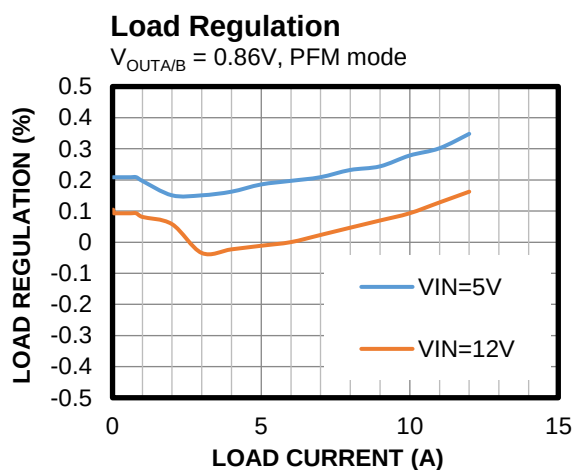
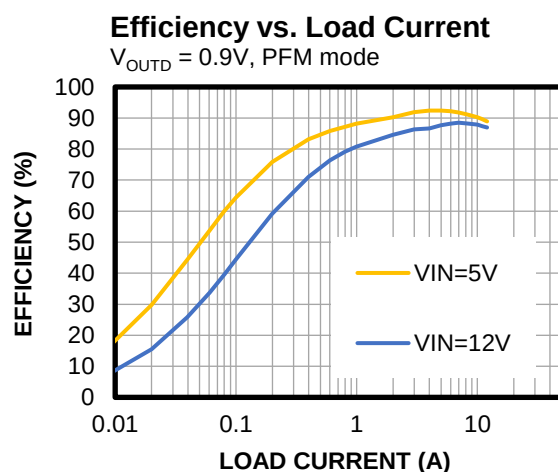
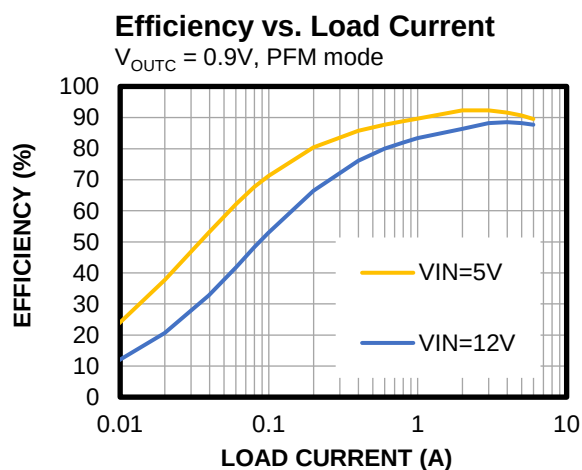
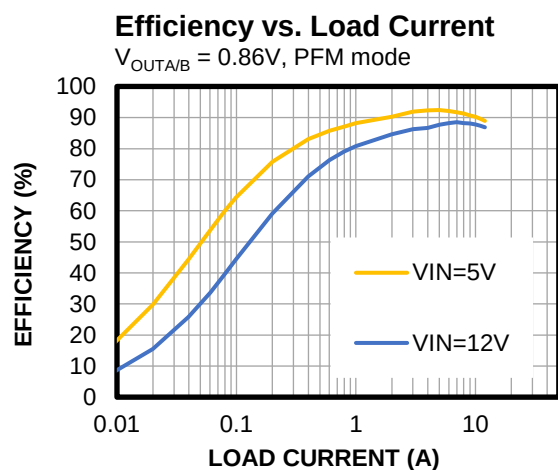
| Parameter                                                                            | Symbol              | Condition                        | C <sub>B</sub> = 100pF |     | C <sub>B</sub> = 400pF |     | Units |
|--------------------------------------------------------------------------------------|---------------------|----------------------------------|------------------------|-----|------------------------|-----|-------|
|                                                                                      |                     |                                  | Min                    | Max | Min                    | Max |       |
| SCLH and SCL clock frequency                                                         | f <sub>SCHL</sub>   |                                  | 0                      | 3.4 | 0                      | 0.4 | MHz   |
| Set-up time for a repeated start command                                             | t <sub>SU_STA</sub> |                                  | 160                    |     | 600                    |     | ns    |
| Hold time for a (repeated) start command                                             | t <sub>HD_STA</sub> |                                  | 160                    |     | 600                    |     | ns    |
| Low period of the SCL clock                                                          | t <sub>LOW</sub>    |                                  | 160                    |     | 1300                   |     | ns    |
| High period of the SCL clock                                                         | t <sub>HIGH</sub>   |                                  | 60                     |     | 600                    |     | ns    |
| Data set-up time                                                                     | t <sub>SU_DAT</sub> |                                  | 0                      | 10  |                        |     | ns    |
| Data hold time                                                                       | t <sub>HD_DAT</sub> |                                  | 0                      | 70  |                        |     | ns    |
| Rising time of the SCLH signal                                                       | t <sub>R_CL</sub>   |                                  | 10                     | 40  | 20 x 0.1C <sub>B</sub> | 300 | ns    |
| Rising time of the SCLH signal after a repeated start command and an acknowledge bit | t <sub>F_CL1</sub>  |                                  | 10                     | 80  | 20 x 0.1C <sub>B</sub> | 300 | ns    |
| Falling time of the SCLH signal                                                      | t <sub>F_CL</sub>   |                                  | 10                     | 40  | 20 x 0.1C <sub>B</sub> | 300 | ns    |
| Rising time of the SDAH signal                                                       | t <sub>F_DA</sub>   |                                  | 10                     | 80  | 20 x 0.1C <sub>B</sub> | 300 | ns    |
| Falling time of the SDAH signal                                                      | t <sub>F_DA</sub>   |                                  | 10                     | 80  | 20 x 0.1C <sub>B</sub> | 300 | ns    |
| Set-up time for stop command                                                         | t <sub>SU_STO</sub> |                                  | 160                    |     | 600                    |     | ns    |
| Bus free time between a stop and start command                                       | t <sub>BUF</sub>    |                                  | 160                    |     | 1300                   |     | ns    |
| Data valid time                                                                      | t <sub>VD_DAT</sub> |                                  |                        | 16  |                        | 90  | ns    |
| Data valid acknowledge time                                                          | t <sub>VD_ACK</sub> |                                  |                        | 160 |                        | 900 | ns    |
| Capacitive load for each bus line                                                    | C <sub>B</sub>      | SDAH and SCLH line               |                        | 100 |                        | 400 | pF    |
|                                                                                      |                     | SDAH + SDA line, SCLH + SCL line |                        | 400 |                        | 400 | pF    |

### Note:

7) Guaranteed by design.

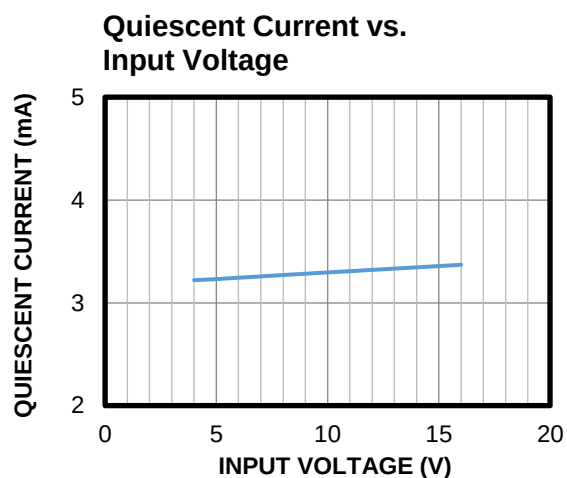
# TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = 25^{\circ}C$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $T_J = 25^{\circ}C$ , unless otherwise noted.

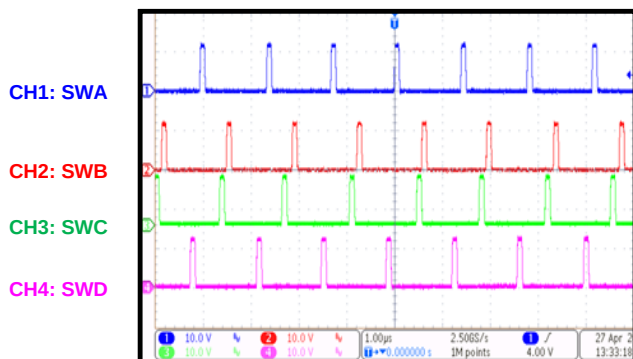


# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = 25^{\circ}C$ , unless otherwise noted.

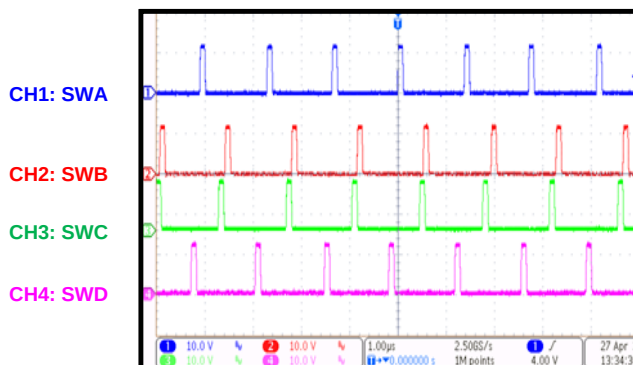
## Steady State

Each buck channel with half load



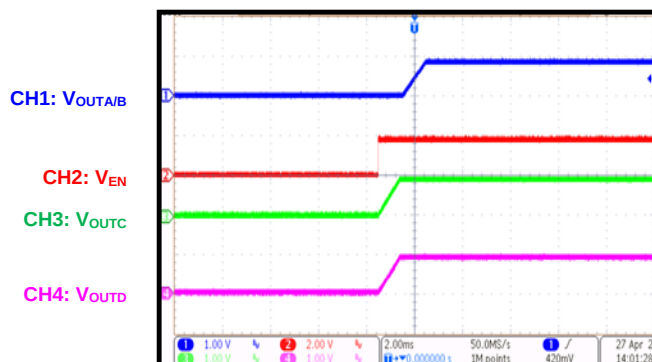
## Steady State

Each buck channel with full load



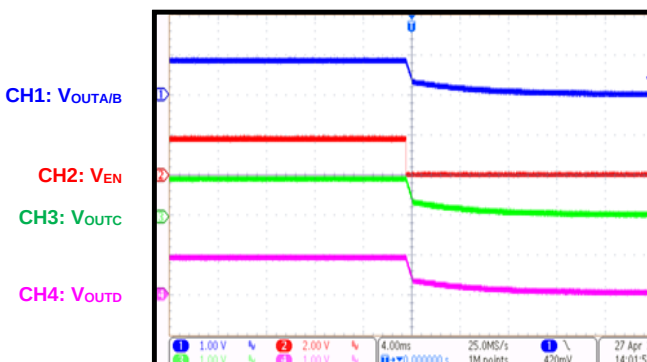
## Start-Up through EN

Each buck channel without load



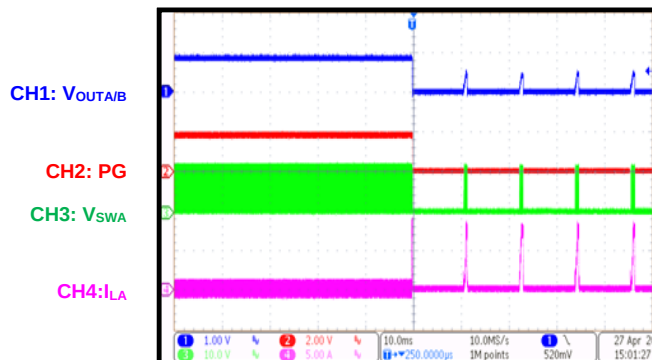
## Shutdown through EN

Each buck channel without load



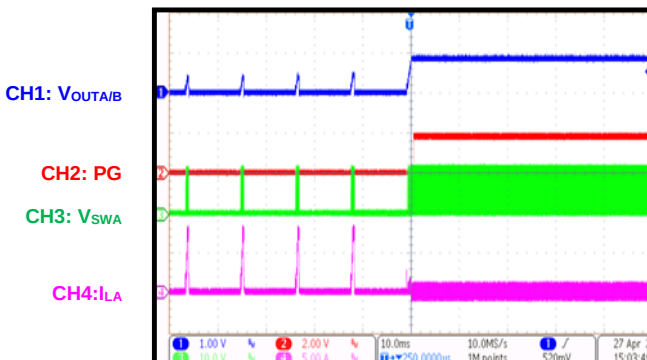
## SCP Entry

Buck A/B output = 0.86V,  $I_{OUT} = 0A$



## SCP Recovery

Buck A/B output = 0.86V,  $I_{OUT} = 0A$

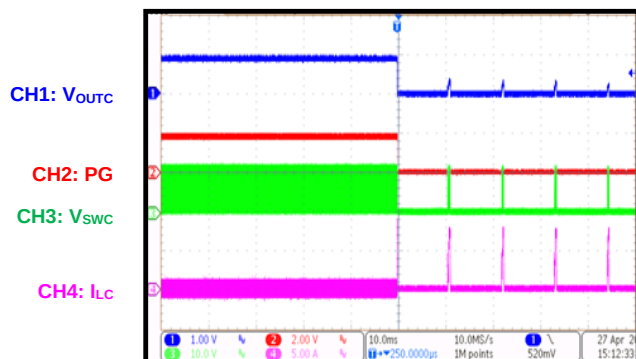


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, T<sub>J</sub> = 25°C, unless otherwise noted.

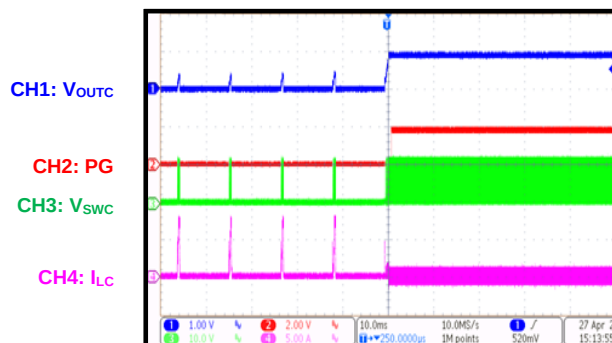
## SCP Entry

Buck C output = 0.9V, I<sub>OUT</sub> = 0A



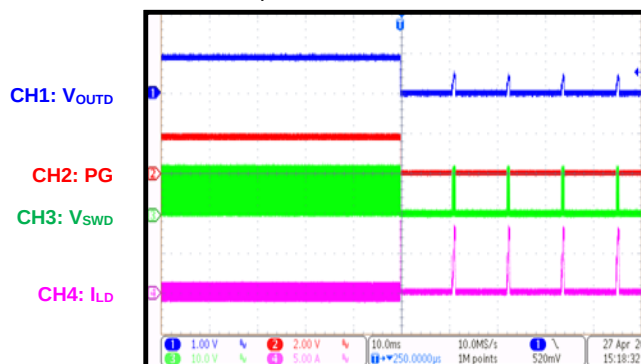
## SCP Recovery

Buck C output = 0.9V, I<sub>OUT</sub> = 0A



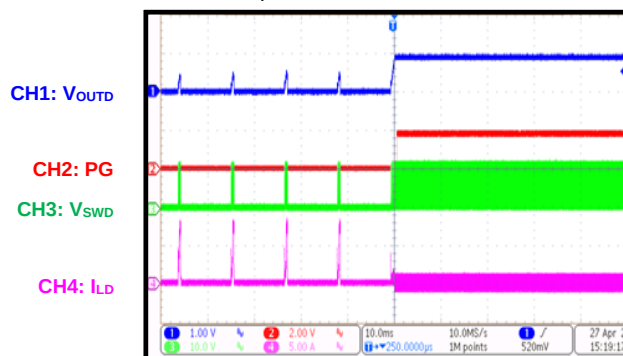
## SCP Entry

Buck D output = 0.9V, I<sub>OUT</sub> = 0A



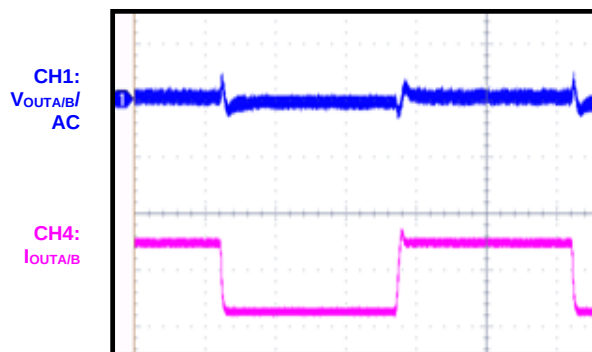
## SCP Recovery

Buck D output = 0.9V, I<sub>OUT</sub> = 0A



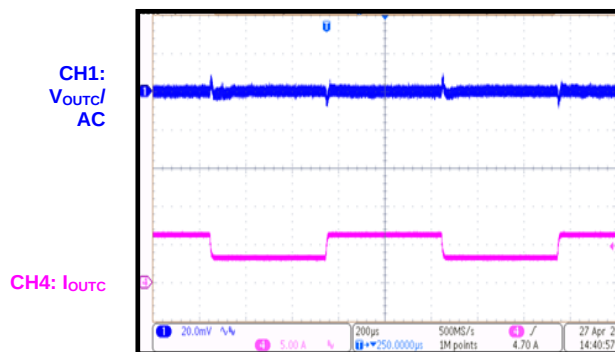
## Load Transient Reponse

I<sub>OUT</sub> = 6A to 12A, slew rate is 2.5A/μs by e-load



## Load Transient Response

I<sub>OUT</sub> = 3A to 6A, slew rate is 2.5A/μs by e-load



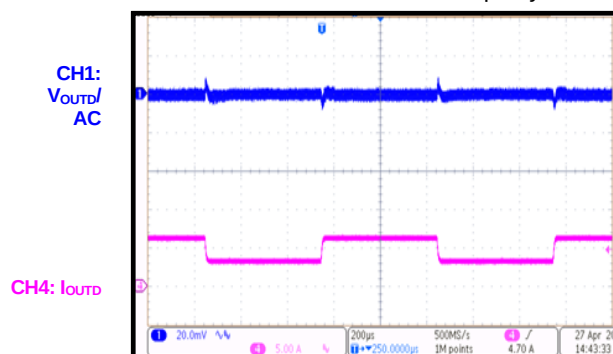


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $T_J = 25^{\circ}C$ , unless otherwise noted.

### Load Transient Response

$I_{OUT} = 3A$  to  $6A$ , slew rate is  $2.5A/\mu s$  by e-load



# FUNCTIONAL BLOCK DIAGRAM

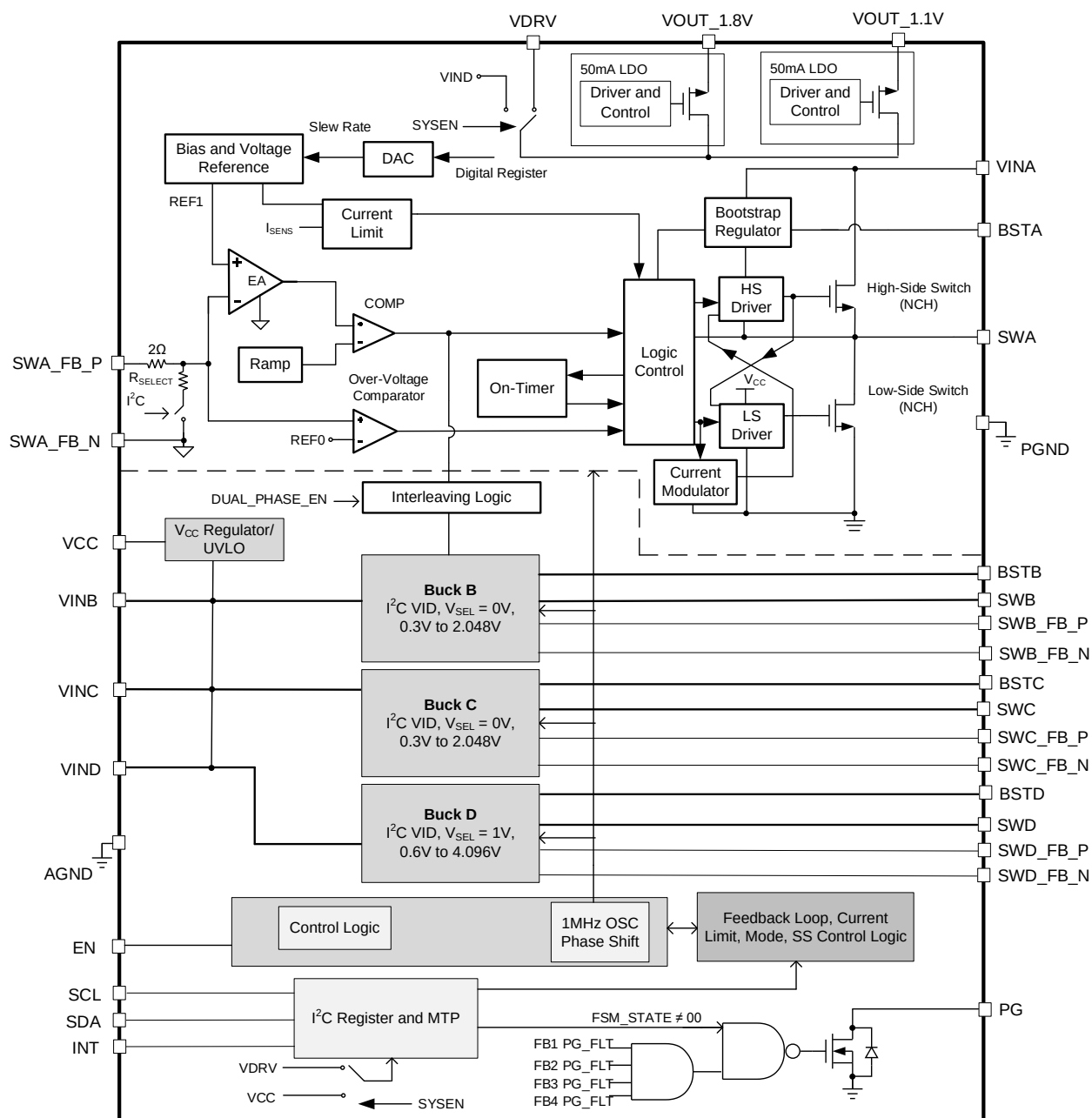


Figure 4: Functional Block Diagram

## OPERATION

### High-Efficiency Buck Converters

Buck converter A (buck A), buck converter B (buck B), buck converter C (buck C), and buck converter D (buck D) are synchronous, step-down DC/DC converters with built-in soft-start (SS), compensation, and current-limit protection with hiccup mode. Fixed-frequency constant-on-time (COT) control provides fast transient response. The switching clock is locked and phase-shifted from buck A to buck D in continuous conduction mode (CCM).

### POWER CONTROL

#### State Machine Diagram

The state machine has a number of statuses, described below (see Figure 5).

#### No Supply

The MP5475's input pin has an under-voltage lockout (UVLO) detection circuit. If the input voltage ( $V_{INx}$ ) (where  $x = A, B, C, \text{ or } D$ ) and the  $V_{DRV}$  voltage ( $V_{DRV}$ ), are below their respective UVLO rising thresholds, all the MP5475's functions are disabled.

#### Management State

After  $V_{DRV}$  exceeds its UVLO threshold, and before  $SYSEN$  is set, the MP5475 enters the management state. In the management state, the  $V_{INx}$  range is defined by  $V_{DRV}$ . The two low-dropout (LDO) regulator outputs,  $V_{OUT\_1.8V}$  and  $V_{OUT\_1.1V}$ , are enabled automatically when  $V_{DRV}$  reaches its UVLO rising threshold.

#### Power Off

If an over-temperature (OT) condition is triggered when  $V_{IN}$  exceeds its rising UVLO threshold, the MP5475 enters the power-off state. The MP5475 always monitors the power-on factor. If the power-on factor is detected after the MP5475's temperature drops below the falling threshold while in the power-off state, then the MP5475 enters the power-on sequence state.

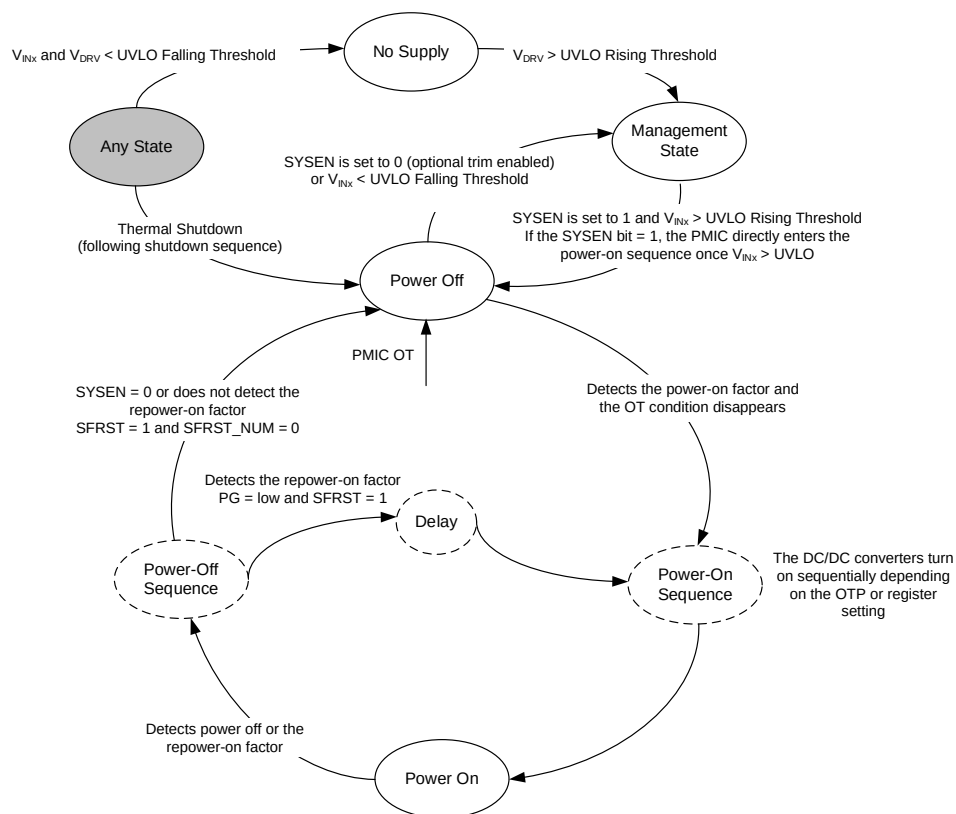


Figure 5: Power Control State Machine Diagram

### **Power Supply and Under-Voltage Lockout (UVLO)**

$V_{INA}$  is the power supply for buck A;  $V_{INB}$  is the power supply for buck B;  $V_{INC}$  is the power supply for buck C;  $V_{IND}$  is the power supply for buck D. It is recommended to connect the  $V_{INA}$ ,  $V_{INB}$ ,  $V_{INC}$ , and  $V_{IND}$  pins together during application. When  $V_{INx}$  exceeds its UVLO rising threshold, the corresponding buck starts up. The buck shuts down when  $V_{INx}$  drops below the UVLO falling threshold. See Figure 5 on page 19 for more details regarding the power-on sequence state.

### **Power-On Sequence**

The DC/DC converters turn on sequentially according to the pre-configured order set via the multiple-time programmable (MTP) memory.

### **Power On**

The DC/DC converter turns on. In this state, the MP5475 is always monitoring the power-off factor or repower-on factor.

### **Power-Off Sequence**

The MP5475 initiates the power-off sequence when it detects the power-off factor or repower-on factor in the power-on state. Set the SFRST bit to 1 when the PG pin goes low, then the DC/DC converters shut down sequentially following the power-off sequence. After the power-off sequence is completed, the PMIC automatically enters the power-on sequence after a timer delay.

Set the SFRST bit to 1 when PG is high, then wait until PG goes low for the DC/DC converters to shut down sequentially following the power-off sequence.

### **Shutdown Event**

If the PMIC detects that both  $V_{INx}$  and  $V_{DRV}$  have fallen below their respective UVLO thresholds, the MP5475 changes to a no supply state, regardless of the current state.

### **Power-On Factors**

After  $V_{INx}$  and  $V_{DRV}$  exceed their respective ULVO thresholds, apply a logic low-to-high

transition to the EN pin. The MP5475 has a few power-on factors, described below.

### **SYSEN**

SYSEN is 1 data bit in the I<sup>2</sup>C register. If it is set to 1, the system changes from the power-off state to the power-on sequence. There are two ways to set SYSEN from 0 to 1:

- If the SYSEN bit is set to 1 via the MTP, the system automatically loads the SYSEN bit into the SYSEN I<sup>2</sup>C register when  $V_{INx}$  crosses its UVLO threshold.
- After the MP5475 enters the management state, write the SYSEN bit to 1 via the I<sup>2</sup>C to enable the buck converter.

### **Thermal Protection Recovery**

If the MP5475 is in a power-off state due to the die temperature exceeding the thermal protection threshold, then the MP5475 enters the power-on sequence automatically once the die temperature decreases.

### **Power-On Sequence**

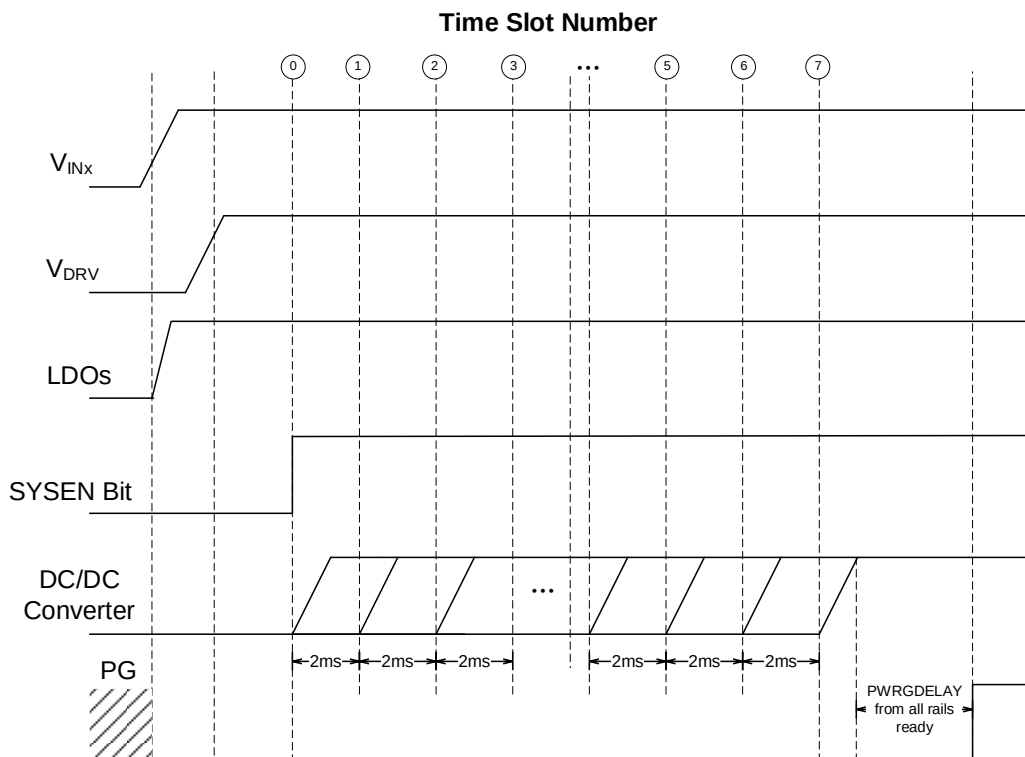
There are 8 slots for power-on sequence timing. All the converters can be configured to time slots 0 to 7 via the MTP. The delay time between each time slot is configured by the 3-bit register TS\_INTERVAL (see Table 1).

**Table 1: Slot Time Interval**

| TS_INTERVAL | Time Delay between Each Slot |
|-------------|------------------------------|
| 000         | 10ms                         |
| 001         | 5ms                          |
| 010         | 2ms                          |
| 011         | 1ms                          |
| 100         | 500μs                        |
| 101         | 200μs                        |

Figure 6 on page 21 and Figure 7 on page 22 show the MP5475's power-on sequence when power is first applied. The platform may power up  $V_{INx}$  and  $V_{DRV}$  supplies in any sequence.

Figure 6 on page 21 shows  $V_{INx}$  supply ramping before the  $V_{DRV}$  supply.



**Figure 6: Power-On Sequence (V<sub>INx</sub> Ready before V<sub>DRV</sub>)**

Figure 7 on page 22 shows the V<sub>DRV</sub> supply ramping up before the V<sub>INx</sub> supply. The PMIC does not mandate any specific timing relationship between the V<sub>INx</sub> and V<sub>DRV</sub> supplies.

Once either the V<sub>INx</sub> or V<sub>DRV</sub> supply is valid and stable, the MP5475 drives the LDO output supplies, VOUT\_1.8V and VOUT\_1.1V, to the load devices for LDO (SPD, TS, and RCD).

The PMIC has an automatic internal supply switch-over function from the V<sub>DRV</sub> input supply

to the V<sub>INx</sub> input supply. The input supply switch-over function is only applicable after the MP5475 has registered the SYSEN command. The MP5475 triggers the switch-over to the V<sub>INx</sub> input supply when the V<sub>DRV</sub> input drops below the 3V threshold. The internal input supply switch-over is for the MP5475's LDO outputs (VOUT\_1.8V and VOUT\_1.1V) and its I<sup>2</sup>C. The PMIC's I<sup>2</sup>C stays active when the MP5475 switches over to the V<sub>INx</sub> input supply.

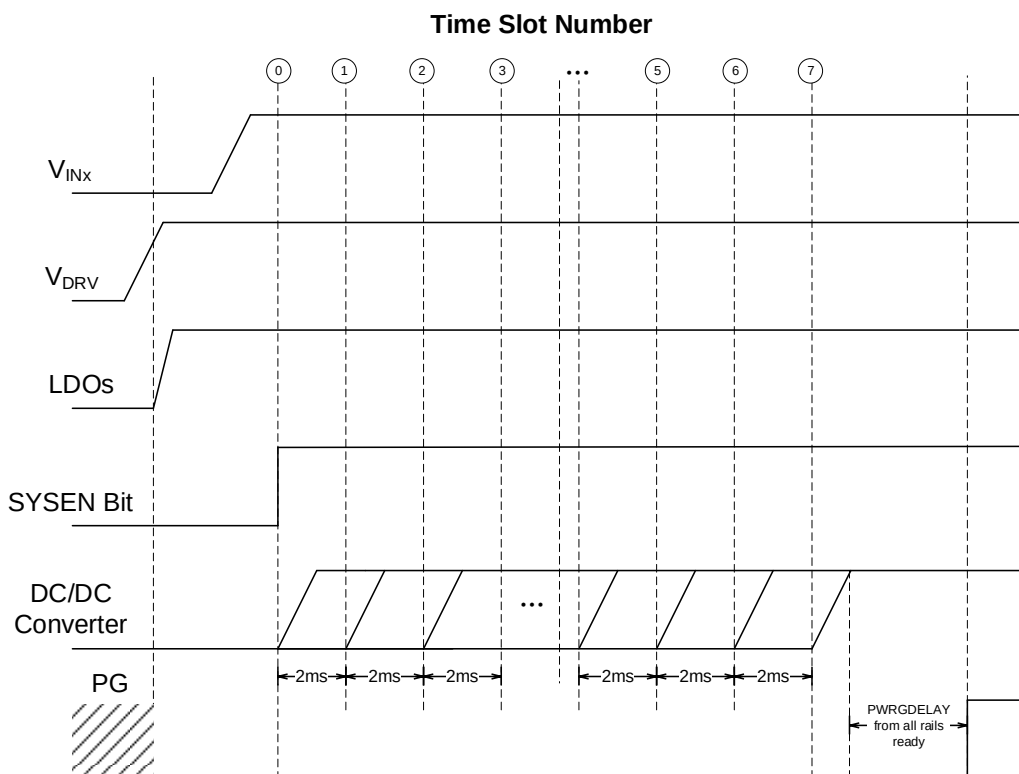


Figure 7: Power-On Sequence ( $V_{DRV}$  Ready before  $V_{INx}$ )

## Power-Off Factors

### **SYSEN – Software-Initiated Power Off (Trim Enable Function)**

The MP5475 supports a software-controlled power off via the I<sup>2</sup>C interface. The SYSEN is 1 data bit in the I<sup>2</sup>C register. If the SYSEN bit is set to 0, the system enters a power-off sequence (trim enabled).

### **Thermal Protection Entry**

If the MP5475's silicon die temperature exceeds the thermal protection threshold, the system enters a power-off state. In this scenario, the MP5475 enters the shutdown sequence instead of the power-off sequence and finally remains in the power-off state. For more details, see the Shutdown Sequence section on page 25.

### **$V_{INx}$ Under-Voltage Lockout (UVLO)**

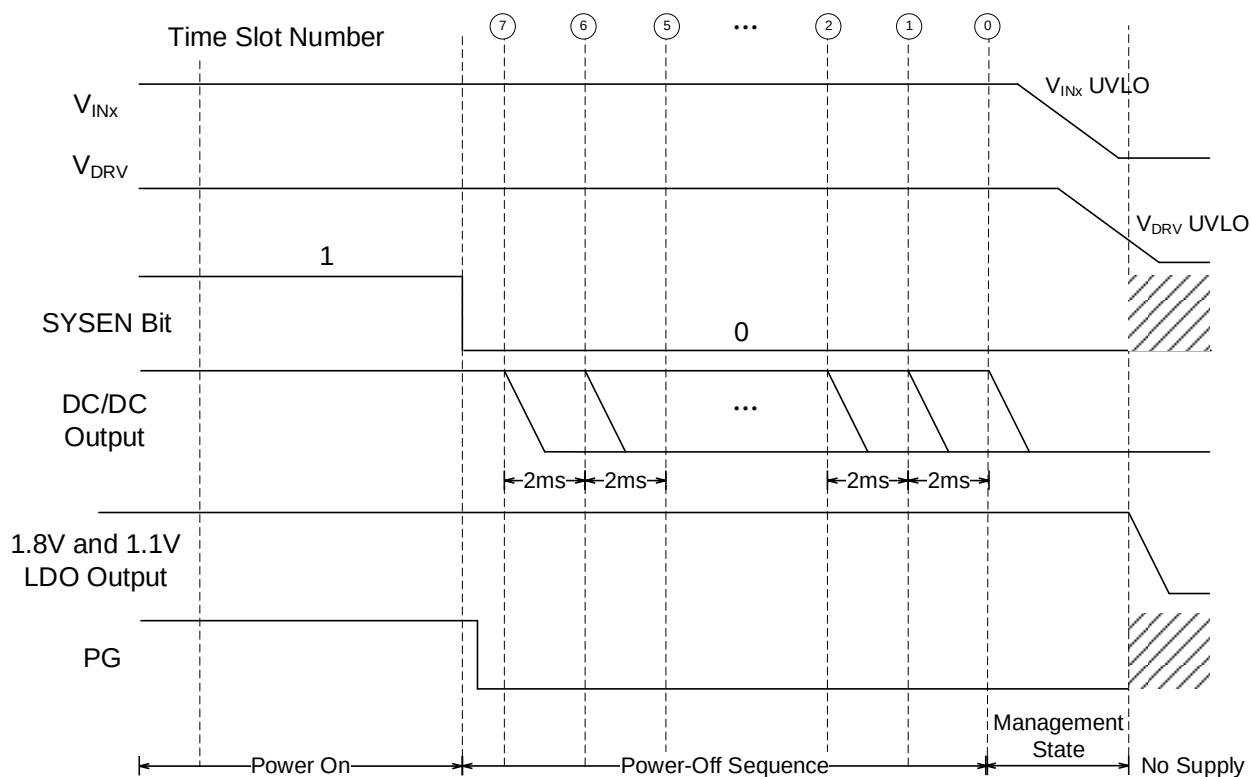
If the MP5475's  $V_{INx}$  falls below its UVLO falling threshold while  $V_{DRV}$  is still active, the system

enters a power-off state. In this scenario, the MP5475 enters the shutdown sequence instead of the power-off sequence and finally remains in the power-off state. For more details, see the Shutdown Sequence section on page 25.

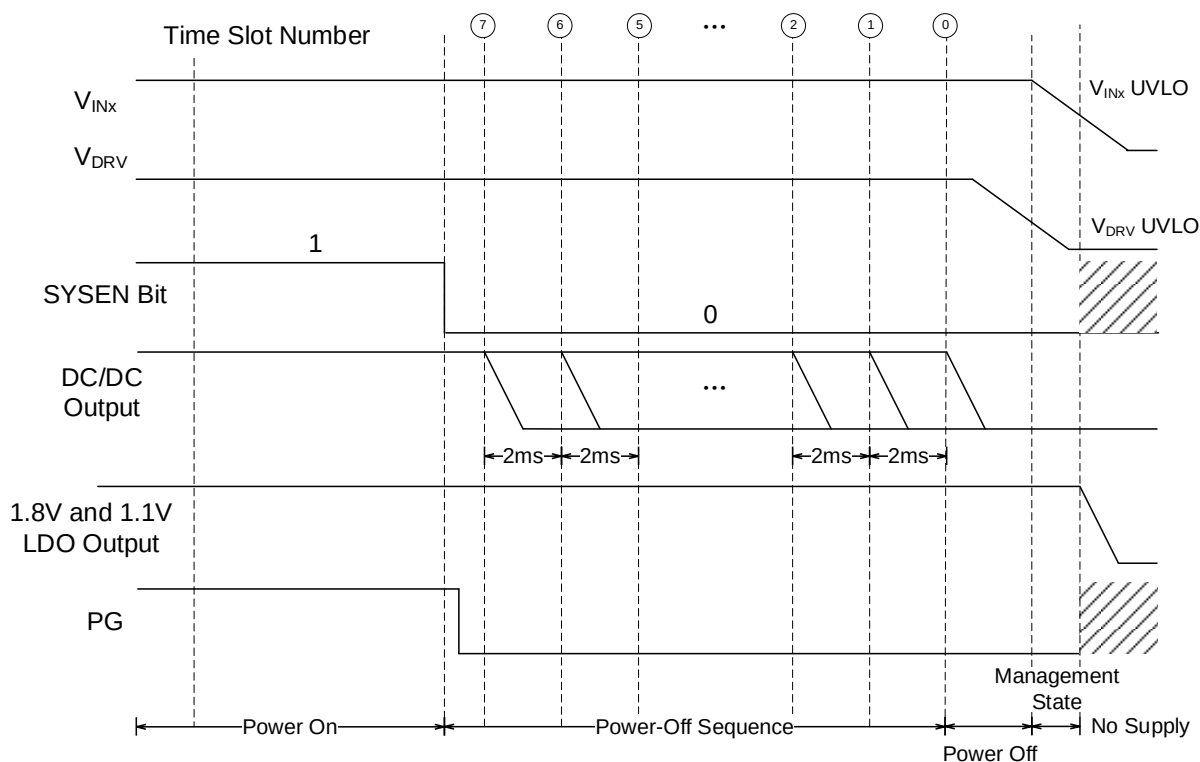
### **Power-Off Sequence (Enabled by the Trim SYSEN Off Function)**

The PG pin pulls low before the DC/DC converter initiates shutdown. The converter's power-off sequence is determined by the shutdown delay registers (11h, 19h, 21h, and 29h).

Figure 8 on page 23 shows the power-off sequence via the SYSEN bit when  $V_{DRV}$  turns off before  $V_{INx}$ . Figure 9 on page 23 shows the power-off sequence via the SYSEN bit when  $V_{INx}$  turns off before  $V_{DRV}$ .



**Figure 8: Power-Off Sequence via the SYSEN Bit ( $V_{INx}$  Off before  $V_{DRV}$ )**



**Figure 9: Power-Off Sequence via the SYSEN Bit ( $V_{DRV}$  Off before  $V_{INx}$ )**

## Repower-On Factor

### Manual Reset (SFRST)

It is possible to manually reset the device with a software reset. If the SFRST bit is set to 1 via the I<sup>2</sup>C and the PG pin is low, the system detects this as a repower-on factor.

### Repower-On Sequence (Software-Initiated Power Cycle)

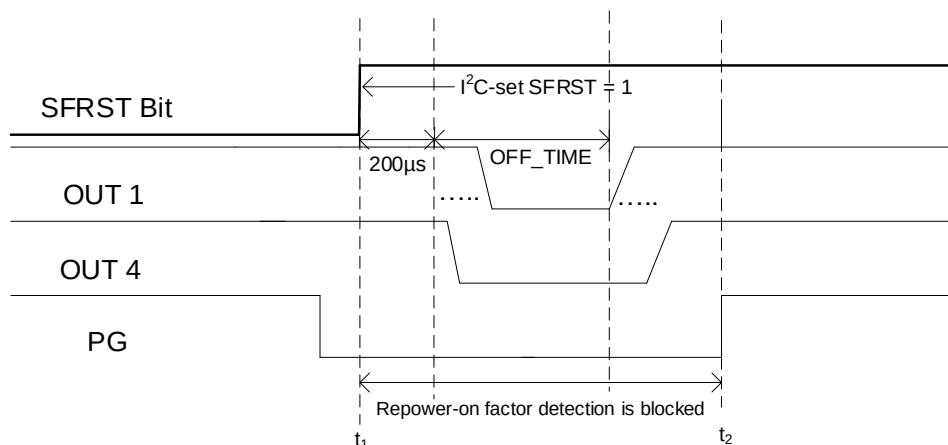
The MP5475 supports a software-controlled power reset via the I<sup>2</sup>C interface.

When using the software-controlled method, the SFRST bit is set high when the PG pin is low. The MP5475 waits for 200μs, then powers off the system. If the SFRST\_NUM bit is not set to 0 after the delay time (set via the OFF\_TIME register), then all the power rails power on again (see Figure 10).

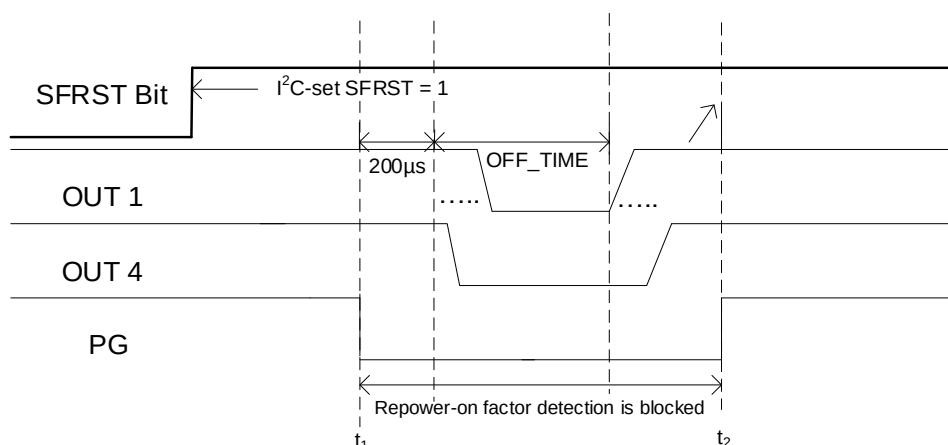
When setting the SFRST bit high while PG is high, the MP5475 does not enter the repower-on sequence until PG goes low (see Figure 11).

After the repower-on sequence finishes, the SFRST\_NUM value is set by register 43h, bits[2:0] - 1. If SFRST\_NUM drops to 0 during the repower-on sequence, the MP5475 remains in the power-off state the next time a repower-on event occurs. There are two ways to restart the MP5475:

- Toggle V<sub>INx</sub> to below its UVLO threshold and ramp up.
- Configure SFRST\_NUM to a non-zero value.



**Figure 10: Repower-On Sequence (Set the SFRST Bit while PG Is Low)**



**Figure 11: Repower-On Sequence (Set the SFRST Bit while PG Is High)**



## Shutdown Sequence

When  $V_{INx}$  drops below its UVLO falling threshold or the MP5475 has an OT condition, the MP5475

enters the shutdown sequence directly. All the DC/DC converters turn off at the same time following the soft-stop ramping down slew rate (see Figure 12).

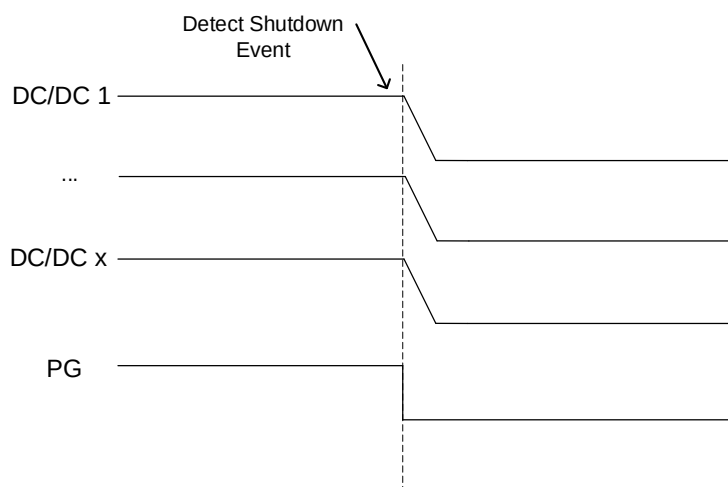


Figure 12: Shutdown Sequence

## Thermal Shutdown

The MP5475 employs thermal shutdown by internally monitoring the IC's junction temperature ( $T_J$ ). If  $T_J$  exceeds the 150°C threshold, the converter shuts off following the soft-stop ramping down slew rate. This is a non-latch protection. There is a 20°C hysteresis. Once  $T_J$  drops to about 130°C, the MP5475 initiates a soft start.

## Pre-Biased Start-Up

The MP5475 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a set voltage during start-up, the internal bootstrap (BST) voltage ( $V_{BST}$ ) is refreshed and charged, as well as the voltage on the internal soft-start capacitor ( $C_{SS}$ ). If  $V_{BST}$  exceeds its rising threshold and the  $C_{SS}$  voltage exceeds the sensed output voltage ( $V_{OUTx}$ ) (where  $x = A, B, C, \text{ or } D$ ) at the FB pin, then the MP5475 starts to work normally.

## Power Good (PG)

The MP5475 provides a power good (PG) output to indicate whether the enabled buck's  $V_{OUTx}$  is ready. The PG pin is an open-drain output. Connect the PG pin to VCC or another voltage source through a pull-up resistor (e.g. 10kΩ).

If the FB voltage ( $V_{FB}$ ) exceeds 92% of the reference voltage ( $V_{REF}$ ), the PG pin pulls high after a 500μs default time (or another MTP-configured delay time). During normal operation, the PG pin pulls low when any enabled regulator falls below the UV threshold with a 50μs delay. The PG pin pulls low when all converters are disabled.

If UVLO occurs,  $SYSEN = 0$ , or over-temperature protection (OTP) occurs, then the PG pin pulls low immediately. If an over-current (OC) condition occurs, the PG pin pulls low when  $V_{FB}$  drops below 87% of  $V_{REF}$  after a 50μs delay.

## General Status Interrupt (INT)

The MP5475 provides an interrupt control unit that is responsible for asserting and de-asserting the INT pin to the application host.

If the related interrupt is unmasked, it propagates to the INT pin. If the related interrupt is masked, the assertion of an interrupt from the masked register does not cause the IRQ signal to assert.

INT asserts low until all the interrupt events are removed. Figure 13 on page 26 shows the IRQ architecture block diagram.

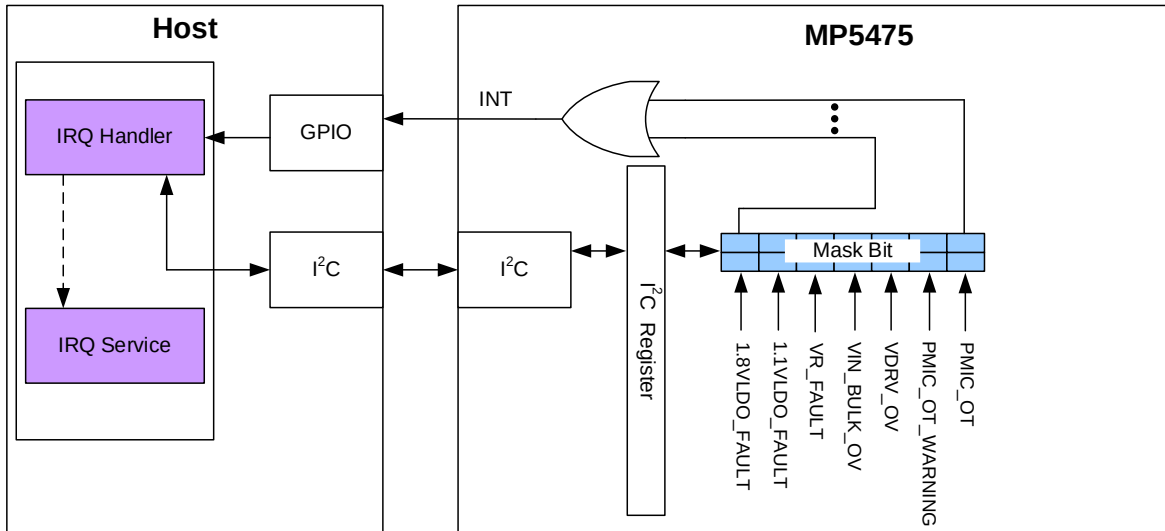


Figure 13: IRQ Architecture Block Diagram

### Output Over-Voltage Protection (OVP)

The MP5475 monitors  $V_{OUTx}$  and enters over-voltage protection (OVP) discharge mode once  $V_{OUTx}$  exceeds 122% of its regulation voltage for longer than 2 $\mu$ s. In OVP discharge mode, the low-side MOSFET (LS-FET) turns on and stays on until the LS-FET's current reaches the negative current limit. This discharges the output to keep  $V_{OUTx}$  within its normal range. If the OV condition still exists, the LS-FET turns on again after a fixed delay to repeat the discharge behavior.

The MP5475 exits this discharge mode when  $V_{FB}$  drops below 110% of  $V_{REF}$ .

If the MP5475's  $V_{INx}$  exceeds the input OVP threshold by 14.5V during OVP discharge mode, then the MP5475 shuts down until  $V_{INx}$  drops below 14.2V, after which the MP5475 restarts. Input OVP is only active when under an output OV condition.

OVP can be enabled or disabled via the I<sup>2</sup>C and MTP interface.

### Input Over-Voltage Protection (OVP)

The MP5475 monitors  $V_{INx}$  and enters OVP mode once  $V_{INx}$  exceeds 16.6V. In OVP mode, the MP5475 cannot enter forced continuous conduction mode (FCCM), which means that there is no soft shutdown when the device shuts down.

The MP5475 exits this mode when  $V_{INx}$  drops below 16V.

### Output Discharge

To discharge the energy of the output capacitor ( $C_{OUT}$ ) during the power-off sequence or shutdown sequence, there are discharge paths both from the SWx and FBx pins to ground. The discharge function can be enabled or disabled via the I<sup>2</sup>C and MTP interface.

### Soft Start (SS) and Soft Shutdown

The MP5475 employs a soft-start and soft shutdown mechanism to ensure a smooth output during start-up and shutdown.

When the MP5475 is enabled and  $V_{BST}$  reaches its rising threshold, the internal digital-to-analog converter (DAC) outputs a ramp voltage ( $V_{REF}$ ).  $V_{OUTx}$  smoothly ramps up with  $V_{REF}$ . Once the DAC output reaches the final voltage, it maintains a steady voltage. At this point, soft start finishes, and the MP5475 enters steady state operation.

When the MP5475 is disabled, the internal DAC ramps down  $V_{REF}$ .  $V_{OUTx}$  follows the soft-shutdown slew rate with  $V_{REF}$  until the output drops to 0.3V. Then soft shutdown stops and the MP5475's output is discharged by the FB pin's discharge FET, if the discharge function is enabled.

The start-up delay, shutdown delay, soft-start and soft-shutdown slew rate can be configured via the MTP.

## Out-of-Phase Operation

Buck A, buck B, buck C, and buck D are frequency-locked and phase-shifted. Figure 14 shows the phase shift's default definition, which can also be changed via the MTP.

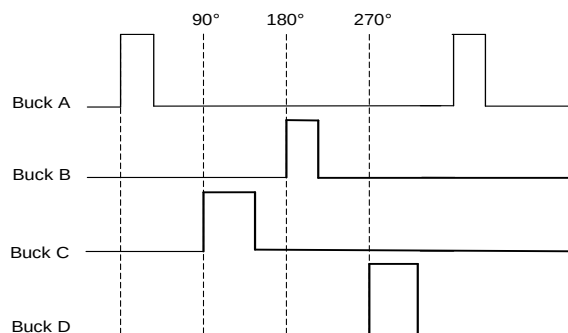


Figure 13: Phase-Shift Functional Diagram

## Interleaving for Dual-Rail Mode

When interleaving mode is enabled, the MP5475's buck A/B and buck C/D operate with dual-phase interleaving (see Figure 14).

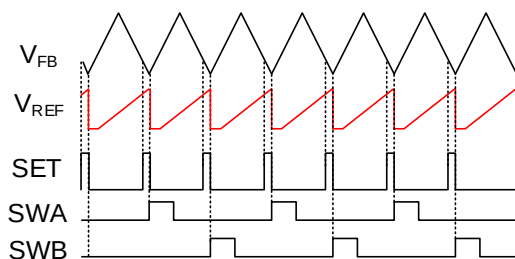


Figure 14: Interleaving for Dual-Rail Mode Diagram

The SET signal is triggered by comparing  $V_{FB}$  and  $V_{REF}$ . When the SET signal goes high, only one phase's pulse-width modulation (PWM) output becomes high; the next time SET goes high, the next phase's PWM output goes high. This achieves interleaving.

## Current Balancing

When buck A and buck B work in dual-phase interleaving mode, the MP5475 senses two phase currents and auto-tunes buck A and buck B's on time ( $t_{ON}$ ) to achieve current balancing.

## Active Voltage Positioning (AVP)

When buck A and buck B (or buck C and buck D) work in dual-phase interleaving mode, the MP5475 supports active voltage positioning (AVP) by setting the AVP\_EN bit to 1 via the I<sup>2</sup>C. An internal current-sense circuit generates the droop current ( $I_{DROOP}$ ) source, which is

proportional to the internal sensing current.  $I_{DROOP}$  is injected into the FB pin to produce the feedback (FB) voltage ( $V_{FBx}$ ) with a droop voltage.

## VCC Regulator

A 3.5V internal regulator powers most of the internal circuitry. A decoupling capacitor is required to stabilize the regulator and reduce the ripple. This regulator takes the VINA input and operates across the full  $V_{INA}$  range.

## Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP5475 provides valley current limit control. While the LS-FET turns on, the inductor current ( $I_L$ ) is monitored. If the sensed  $I_L$  exceeds the valley current limit threshold, the device enters over-current protection (OCP) mode. The high-side MOSFET (HS-FET) cannot turn on until the valley current limit disappears. Meanwhile,  $V_{OUTx}$  drops until it falls below the under-voltage (UV) threshold.

If an UV and OC condition are both triggered, the MP5475 enters hiccup mode to periodically restart the related power rail. The hiccup duty cycle is very small to reduce the power dissipation during a short-circuit condition. During OCP, the device tries to recover from the OC fault with hiccup mode. That means that the chip disables the output power stage, discharges  $C_{SS}$ , and then automatically tries to soft start again. If the OC condition still exists when soft start elapses, the device repeats this operation. OCP is a non-latch protection.

## Multiple-Time Programmable (MTP) Configuration

The I<sup>2</sup>C and MTP blocks are active once  $V_{DRV}$  exceeds its UVLO rising threshold.

When  $V_{DRV}$  starts up the MP5475, the MTP data is loaded into the corresponding I<sup>2</sup>C registers during the first start-up, and the I<sup>2</sup>C registers directly control buck A to buck D's parameters. The I<sup>2</sup>C register and MTP table share the same register address.

After the MP5475's  $V_{DRV}$  and  $V_{INx}$  start up, the system-on-chip (SoC) configures the MP5475's I<sup>2</sup>C register and MTP.

When the SoC writes to the I<sup>2</sup>C register, the I<sup>2</sup>C register takes effect immediately; this setting can also be burned into the MTP. During normal buck

operation, the I<sup>2</sup>C master can read and write to the register's data online.

## Safety Considerations for Writing to the MTP

Several protection items can reduce the failure rate of MTP writing. Figure 15 shows how to configure the MTP, and follow the three steps below to write to the MTP registers:

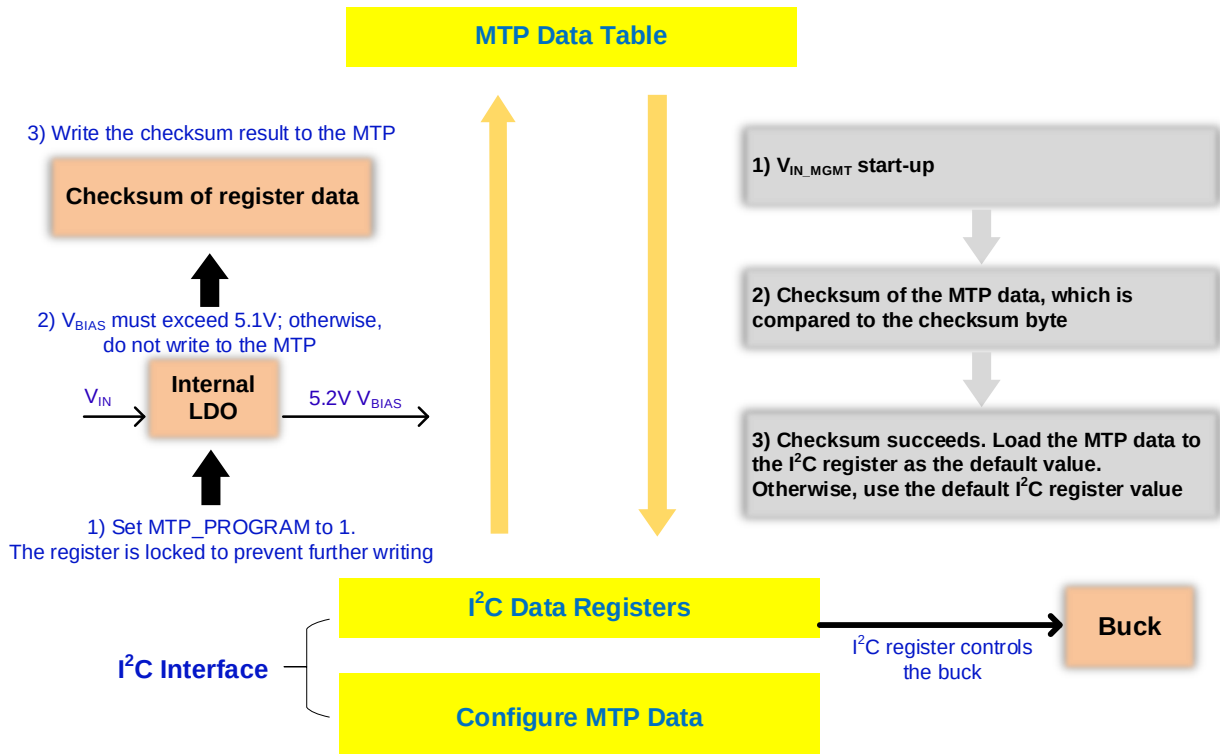
1. Set MTP\_PROGRAM to 1. The I<sup>2</sup>C register is locked to prevent write operations until MTP configuring finishes, but the SoC can read the I<sup>2</sup>C register during this period.
2. The MP5475 checks the MTP's burning power supply. If this supply exceeds 5.1V, MTP writing continues; otherwise, abort and unlock the I<sup>2</sup>C write protection.
3. The MP5475 calculates the sum of all related I<sup>2</sup>C registers that are burnt into the MTP register, then generates 8-bit checksum data. The sum is not a true sum of all I<sup>2</sup>C registers. Rather, it is an arithmetic to combine all the data. The checksum result is written to the MTP register as well.

After MTP write operation finishes (typically after about 100ms), the MP5475 sets MTP\_PROGRAM to 0. I<sup>2</sup>C register write protection is unlocked. The MTP device configuration specification is up to 0.5mA/bit for 50ms. This means that two configuration cycles with less current requires about 100ms.

The SoC can read the register; if the MTP\_PROGRAM goes to 0, this indicates that the MTP configuration is done.

After MTP write operation finishes, the system SoC can read the MTP register data to confirm that the correct value is saved to the MTP registers. If anything is wrong, the SoC writes to the MTP again.

During  $V_{IN}$  start-up, before loading the MTP data into the I<sup>2</sup>C register, the MP5475 executes a checksum calculation for all related MTP registers, then compare this value with the checksum byte. If they match, then MTP data is loaded to the I<sup>2</sup>C register; Otherwise, the I<sup>2</sup>C register uses a hard-coded default value. An I<sup>2</sup>C/register flag bit is available to indicate whether this is a checksum error.



### Figure 15: MTP Configuration

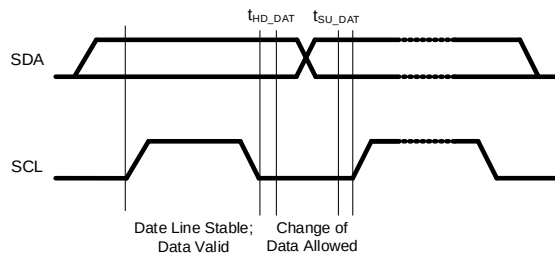
## I<sup>2</sup>C INTERFACE

### I<sup>2</sup>C Serial Interface

The I<sup>2</sup>C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MP5475 interface is an I<sup>2</sup>C slave. The I<sup>2</sup>C adds flexibility to the power supply solution. V<sub>OUTx</sub>, the transition slew rate, and other parameters can be controlled by the I<sup>2</sup>C instantaneously.

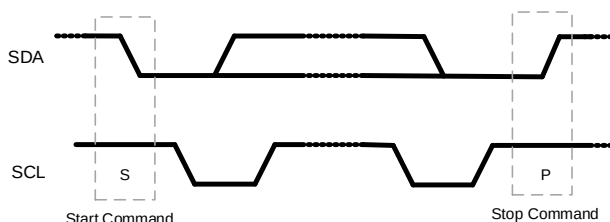
### Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The high or low state of the data line can only change after the clock signal on the SCL line stays low for no shorter than maximum data hold time (t<sub>HD\_DAT</sub>), and also no longer than the maximum data set-up time (t<sub>SU\_DAT</sub>) before the next SCL clock starts (see Figure 16).



**Figure 16: Bit Transfer on the I<sup>2</sup>C Bus**

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I<sup>2</sup>C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 17).



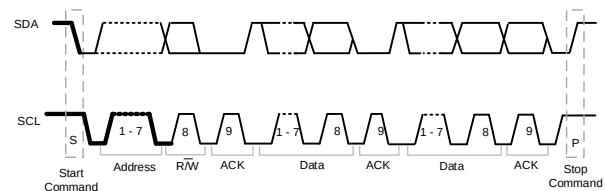
**Figure 17: Start and Stop Commands**

Start and stop commands are always generated by the master. The bus is busy after the start condition, and it is considered to be free again after the stop command. The bus remains busy if a repeated start (Sr) is generated instead of a stop command. The start and repeated start commands are functionally identical.

### Transfer Data

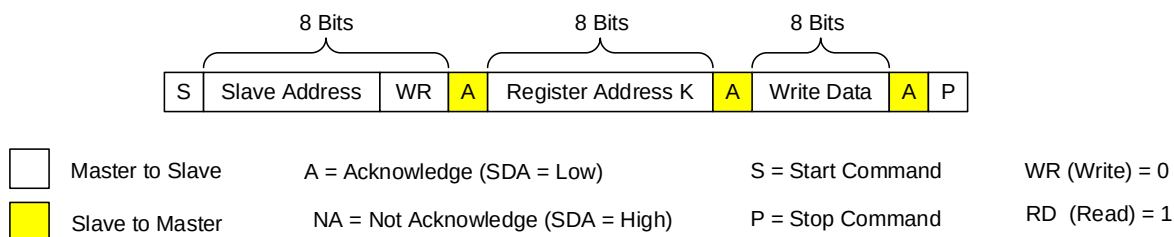
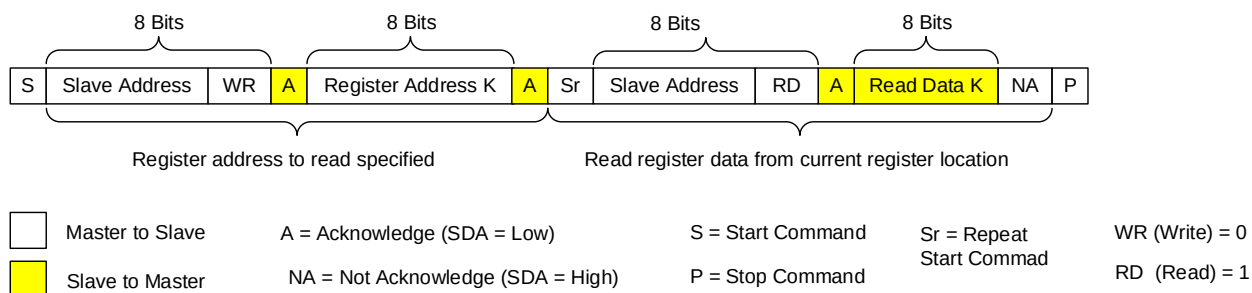
Every byte put on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the clock pulse's high period.

Figure 18 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If the master still wants to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.



**Figure 18: A Complete Data Transfer**

Figure 19 on page 30 shows an I<sup>2</sup>C write example for a single register. Figure 20 on page 30 shows an I<sup>2</sup>C read example for a single register.


**Figure 19: I<sup>2</sup>C Write Single Register Example**

**Figure 20: I<sup>2</sup>C Read Single Register Example**



## REGISTER MAP

### MTP CONFIGURATION TABLE

| Scope  | REG (0x) | D[7]            | D[6]              | D[5]           | D[4]            | D[3]             | D[2]                  | D[1]        | D[0]         |
|--------|----------|-----------------|-------------------|----------------|-----------------|------------------|-----------------------|-------------|--------------|
| Buck A | 10 (WR)  | DUAL_PHASE_ENA  | SOFT_START_DELAYA |                |                 | SOFT_START_TIMEA |                       |             |              |
|        | 11 (WR)  | SHUTDOWN_DELAYA |                   |                | SOFT_STOP_TIMEA |                  | VOUT_TRANSITION_RATEA |             |              |
|        | 12 (WR)  | VOUT_LIMIT_ENA  | MODEA             | CURRENT_LIMITA |                 | VOUT_OVP_ENA     | PHASE_DELAY_SELECTA   |             | VOUT_DIS_ENA |
|        | 13 (WR)  | VOUT_SELECTA    | RESERVED          |                |                 |                  |                       | V_REFA_HIGH |              |
|        | 14 (WR)  | V_REFA_LOW      |                   |                |                 |                  |                       |             |              |
|        | 15 (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
|        | 16 (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
|        | 17 (WR)  | AVP_ENA         | AVP_GAINA         |                |                 | AVP_TRIMA        |                       |             |              |
| Buck B | 18 (WR)  | RESERVED        | SOFT_START_DELAYB |                |                 | SOFT_START_TIMEB |                       |             |              |
|        | 19 (WR)  | SHUTDOWN_DELAYB |                   |                | SOFT_STOP_TIMEB |                  | VOUT_TRANSITION_RATEB |             |              |
|        | 1A (WR)  | VOUT_LIMIT_ENB  | MODEB             | CURRENT_LIMITB |                 | VOUT_OVP_ENB     | PHASE_DELAY_SELECTB   |             | VOUT_DIS_ENB |
|        | 1B (WR)  | VOUT_SELECTB    | RESERVED          |                |                 |                  |                       | V_REFB_HIGH |              |
|        | 1C (WR)  | V_REFB_LOW      |                   |                |                 |                  |                       |             |              |
|        | 1D (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
|        | 1E (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
| Buck C | 20 (WR)  | DUAL_PHASE_ENC  | SOFT_START_DELAYC |                |                 | SOFT_START_TIMEC |                       |             |              |
|        | 21 (WR)  | SHUTDOWN_DELAYC |                   |                | SOFT_STOP_TIMEC |                  | VOUT_TRANSITION_RATEC |             |              |
|        | 22 (WR)  | VOUT_LIMIT_ENC  | MODEC             | CURRENT_LIMITC |                 | VOUT_OVP_ENC     | PHASE_DELAY_SELECTC   |             | VOUT_DIS_ENC |
|        | 23 (WR)  | VOUT_SELECTC    | RESERVED          |                |                 |                  |                       | V_REFC_HIGH |              |
|        | 24 (WR)  | V_REFC_LOW      |                   |                |                 |                  |                       |             |              |
|        | 25 (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
|        | 26 (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
|        | 27 (WR)  | AVP_ENC         | AVP_GAINC         |                |                 | AVP_TRIMC        |                       |             |              |
| Buck D | 28 (WR)  | RESERVED        | SOFT_START_DELAYD |                |                 | SOFT_START_TIMED |                       |             |              |
|        | 29 (WR)  | SHUTDOWN_DELAYD |                   |                | SOFT_STOP_TIME4 |                  | VOUT_TRANSITION_RATED |             |              |
|        | 2A (WR)  | VOUT_LIMIT_END  | MODED             | CURRENT_LIMITD |                 | VOUT_OVP_END     | PHASE_DELAY_SELECTD   |             | VOUT_DIS_END |
|        | 2B (WR)  | VOUT_SELECTD    | RESERVED          |                |                 |                  |                       | V_REFD_HIGH |              |
|        | 2C (WR)  | V_REFD_LOW      |                   |                |                 |                  |                       |             |              |
|        | 2D (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |
|        | 2E (WR)  | RESERVED        |                   |                |                 |                  |                       |             |              |

## REGISTER MAP (continued)

### MTP CONFIGURATION TABLE

| Scope  | REG (0x) | D[7]                                                | D[6]              | D[5]              | D[4]         | D[3]         | D[2]        | D[1]                       | D[0]                        |
|--------|----------|-----------------------------------------------------|-------------------|-------------------|--------------|--------------|-------------|----------------------------|-----------------------------|
| System | 40 (WR)  | SYSEN                                               | RESERVED          | ENA               | ENB          | ENC          | END         | RESERVED                   | SFRST                       |
|        | 41 (WR)  | RESERVED                                            | I2C_SLAVE_ADDRESS |                   |              |              |             |                            |                             |
|        | 42 (WR)  | FREQ<br>(500kHz/750kHz/1000kHz/1.25MHz/1.5MHz/2MHz) |                   |                   | TS_INTERVAL  |              |             | PWRG_DELAY                 |                             |
|        | 43 (WR)  | UVLO                                                | MTP_PROGRAM       | SHUTDOWN_DELAY_EN | OFF_TIME     |              | SFRST_NUM   |                            |                             |
|        | 44 (WR)  | RESERVED                                            | RESERVED          |                   | WP_EN        | RESERVED     | RESERVED    | PWR_GOOD_CFG               |                             |
|        | 45 (WR)  | RESERVED                                            | 1.8VLDO_FAULT_MSK | 1.1VLDO_FAULT_MSK | VR_FAULT_MSK | VBULK_OV_MSK | VDRV_OV_MSK | PMIC_HIGH_TEMP_WARNING_MSK | PMIC_HIGH_TEMP_SHUTDOWN_MSK |
|        | 50 (WR)  | MTP_CONFIGURE_CODE                                  |                   |                   |              |              |             |                            |                             |
|        | 51 (WR)  | MTP_REVISION_NUMBER                                 |                   |                   |              |              |             |                            |                             |



## MTP TABLE DESCRIPTION

### DUAL\_PHASE\_EN1 and DUAL\_PHASE\_EN3 (from Registers 10h and 20h)

The DUAL\_PHASE\_ENx bits set whether buck A and buck B (or buck C and buck D) operate in dual-phase interleaving mode or in independent, single-phase mode.

| Bits | Access | Bit Name                         | Default                                  | Reset Condition                                | Description                                                                                                                                                                                                                                                                   |
|------|--------|----------------------------------|------------------------------------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | WR     | DUAL_PHASE_ENA<br>DUAL_PHASE_ENC | DUAL_PHASE_ENA = 1<br>DUAL_PHASE_ENC = 0 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets whether buck A and buck B (or buck C and buck D) operate in dual-phase interleaving mode or in independent, single-phase mode. The dual-phase enable bit only takes effect in MTP.<br><br>0: Independent, single-phase operation<br>1: Dual-phase interleaving operation |

### SOFT\_START\_DELAYx and SOFT\_START\_TIMEx (from Registers 10h, 18h, 20h, and 28h)

The SOFT\_START\_DELAYx and SOFT\_START\_TIMEx (where x = A, B, C, and D) bits set the soft-start delay time and soft-start time for buck A, buck B, buck C, and buck D.

| Bits | Access | Bit Name          | Default | Reset Condition                                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|--------|-------------------|---------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:4  | WR     | SOFT_START_DELAYx | 00      | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the time delay between when the input voltage (V <sub>INx</sub> ) exceeds UVLO threshold, the LDOs are ready, and SYSEN = high to when the related buck's output voltage starts to ramp up. There are 8 different values. For more details, see Figure 6 on page 21 and Figure 7 on page 22.<br><br>000: Time slot 0<br>001: Time slot 1<br>010: Time slot 2<br>011: Time slot 3<br>100: Time slot 4<br>101: Time slot 5<br>110: Time slot 6<br>111: Time slot 7                                                                                                                                 |
| 3:0  | WR     | SOFT_START_TIMEx  | 0111    | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the soft-start slew rate for each buck. The values below are the potential internal reference voltage (V <sub>REF</sub> ) slew rates. If the relevant VOUT_SELECT bit is set, the output voltage (V <sub>OUTx</sub> ) (where x = A, B, C, and D) slew rate is 2 times the value listed below.<br><br>0000: 8mV/μs<br>0001: 4mV/μs<br>0010: 2.7mV/μs<br>0011: 2mV/μs<br>0100: 1.6mV/μs<br>0101: 1.3mV/μs<br>0110: 1.14mV/μs<br>0111: 1mV/μs<br>1000: 0.89mV/μs<br>1001: 0.67mV/μs<br>1010: 0.5mV/μs<br>1011: 0.4mV/μs<br>1100: 0.33mV/μs<br>1101: 0.25mV/μs<br>1110: 0.2mV/μs<br>1111: 0.167mV/μs |

### SHUTDOWN\_DELAY<sub>x</sub>, SOFT\_STOP\_TIME<sub>x</sub>, and VOUT\_TRANSITION\_RATE<sub>x</sub> (from Registers 11h, 19h, 21h, and 29h)

The SHUTDOWN\_DELAY<sub>x</sub>, SOFT\_STOP\_TIME<sub>x</sub>, and VOUT\_TRANSITION\_RATE<sub>x</sub> (where x = A, B, C, or D) bits set the shutdown time, soft-stop time, and V<sub>OUTx</sub> transition rate for buck A, buck B, buck C, and buck D.

| Bits | Access | Bit Name                          | Default | Reset Condition                                | Description                                                                                                                                                                                                                                                                                                                                                                       |
|------|--------|-----------------------------------|---------|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5  | WR     | SHUTDOWN_DELAY <sub>x</sub>       | 00      | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the delay time to SYSEN = 0 or SFRST = 0 and the buck V <sub>OUTx</sub> starting to ramp down. The 3 bits can set 8 different values:<br><br>000: Time slot 0<br>001: Time slot 1<br>010: Time slot 2<br>011: Time slot 3<br>100: Time slot 4<br>101: Time slot 5<br>110: Time slot 6<br>111: Time slot 7                                                                    |
| 4:3  | WR     | SOFT_STOP_TIME <sub>x</sub>       | 10      | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the soft-shutdown slew rate for each buck. The slew rates below are the internal V <sub>REF</sub> slew rates. If the relevant VOUT_SELECT bit is set, the soft-shutdown slew rate is 2 times the value listed below.<br><br>00: 4mV/μs<br>01: 2mV/μs<br>10: 1mV/μs<br>11: 0.5mV/μs                                                                                           |
| 2:0  | WR     | VOUT_TRANSITION_RATE <sub>x</sub> | 011     | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the V <sub>OUTx</sub> transition slew rate for each buck. The value below is the internal V <sub>REF</sub> slew rate. If the relevant VOUT_SELECT bit is set, the V <sub>OUT</sub> slew rate is 2 times the value listed below.<br><br>000: 1.6mV/μs<br>001: 1.3mV/μs<br>010: 1.14mV/μs<br>011: 1mV/μs<br>100: 0.89mV/μs<br>101: 0.67mV/μs<br>110: 0.5mV/μs<br>111: 0.4mV/μs |

### VOUT\_LIMIT\_EN<sub>x</sub>, MODE<sub>x</sub>, CURRENT\_LIMIT<sub>x</sub>, VOUT\_OVP\_EN<sub>x</sub>, PHASE\_DELAY\_SELECT<sub>x</sub>, and VOUT\_DIS\_EN<sub>x</sub> (from Registers 12h, 1Ah, 22h, 2Ah)

The VOUT\_LIMIT\_EN<sub>x</sub>, MODE<sub>x</sub>, CURRENT\_LIMIT<sub>x</sub>, VOUT\_OVP\_EN<sub>x</sub>, PHASE\_DELAY\_SELECT<sub>x</sub>, and VOUT\_DIS\_EN<sub>x</sub> (where x = A, B, C, or D) bits set the pulse-width modulation (PWM) mode, maximum V<sub>OUTx</sub>, current limit, phase delay, and enable other protection functions, such as over-voltage protection (OVP) and passive output discharge.

| Bits | Access | Bit Name                   | Default | Reset Condition                                | Description                                                                                                                                                                                                                                                                                                                                 |
|------|--------|----------------------------|---------|------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | WR     | VOUT_LIMIT_EN <sub>x</sub> | 0       | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Limits the maximum V <sub>OUTx</sub> of each buck's rail.<br><br>0: The maximum V <sub>OUTx</sub> has no limit; the value depends on the I <sup>2</sup> C V <sub>OUTx</sub> setting maximum duty cycle or absolute voltage limit<br>1: The maximum V <sub>OUTx</sub> is limited to V <sub>REF</sub> x 1 if the relevant VOUT_SELECT bit = 1 |

|     |    |                                 |                                                                                                                      |                                   |                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----|---------------------------------|----------------------------------------------------------------------------------------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | WR | MODE <sub>x</sub>               | 0                                                                                                                    | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Select the mode between automatic pulse-frequency modulation (PFM)/PWM mode and forced PWM mode.<br><br>0: Automatic PFM/PWM mode<br>1: Forced PWM mode                                                                                                                                                                                                           |
| 5:4 | WR | CURRENT_LIMIT <sub>x</sub>      | 11                                                                                                                   | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the current limit of each buck, with 15% accuracy.<br><br>00: 4A valley current limit for 3A output current (I <sub>OUT</sub> ) applications<br>01: 5A valley current limit for 4A I <sub>OUT</sub> applications<br>10: 6A valley current limit for 5A I <sub>OUT</sub> applications<br>11: 7A valley current limit for 6A I <sub>OUT</sub> applications     |
| 3   | WR | VOUT_OVP_EN <sub>x</sub>        | 1                                                                                                                    | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Enables each buck's output OVP.<br><br>0: Disabled<br>1: Enabled                                                                                                                                                                                                                                                                                                  |
| 2:1 | WR | PHASE_DELAY_SELECT <sub>x</sub> | PHASE_DELAY_SELECTA = 00 (fixed)<br>PHASE_DELAY_SELECTB = 10<br>PHASE_DELAY_SELECTC = 01<br>PHASE_DELAY_SELECTD = 11 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the phase delay for each buck. Buck A is fixed to 00.<br><br>00: 0° delay<br>01: 90° delay<br>10: 180° delay<br>11: 270° delay                                                                                                                                                                                                                               |
| 0   | WR | VOUT_DIS_EN <sub>x</sub>        | 1                                                                                                                    | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Enables the passive discharge function. Soft shutdown finishes until the buck V <sub>OUTx</sub> discharges to 0.3V. The passive discharge resistor is then connected to the buck V <sub>OUTx</sub> to further discharge the buck V <sub>OUTx</sub> . This bit also enables buck A to buck D's output passive discharge function.<br><br>0: Disabled<br>1: Enabled |

### VOUT\_SELECT<sub>x</sub> and V\_REF<sub>x</sub>\_HIGH (from Registers 13h, 1Bh, 23h, and 2Bh)

The VOUT\_SELECT<sub>x</sub> and V\_REF<sub>x</sub>\_HIGH<sub>x</sub> (where x = A, B, C, or D) bits set the buck's V<sub>OUTx</sub>, the internal feedback divider ratio, and the high bit to set the internal V<sub>REF</sub>.

| Bits | Access | Bit Name                 | Default                                                                      | Reset Condition                   | Description                                                                                                                                                                                                                                                                                                                  |
|------|--------|--------------------------|------------------------------------------------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | WR     | VOUT_SELECT <sub>x</sub> | VOUT_SELECTA = 0<br>VOUT_SELECTB = 0<br>VOUT_SELECTC = 0<br>VOUT_SELECTD = 1 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the internal feedback divider ratio.<br><br>0: V <sub>FB</sub> is directly fed to the error amplifier; V <sub>FB</sub> is equal to V <sub>REF</sub><br>1: V <sub>FB</sub> is divided by 2, then compared to V <sub>REF</sub> ; V <sub>FB</sub> is equal to 2 times of V <sub>REF</sub> , and is between 0.6V and 4.096V |
| 6:2  | RO     | RESERVED                 | 5'b000000                                                                    | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Reserved.                                                                                                                                                                                                                                                                                                                    |

|     |    |             |                                                      |                                                |                                                                                                                                                                                                    |
|-----|----|-------------|------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | WR | V_REFx_HIGH | VREFA = 10<br>VREFB = 10<br>VREFC = 10<br>VREFD = 01 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | These high bits set the internal V <sub>REF</sub> . The MP5475 does not execute V <sub>REF</sub> until the V_REFx_LOW bits are configured. Configure V_REFx_HIGH first, then configure V_REFx_LOW. |
|-----|----|-------------|------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### V\_REFx\_LOW (from Registers 14h, 1Ch, 24h, and 2Ch)

The V\_REFx\_LOW bits set the internal V<sub>REF</sub>.

| Bits | Access | Bit Name   | Default                                                                      | Reset Condition                                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|--------|------------|------------------------------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | WR     | V_REFx_LOW | VREFA = 00100110<br>VREFB = 00100110<br>VREFC = 00100110<br>VREFD = 11000010 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | <p>These low bits set the internal V<sub>REF</sub> between 300mV and 2.048V, with 2mV per step.</p> <p>{V_REFx_HIGH, V_REFx_LOW} = 00_1001_0110: 300mV<br/>           {V_REFx_HIGH, V_REFx_LOW} = 00_1001_0111: 302mV<br/>           ...<br/>           {V_REFx_HIGH, V_REFx_LOW} = 11_1111_1111: 2.048V<br/>           Others: 0mV</p> <p>Note that the MP5475 does not execute V<sub>REF</sub> until the V_REFx_LOW bits are configured. The user must configure V_REFx_HIGH first, then configure V_REFx_LOW.</p> |

### SYSTEM (40h)

The SYSTEM command enables system settings, including the overall system, each buck regulator, and software restart.

| Bits | Access | Bit Name | Default                                  | Reset Condition                                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|--------|----------|------------------------------------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | WR     | SYSEN    | 1'b0                                     | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | <p>Enables the system. When the MP5475 detects a power-on event, it sets this bit to 1. Then the power-on sequence starts. The DC/DC converters turn on sequentially according to the corresponding enable bit (e.g. ENA = 1 for buck A) and power-on delay (SOFT_START_DELAY1) setting.</p> <p>Set this bit from 1 to 0 to trigger the power-off sequence. Other I<sup>2</sup>C registers are not reset when the I<sup>2</sup>C-set SYSEN transitions from 1 to 0.</p> |
| 6    | WR     | RESERVED | 1'b1                                     | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 5:2  | WR     | ENx      | ENA = 1<br>ENB = 1<br>ENC = 1<br>END = 1 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | <p>Enables each buck regulator.</p> <p>1: Enabled<br/>0: Disabled</p>                                                                                                                                                                                                                                                                                                                                                                                                   |
| 0    | WR     | SFRST    | 1'b1                                     | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | <p>Enables software restart.</p> <p>0: Software restart is disabled<br/>1: Software restart is enabled. The MP5475 initiates a repower-on event when PG low is detected during the power-on state</p>                                                                                                                                                                                                                                                                   |

**AVP\_ENx, AVP\_GAINx, and AVP\_TRIMx (from Registers 17h and 27h)**

The AVP\_EN, AVP\_GAIN, and AVP\_TRIM bits configure active voltage positioning (AVP) for buck A and buck B (or buck C and buck D).

| Bits | Access | Bit Name  | Default                                  | Reset Condition                   | Description                                                                                                                                                                                                               |
|------|--------|-----------|------------------------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | WR     | AVP_ENx   | AVP_ENA = 0<br>AVP_ENC = 0               | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Enables buck A and buck C's AVP function.<br>0: The AVP function is disabled<br>1: The AVP function is enabled                                                                                                            |
| 6:5  | WR     | AVP_GAINx | AVP_GAINA = 01<br>AVP_GAINC = 01         | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the AVP gain.<br>00: 2.5mV/A<br>01: 2mV/A<br>10: 1mV/A<br>11: 0.5V/A                                                                                                                                                 |
| 4:0  | WR     | AVP_TRIMx | AVP_TRIMA = 0_0000<br>AVP_TRIMC = 0_0000 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the DC offset voltage to the $V_{OUTx}$ command value when AVP is enabled between -28mV and +28mV, with 2mV per step.<br>x_0000 : 0mV<br>0_0001 : 2mV<br>...<br>0_1111: 28mV<br>1_0001: -2mV<br>...<br>1_1111: -28mV |

**I2C\_SLAVE\_ADDRESS (from Register 41h)**

The I2C\_SLAVE\_ADDRESS bits configures the slave address.

| Bits | Access | Bit Name          | Default     | Reset Condition                   | Description                                                                                                                                                             |
|------|--------|-------------------|-------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0  | WR     | I2C_SLAVE_ADDRESS | 6'b1100 000 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the MP5475's I <sup>2</sup> C slave address.<br>Note that the I <sup>2</sup> C slave address bits only take effect in the multiple-time programmable (MTP) memory. |

**FREQ, TS\_INTERVAL, and PWRG\_DELAY (from Register 42h)**

The FREQ, TS\_INTERVAL, and PWRG\_DELAY bits configure the system setting, including frequency, TS\_INTERVAL, and PG delay time.

| Bits | Access | Bit Name | Default         | Reset Condition                   | Description                                                                                                                                                                                                        |
|------|--------|----------|-----------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5  | WR     | FREQ     | 3'b010: 1000kHz | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the frequency of the buck regulator. The switching frequency ( $f_{sw}$ ) of buck A to buck D remains constant.<br>000: 500kHz<br>001: 750kHz<br>010: 1000kHz<br>011: 1250kHz<br>100: 1500kHz<br>101: 2000kHz |

|     |    |             |        |                                   |                                                                                                                                                                                 |
|-----|----|-------------|--------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:2 | WR | TS_INTERVAL | 3'b011 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Determines the delay time between each time slot during the start-up delay and shutdown delay.<br><br>000: 10ms<br>001: 5ms<br>010: 2ms<br>011: 1ms<br>100: 500μs<br>101: 200μs |
| 1:0 | WR | PWRG_DELAY  | 2'b01  | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the PG delay timer after the MP5475's start-up delay finishes.<br><br>00: 0.5ms<br>01: 1ms<br>10: 10ms<br>11: 25ms                                                         |

### UVLO, SHUTDOWN\_DELAY\_EN, OFF\_TIME, and SFRST\_NUM (from Register 43h)

The UVLO, SHUTDOWN\_DELAY\_EN, OFF\_TIME, and SFRST\_NUM bits configure the system, including  $V_{IN}$  under-voltage lockout (UVLO), shutdown delay enable, off time during the repower-on sequence for software restart, and the number of repower times for software restart.

| Bits | Access | Bit Name          | Default | Reset Condition                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|--------|-------------------|---------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | WR     | UVLO              | 1'b0    | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the $V_{IN}$ UVLO threshold.<br><br>0: 3.7V rising UVLO threshold, and 3.48V falling UVLO threshold (default)<br>1: 2.85V rising UVLO threshold, and 2.6V falling UVLO threshold<br><br>Note that the UVLO control bit only takes effect in the MTP.                                                                                                                                                                                                                                                                                                         |
| 5    | WR     | SHUTDOWN_DELAY_EN | 1'b1    | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | The MP5475 offers two types of shutdown sequences when SYSEN = 0 or during software reset. The first type of shutdown sequence is where buck A to buck D follow the shutdown sequence. The second type of shutdown sequence is where the buck A to buck D shutdown sequences occur at the same time. For more details, see the SHUTDOWN_DELAYx bit configuration (from registers 11h, 19h, 21h, and 29h).<br><br>0: Shuts down at the same time<br>1: The shutdown sequence follows the SHUTDOWN_DELAYx bit configuration (from registers 11h, 19h, 21h, and 29h) |
| 4:3  | WR     | OFF_TIME          | 2'b00   | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the off time during repower sequence for software restart.<br><br>00: 10ms<br>01: 25ms<br>10: 50ms<br>11: 100ms                                                                                                                                                                                                                                                                                                                                                                                                                                              |

|     |    |           |        |                                                                 |                                                                                                                                                                                                                                                                                                                                            |
|-----|----|-----------|--------|-----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | WR | SFRST_NUM | 3'b111 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$<br>$\parallel V_{INX} < UVLO$ | Sets the number of repower times for software restart.<br>111: Repowers when SFRST is set, and PG low is detected<br>110: Repower times set to 5<br>101: Repower times set to 4<br>100: Repower times set to 3<br>011: Repower times set to 2<br>010: Repower times set to 1<br>001: Repower times set to 0<br>000: Repower times set to 0 |
|-----|----|-----------|--------|-----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### PWR\_GOOD\_CFG (from Register 44h)

The PWR\_GOOD\_CFG bits configure the mask bit for the PWR\_GOOD signal.

| Bits | Access | Bit Name     | Default | Reset Condition                   | Description                                                                                                                                       |
|------|--------|--------------|---------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0  | WR     | PWR_GOOD_CFG | 2'b00   | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the mask bit for the PWR_GOOD signal.<br>00: PWR_GOOD automatic mode<br>01: Reserved<br>10: Forces PWR_GOOD to 0<br>11: Forces PWR_GOOD to 1 |

### XXX\_MSK (from Register 45h)

The XXX\_MSK bits (1.8VLDO\_FAULT\_MSK, 1.1VLDO\_FAULT\_MSK, VR\_FAULT\_MSK, VBULK\_OV\_MSK, VDRV\_OV\_MSK, PMIC\_HIGH\_TEMP\_WARNING\_MSK, or PMIC\_HIGH\_TEMP\_SHUTDOWN\_MSK) set the mask or unmask for the 1.8VLDO\_FAULT, 1.1VLDO\_FAULT, VR\_FAULT, VBULK\_OV, VDRV\_OV, PMIC\_HIGH\_TEMP\_WARNING, or PMIC\_HIGH\_TEMP\_SHUTDOWN signal.

| Bits | Access | Bit Name | Default   | Reset Condition                   | Description                                                                                                                                                                                                                               |
|------|--------|----------|-----------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0  | WR     | XXX_MSK  | 6'b000000 | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the interrupt mask bit for the 1.8VLDO_FAULT, 1.1VLDO_FAULT, VR_FAULT, VBULK_OV, VDRV_OV, PMIC_HIGH_TEMP_WARNING, or PMIC_HIGH_TEMP_SHUTDOWN signal.<br>0: Unmask is off for the related interrupt<br>1: Masks the related interrupt |

### MTP\_CONFIGURE\_CODE (from Register 50h)

The MTP\_CONFIGURE\_CODE bits set the MTP configure code.

| Bits | Access | Bit Name           | Default | Reset Condition                   | Description                                                                          |
|------|--------|--------------------|---------|-----------------------------------|--------------------------------------------------------------------------------------|
| 7:0  | WR     | MTP_CONFIGURE_CODE | N/A     | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the MTP configure code, which is used to identify different MTP configurations. |

### MTP\_REVISION\_NUMBER (from Register 51h)

The MTP\_REVISION\_NUMBER bits set the MTP revision number.

| Bits | Access | Bit Name            | Default | Reset Condition                   | Description                                                                  |
|------|--------|---------------------|---------|-----------------------------------|------------------------------------------------------------------------------|
| 7:0  | WR     | MTP_REVISION_NUMBER | N/A     | $V_{CC} < 2V$ ,<br>$V_{DRV} < 2V$ | Sets the MTP revision number, which is used to track multiple MTP revisions. |

## I<sup>2</sup>C REGISTER MAP

| Scope  | Reg (0x) | D[7]            | D[6]              | D[5]           | D[4]            | D[3]             | D[2]                  | D[1]                   | D[0]                    |
|--------|----------|-----------------|-------------------|----------------|-----------------|------------------|-----------------------|------------------------|-------------------------|
| System | 05 (RO)  | RESERVED        |                   |                |                 | FSM_STATE        |                       | PMR_GOOD               | PMR_GOOD_RAW            |
|        | 06 (RO)  | BUCKA_PG_FILT   | BUCKB_PG_FILT     | BUCKC_PG_FILT  | BUCKD_PG_FILT   | BUCKA_PG_RAW     | BUCKB_PG_RAW          | BUCKC_PG_RAW           | BUCKD_PG_RAW            |
|        | 07 (RC)  | BUCKA_UV        | BUCKB_UV          | BUCKC_UV       | BUCKD_UV        | BUCKA_OV         | BUCKB_OV              | BUCKC_OV               | BUCKD_OV                |
|        | 08 (RC)  | BUCKA_OC        | BUCKB_OC          | BUCKC_OC       | BUCKD_OC        | BUCKA_OC_WARNING | BUCKB_OC_WARNING      | BUCKC_OC_WARNING       | BUCKD_OC_WARNING        |
|        | 09 (WC)  | RESERVED        | 1.8VLDO_FAULT     | 1.1VLDO_FAULT  | VR_FAULT        | VBULK_OV         | VDRV_OV               | PMIC_HIGH_TEMP_WARNING | PMIC_HIGH_TEMP_SHUTDOWN |
| Buck A | 10 (WR)  | DUAL_PHASE_ENA  | SOFT_START_DELAYA |                |                 | SOFT_START_TIMEA |                       |                        |                         |
|        | 11 (WR)  | SHUTDOWN_DELAYA |                   |                | SOFT_STOP_TIMEA |                  | VOUT_TRANSITION_RATEA |                        |                         |
|        | 12 (WR)  | VOUT_LIMIT_ENA  | MODEA             | CURRENT_LIMITA |                 | VOUT_OVP_ENA     | PHASE_DELAY_SELECTA   |                        | VOUT_DIS_ENA            |
|        | 13 (WR)  | VOUT_SELECTA    | RESERVED          |                |                 |                  |                       | V_REFA_HIGH            |                         |
|        | 14 (WR)  | V_REFA_LOW      |                   |                |                 |                  |                       |                        |                         |
|        | 15 (WR)  | RESERVED        |                   |                |                 |                  |                       |                        |                         |
|        | 16 (WR)  | RESERVED        |                   |                |                 |                  |                       |                        |                         |
| Buck B | 17 (WR)  | AVP_ENA         | AVP_GAINA         |                | AVP_TRIMA       |                  |                       |                        |                         |
|        | 18 (WR)  | RESERVED        | SOFT_START_DELAYB |                |                 | SOFT_START_TIMEB |                       |                        |                         |
|        | 19 (WR)  | SHUTDOWN_DELAYB |                   |                | SOFT_STOP_TIMEB |                  | VOUT_TRANSITION_RATEB |                        |                         |
|        | 1A (WR)  | VOUT_LIMIT_ENB  | MODEB             | CURRENT_LIMITB |                 | VOUT_OVP_ENB     | PHASE_DELAY_SELECTB   |                        | VOUT_DIS_ENB            |
|        | 1B (WR)  | VOUT_SELECTB    | RESERVED          |                |                 |                  |                       | V_REFB_HIGH            |                         |
|        | 1C (WR)  | V_REFB_LOW      |                   |                |                 |                  |                       |                        |                         |
|        | 1D (WR)  | RESERVED        |                   |                |                 |                  |                       |                        |                         |
| Buck C | 1E (WR)  | RESERVED        |                   |                |                 |                  |                       |                        |                         |
|        | 20 (WR)  | DUAL_PHASE_ENC  | SOFT_START_DELAYC |                |                 | SOFT_START_TIMEC |                       |                        |                         |
|        | 21 (WR)  | SHUTDOWN_DELAYC |                   |                | SOFT_STOP_TIMEC |                  | VOUT_TRANSITION_RATEC |                        |                         |
|        | 22 (WR)  | VOUT_LIMIT_ENC  | MODEC             | CURRENT_LIMITC |                 | VOUT_OVP_ENC     | PHASE_DELAY_SELECTC   |                        | VOUT_DIS_ENC            |
|        | 23 (WR)  | VOUT_SELECTC    | RESERVED          |                |                 |                  |                       | V_REFC_HIGH            |                         |
|        | 24 (WR)  | V_REFC_LOW      |                   |                |                 |                  |                       |                        |                         |
|        | 25 (WR)  | RESERVED        |                   |                |                 |                  |                       |                        |                         |
| Buck C | 26 (WR)  | RESERVED        |                   |                |                 |                  |                       |                        |                         |
|        | 27 (WR)  | AVP_ENC         | AVP_GAINC         |                | AVP_TRIMC       |                  |                       |                        |                         |



## I<sup>2</sup>C REGISTER MAP (continued)

| Scope  | Reg (0x) | D[7]                                    | D[6]              | D[5]              | D[4]            | D[3]                       | D[2]                  | D[1]                       | D[0]                        |
|--------|----------|-----------------------------------------|-------------------|-------------------|-----------------|----------------------------|-----------------------|----------------------------|-----------------------------|
| Buck D | 28 (WR)  | RESERVED                                | SOFT_START_DELAYD |                   |                 | SOFT_START_TIMED           |                       |                            |                             |
|        | 29 (WR)  | SHUTDOWN_DELAYD                         |                   |                   | SOFT_STOP_TIMED |                            | VOUT_TRANSITION_RATED |                            |                             |
|        | 2A (WR)  | VOUT_LIMIT_END                          | MODED             | CURRENT_LIMITD    |                 | VOUT_OVP_END               | PHASE_DELAY_SELECTD   |                            | VOUT_DIS_END                |
|        | 2B (WR)  | VOUT_SELECTD                            | RESERVED          |                   |                 |                            |                       | V_REFD_HIGH                |                             |
|        | 2C (WR)  | V_REFD_LOW                              |                   |                   |                 |                            |                       |                            |                             |
|        | 2D (WR)  | RESERVED                                |                   |                   |                 |                            |                       |                            |                             |
|        | 2E (WR)  | RESERVED                                |                   |                   |                 |                            |                       |                            |                             |
| System | 40 (WR)  | SYSEN                                   | RESERVED          | ENA               | ENB             | ENC                        | END                   | RESERVED                   | SFRST                       |
|        | 41 (WR)  | RESERVED                                | SLAVE_ADDRESS     |                   |                 |                            |                       |                            |                             |
|        | 42 (WR)  | FREQ<br>(500k/750k/1000k/1.25M/1.5M/2M) |                   |                   | TS_INTERVAL     |                            |                       | PWRG_DELAY                 |                             |
|        | 43 (WR)  | UVLO                                    | MTP_PROGRAM       | SHUTDOWN_DELAY_EN | OFF_TIME        |                            | SFRST_NUM             |                            |                             |
|        | 44 (WR)  | RESERVED                                | RESERVED          |                   | WP_EN           | RESERVED                   | RESERVED              | PWR_GOOD_CFG               |                             |
|        | 45 (WR)  | RESERVED                                | 1.8VLDO_FAULT_MSK | 1.1VLDO_FAULT_MSK | VR_FAULT_MSK    | VBULK_OV_MSK               | VDRV_OV_MSK           | PMIC_HIGH_TEMP_WARNING_MSK | PMIC_HIGH_TEMP_SHUTDOWN_MSK |
|        | 50 (WR)  | MTP_CONFIGURE_CODE                      |                   |                   |                 |                            |                       |                            |                             |
|        | 51 (WR)  | MTP_REVISION_NUMBER                     |                   |                   |                 |                            |                       |                            |                             |
|        | 52 (WR)  | MTP_PROGRAM_PASSWORD                    |                   |                   |                 |                            |                       |                            |                             |
|        | 54 (WR)  | REVISION_ID_MAJOR_STEPPING              |                   |                   |                 | REVISION_ID_MINOR_STEPPING |                       |                            |                             |
|        | 55 (WR)  | VENDER_ID_BYTE0                         |                   |                   |                 |                            |                       |                            |                             |
|        | 56 (WR)  | VENDER_ID_BYTE1                         |                   |                   |                 |                            |                       |                            |                             |

### Register Bits Description

Most of the register bits share the same description as the MTP table. Only the description of different register bits are included below.

The I<sup>2</sup>C register's default value is determined by the MTP table.

All I<sup>2</sup>C registers are reset at the V<sub>CC</sub> UVLO threshold, V<sub>IN</sub> < UVLO, or the EN pin going low.

OTP does not reset via the I<sup>2</sup>C register.

The below I<sup>2</sup>C register bits can only take effect after MTP:

1. DUAL\_PHASE\_EN1 (bit[7] of register 10h)
2. DUAL\_PHASE\_EN3 (bit[7] of register 20h)
3. I<sup>2</sup>C slave address (bits[6:0] of register 41h)
4. UVLO (bit[7] of register 43h)

### FSM\_STATE, PWR\_GOOD, and PWR\_GOOD\_RAW (from Register 05h)

The FSM\_STATE, PWR\_GOOD, and PWR\_GOOD\_RAW bits control certain system configurations, including the state, PWR\_GOOD\_RAW signal, and the output for all the BUCK\_PG\_FILT states.

| Bits | Access | Bit Name     | Default | Description                                                                                                                                                                                                                |
|------|--------|--------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:2  | RO     | FSM_STATE    | 2'b00   | 00: Management state<br>01: Power-on state                                                                                                                                                                                 |
| 1    | RO     | PWR_GOOD     | 1'b0    | Sets the PWR_GOOD_RAW signal, which is filtered by the FSM_STATE signal. When PWR_GOOD_RAW is high and the MP5475 is not in management state, PWR_GOOD is high.<br><br>0: PWR_GOOD outputs low<br>1: PWR_GOOD outputs high |
| 0    | RO     | PWR_GOOD_RAW | 1'b0    | Sets the output for all the BUCK_PG_FILT signals.<br><br>0: PWR_GOOD_RAW outputs low<br>1: PWR_GOOD_RAW outputs high                                                                                                       |

### BUCKx\_PG\_FILT and BUCKx\_PG\_RAW (from Register 06h)

The BUCKx\_PG\_FILT and BUCKx\_PG\_RAW bits set each buck's PG output and the filter's PG output.

| Bits | Access | Bit Name      | Default | Description                                                                                                                                                                                                                                                                                                                       |
|------|--------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | RO     | BUCKx_PG_FILT | 4'b1111 | Sets buck x's (where x = A, B, C, or D) PG output filter when working with the EN signal.<br><br>0: The filter's PG output is low (the selected rail's output is out of $\pm 20\%$ nominal output)<br>1: The filter's PG output is high (the selected rail's output is out of $\pm 20\%$ nominal output, or the rail is disabled) |
| 3:0  | RO     | BUCKx_PG_RAW  | 4'b0000 | Sets buck x's (where x = A, B, C, or D) raw PG output.<br><br>0: The PG raw output is low (the selected rail's output is out of $\pm 20\%$ nominal output)<br>1: The PG raw output is high (the selected rail output is within $\pm 20\%$ nominal output)                                                                         |

### BUCKx\_UV and BUCKx\_OV (from Register 07h)

The BUCKx\_UV and BUCKx\_OV bits indicate each buck's over-voltage (OV) or under-voltage (UV) status.

| Bits | Access | Bit Name | Default | Description                                                                                                                                                          |
|------|--------|----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | RC     | BUCKx_UV | 4'b0000 | Indicates buck x's (where x = A, B, C, or D) output UV status.<br><br>0: No UV condition on buck x<br>1: UV condition on buck x (below 20% of nominal output window) |
| 3:0  | RC     | BUCKx_OV | 4'b0000 | Indicates buck x's (where x = A, B, C, or D) output OV status.<br><br>0: No OV condition on buck x<br>1: OV condition on buck x (above 20% of nominal output window) |

### BUCKx\_OC and BUCKx\_OC\_WARNING (from Register 08h)

The BUCKx\_OC and BUCKx\_OC\_WARNING bits indicate each buck's over-current (OC) status as well as the high current consumption warning status.

| Bits | Access | Bit Name | Default | Description                                                                                                                                      |
|------|--------|----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | RC     | BUCKx_OC | 4'b0000 | Indicates buck x's (where x = A, B, C, or D) OC status.<br><br>0: No buck x OC condition<br>1: Buck x over-current protection (OCP) has occurred |

|     |    |                  |         |                                                                                                                                                                                                                                      |
|-----|----|------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | RC | BUCKx_OC_WARNING | 4'b0000 | <p>Indicates buck x's (where x = A, B, C, or D) high current consumption warning status (the output current exceeds 85% of the threshold).</p> <p>0: No high current consumption warning<br/>1: High current consumption warning</p> |
|-----|----|------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### SYSTEM (09h)

The SYSTEM command indicates error statuses, such as 1.8V LDO and 1.1V LDO faults, voltage regulator (VR) faults, and V<sub>INx</sub> OV faults, as well as PMIC high-temperature warnings and high-temperature shutdown, where the temperature is between 125°C and 150°C.

| Bits | Access | Bit Name                | Default | Description                                                                                                                                                                                         |
|------|--------|-------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6    | WC     | 1.8VLDO_FAULT           | 1'b0    | <p>Indicates the 1.8VLDO's output PG status.</p> <p>0: The 1.8VLDO output is within ±15% of the nominal output window<br/>1: The 1.8VLDO output is not within ±15% of the nominal output window</p> |
| 5    | WC     | 1.1VLDOX_FAULT          | 1'b0    | <p>Indicates the 1.1VLDO's output PG status.</p> <p>0: The 1.1VLDO output is within ±15% of the nominal output window<br/>1: The 1.1VLDO output is not within ±15% of the nominal output window</p> |
| 4    | WC     | VR_FAULT                | 1'b0    | <p>Indicates the overall buck's PG status.</p> <p>0: All buck outputs are within ±20% of the nominal range<br/>1: One (or more) buck output(s) are outside of the ±20% nominal range</p>            |
| 3    | WC     | VBULK_OV                | 1'b0    | <p>Indicates the V<sub>INx</sub> OV status.</p> <p>0: V<sub>INx</sub> is below 14.2V<br/>1: V<sub>INx</sub> exceeds 14.5V</p>                                                                       |
| 2    | WC     | VDRV_OV                 | 1'b0    | <p>Indicates V<sub>DRV</sub>'s OV status.</p> <p>0: V<sub>DRV</sub> is below 3.5V<br/>1: V<sub>DRV</sub> exceeds 3.6V</p>                                                                           |
| 1    | WC     | PMIC_HIGH_TEMP_WARNING  | 1'b0    | <p>Indicates whether the PMIC has a high-temperature warning.</p> <p>0: No high-temperature warning<br/>1: The PMIC's silicon temperature exceeds 125°C</p>                                         |
| 0    | WC     | PMIC_HIGH_TEMP_SHUTDOWN | 1'b0    | <p>Indicates the PMIC's high-temperature shutdown status.</p> <p>0: No high temperature shutdown<br/>1: The PMIC's silicon temperature exceeds 150°C</p>                                            |

### MTP\_PROGRAM (from Register 43h)

The MTP\_PROGRAM bits control MTP configuration.

| Bits | Access | Bit Name    | Default | Reset Condition | Description                                                                                                                                                                                                                                                                                                                            |
|------|--------|-------------|---------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6    | WR     | MTP_PROGRAM | 1'b0    | Automatic       | <p>Controls MTP configuration.</p> <p>Once this bit is set, the I<sup>2</sup>C register is written to the MTP table. During MTP writing, I<sup>2</sup>C write operation is locked and not acknowledged (NACK), but read operation is not locked until MTP write operation finishes. Then the system automatically resets this bit.</p> |

### WP\_EN (from Register 44h)

The WP\_EN bit enables I<sup>2</sup>C write protection.

| Bits | Access | Bit Name | Default | Reset Condition                                | Description                                                                                                                                                     |
|------|--------|----------|---------|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4    | WR     | WP_EN    | 1'b0    | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Enables I <sup>2</sup> C write protection.<br>0: No write protection<br>1: Only allowed to write to the I <sup>2</sup> C register while in the management state |

### MTP\_PROGRAM\_PASSWORD( from Register 52h)

The MTP\_PROGRAM\_PASSWORD bits set the correct password for MTP configuration.

| Bits | Access | Bit Name             | Default     | Reset Condition                                | Description                                                                                         |
|------|--------|----------------------|-------------|------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| 7:0  | WR     | MTP_PROGRAM_PASSWORD | 8'b00000000 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the correct password for MTP configuration. These bits controls access to the MTP_PROGRAM bit. |

### REVISION\_ID\_MAJOR\_STEPPING and REVISION\_ID\_MINOR\_STEPPING ( from Register 54h)

The REVISION\_ID\_MAJOR\_STEPPING and REVISION\_ID\_MINOR\_STEPPING bits set the major and minor revision.

| Bits | Access | Bit Name                   | Default | Reset Condition                                | Description                                                                                                                              |
|------|--------|----------------------------|---------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | WR     | REVISION_ID_MAJOR_STEPPING | 4'b0000 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the major revision. All other encodings are reserved.<br>0000: Reserved<br>0001: Revision 1<br>0010: Revision 2<br>0011: Revision 3 |
| 3:0  | WR     | REVISION_ID_MINOR_STEPPING | 4'b0000 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the minor revision. All other encodings are reserved.<br>0000: Reserved<br>0001: Revision 1<br>0010: Revision 2<br>0011: Revision 3 |

### VENDOR\_ID\_BYTE0 (from Register 55h)

The VENDOR\_ID\_BYTE0 bits set the lower byte of the vendor's ID.

| Bits | Access | Bit Name        | Default     | Reset Condition                                | Description                             |
|------|--------|-----------------|-------------|------------------------------------------------|-----------------------------------------|
| 7:0  | WR     | VENDOR_ID_BYTE0 | 8'b00000000 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the lower byte of the vendor's ID. |

### VENDOR\_ID\_BYTE1 (from Register 56h)

The VENDOR\_ID\_BYTE1 bits set the higher byte of the vendor's ID.

| Bits | Access | Bit Name        | Default     | Reset Condition                                | Description                              |
|------|--------|-----------------|-------------|------------------------------------------------|------------------------------------------|
| 7:0  | WR     | VENDOR_ID_BYTE1 | 8'b00000000 | V <sub>CC</sub> < 2V,<br>V <sub>DRV</sub> < 2V | Sets the higher byte of the vendor's ID. |

## APPLICATION INFORMATION

### Selecting the Inductor

**Optimized Performance with MPS Inductor MPL4020 Series**

Choose a 0.22μH to 2μH inductor with a minimum DC current rating exceeding 25% of the maximum load current for most applications. To optimize efficiency, use an inductor with a DC resistance below 15mΩ. For most designs, the inductance (L<sub>1</sub>) can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI<sub>L</sub> is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I<sub>L\_MAX</sub>) can be estimated with Equation (2):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Use a larger-value inductor to achieve improved efficiency under light-load conditions (below 100mA).

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 shows the MPS power inductor recommendations, where the part number can be selected based on the design requirements.

**Table 2: Selecting the Power Inductor**

| Part Number    | Inductance | Manufacturer |
|----------------|------------|--------------|
| MPL-AL4020-R47 | 0.47μH     | MPS          |
| MPL-AL4020-R68 | 0.68μH     | MPS          |
| MPL-AL4020-1R0 | 1μH        | MPS          |
| MPL-AL4020-1R5 | 1.5μH      | MPS          |

For more information, visit the Inductors page on the MPS website.

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC V<sub>IN</sub>. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for the best results due to their low ESR and small

temperature coefficients. For most applications, a 22μF capacitor is sufficient.

Since C<sub>1</sub> absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (C<sub>IN</sub>) (I<sub>C1</sub>) can be calculated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at V<sub>IN</sub> = 2 × V<sub>OUT</sub>, which can be estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose C<sub>IN</sub> with an RMS current rating that is greater than half of the maximum load current.

C<sub>IN</sub> can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure there is enough capacitance to provide sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple (ΔV<sub>IN</sub>) caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

### Selecting the Output Capacitor for the Step-Down Regulator

The output capacitor (C<sub>OUT</sub>) for the step-down converter maintains the DC V<sub>OUT</sub>. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple (ΔV<sub>OUT</sub>) can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_2}\right) \quad (6)$$

Where L<sub>1</sub> is the inductance, and R<sub>ESR</sub> is the equivalent series resistance (ESR) of C<sub>OUT</sub>.

For ceramic capacitors, the capacitance dominates the impedance at f<sub>SW</sub> and causes the majority of ΔV<sub>OUT</sub>.

For simplification,  $\Delta V_{OUT}$  can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L1 \times C2} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at  $f_{SW}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \times R_{ESR} \quad (8)$$

The  $C_{OUT}$  characteristics also affect the stability of the regulation system.

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 21 and follow the guidelines below:

1. Connect the input ground to the ground with the shortest and widest trace possible.
2. Connect  $C_{IN}$  to the VINx pin (where x = A, B, C, or D) with the shortest and widest trace possible.
3. Ensure all FB connections are short and direct.
4. Place the FB resistors and compensation components as close to the chip as possible.
5. Route the SWx pin (where x = A, B, C, or D) away from sensitive analog areas, such as FB.
6. Place the VCC decoupling capacitor close to the VCC and AGND pins.
7. Keep an open space around the PMIC and ensure that the airflow is at least 200FPM to 400FPM on the PMIC surface and the other side of the DIMM board. Airflow is required for PMIC heat dissipation.

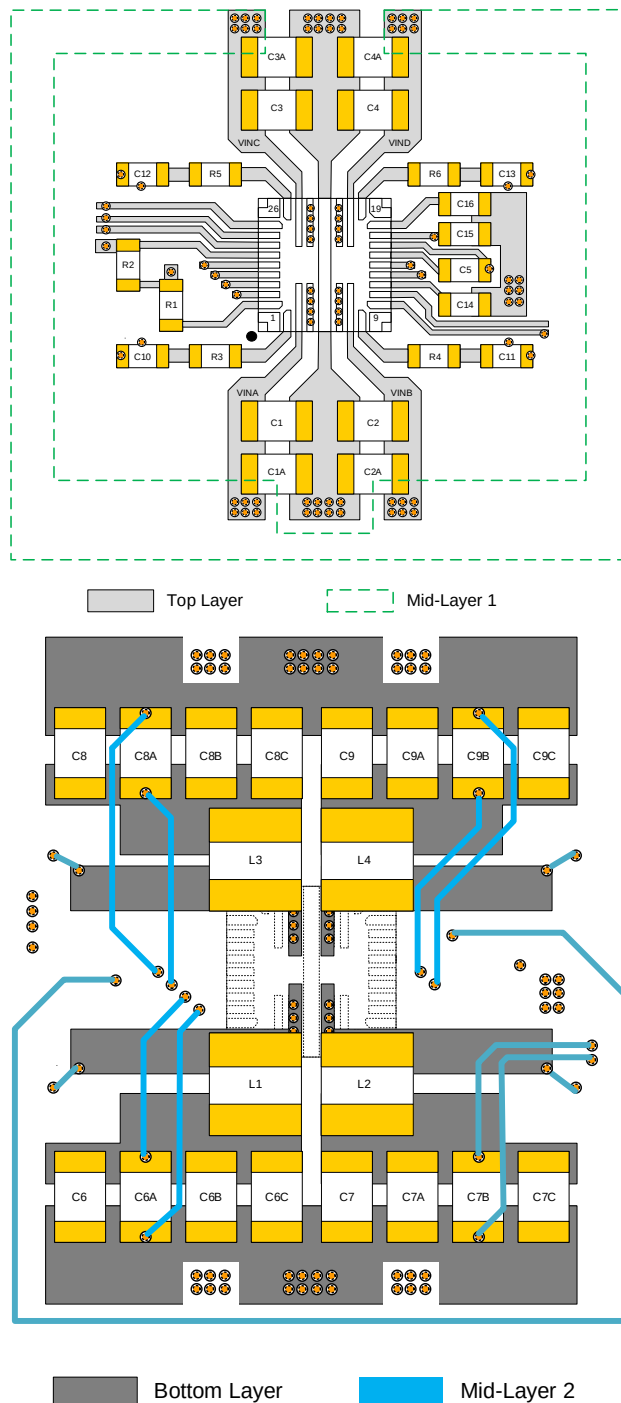


Figure 21: Recommended PCB Layout

## TYPICAL APPLICATION CIRCUITS

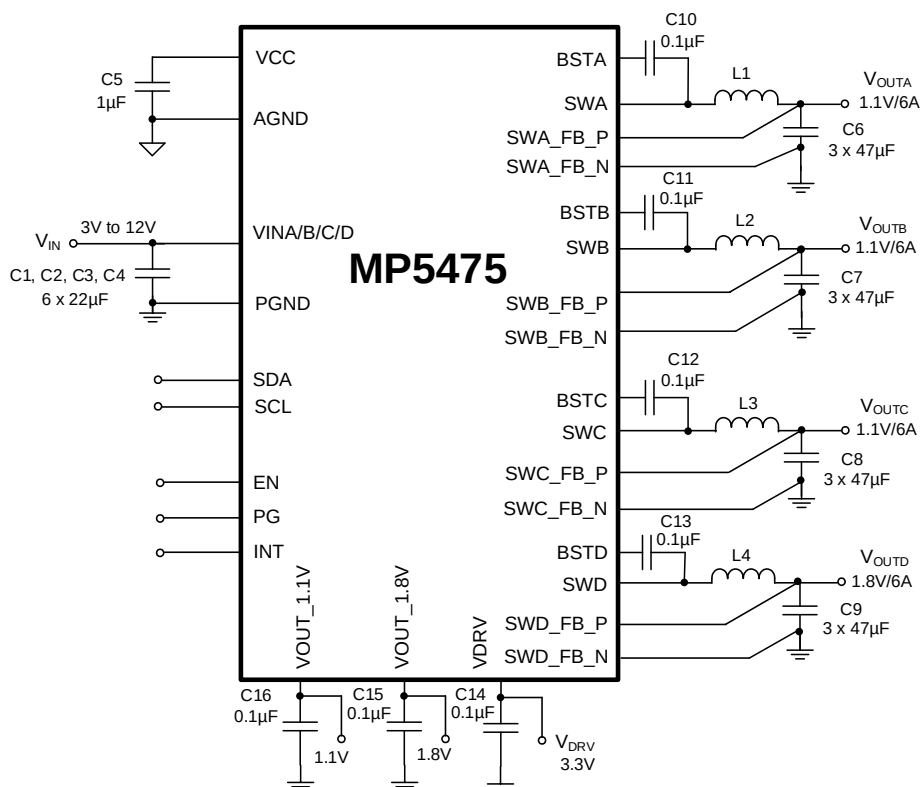


Figure 22: Typical Application Circuit (Buck A and Buck B in Single-Phase Regulator Mode)

# TYPICAL APPLICATION CIRCUITS *(continued)*

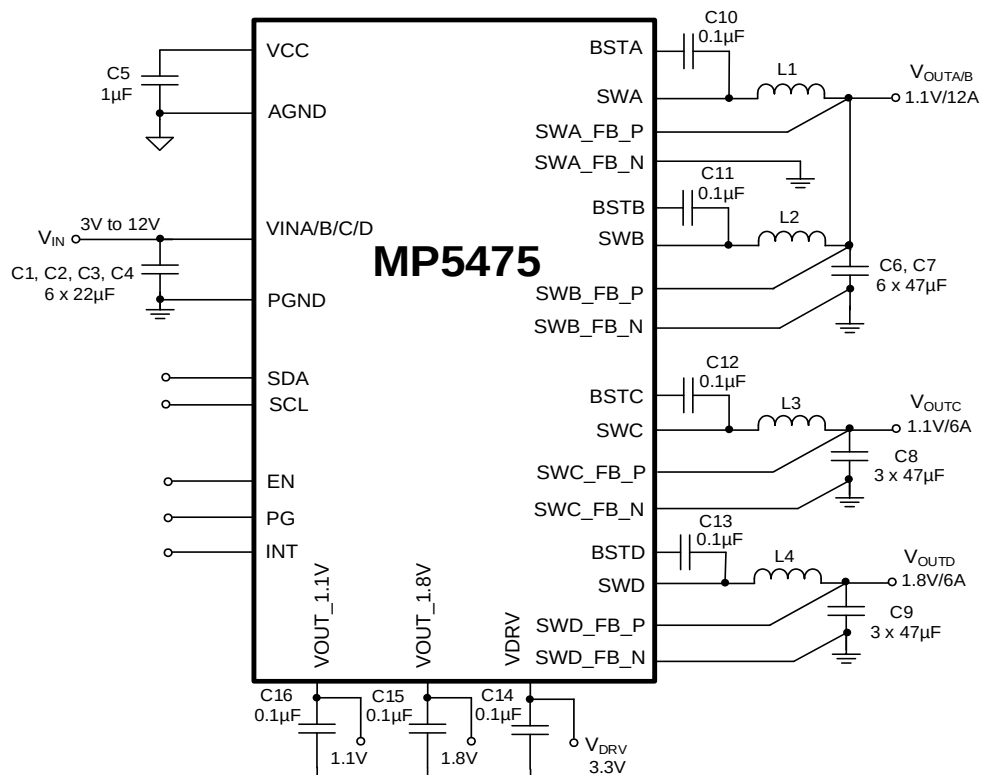
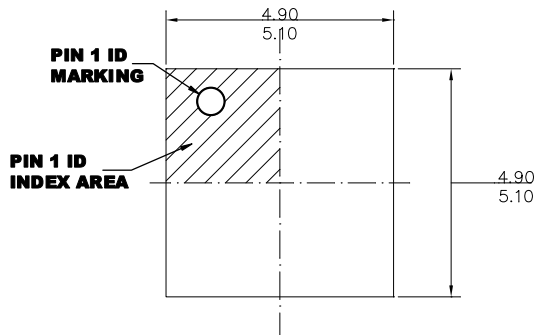


Figure 23: Typical Application (Buck A and Buck B in Dual-Phase Regulator Mode)

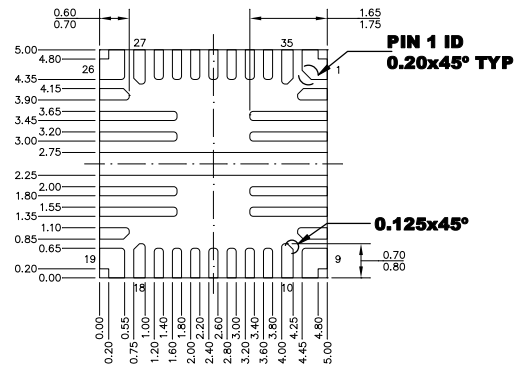


# PACKAGE INFORMATION

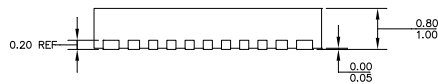
## QFN-35 (5mmx5mm)



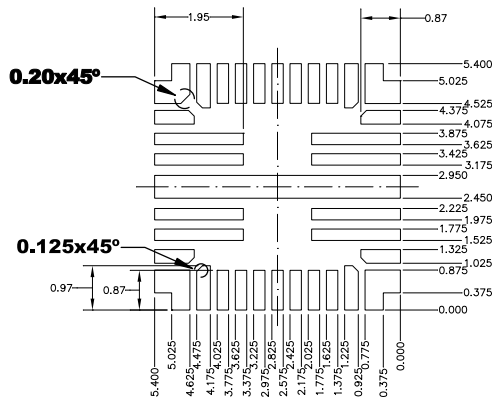
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

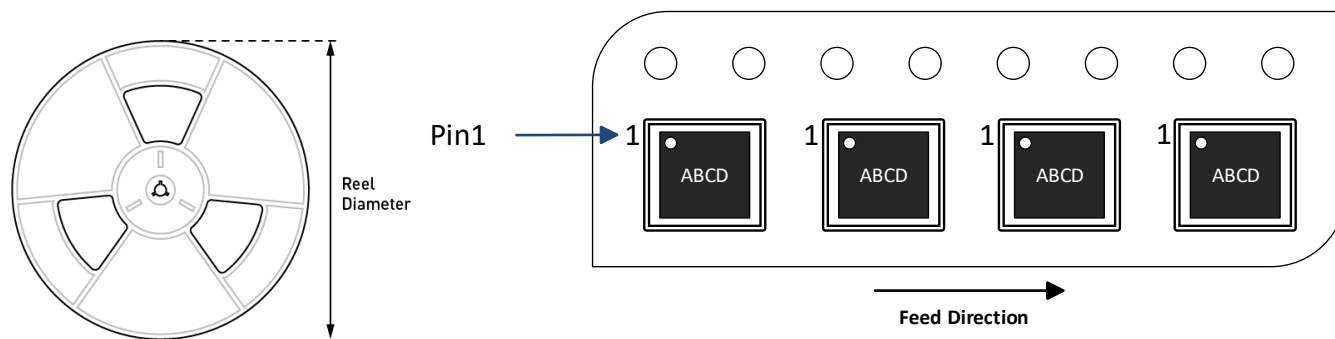


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-333.
- 4) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number     | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-----------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MP5475GU-xxxx-Z | QFN-35 (5mmx5mm)    | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |



## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 3/7/2024      | Initial Release | -             |

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