Functional features

- ADC with dual fully differential input channels
- 16 bit Σ-Δ analog-to-digital conversion
- Integral nonlinearity is less than 0.003%
- Programmable gain: 1 ~ 128
- Serial three wire communication
- Ability to buffer analog input
- 3V or 5V working voltage, range ± 5%
- At 3V, the maximum power consumption is 1mW
- In power down mode, the maximum current is 8 μA
- 16 pin DIP, SOIC, TSSOP, SOP package

Structure Diagrams

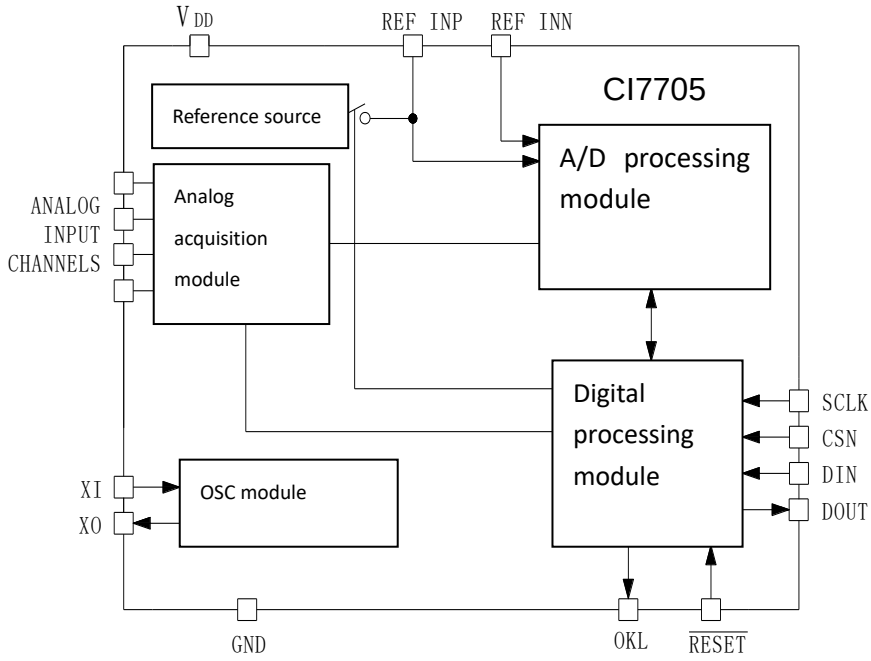


Figure 1

Pin definition

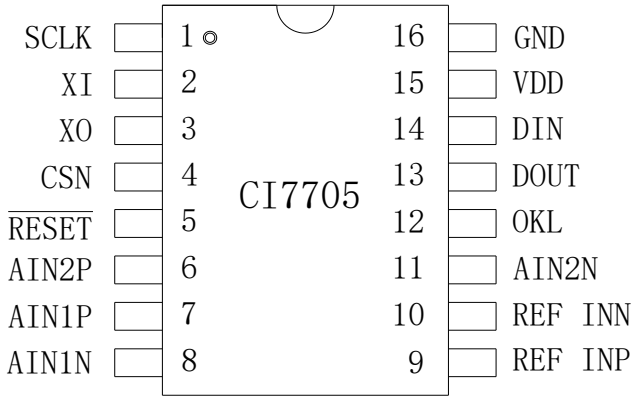


Figure 2

Pin function definition

Pin Name	Serial number of pin	I/O	Function
SCLK	1	I	Serial clock input
XI	2	I	Clock input, crystal oscillator or external clock
XO	3	O	Clock output
CSN	4	I	Chip selection, input low level valid
$\overline{RESET}$	5	I	Reset, low level valid
AIN2P	6	I	Differential analog positive input of channel 2
AIN1P	7	I	Differential analog positive input of channel 1
AIN1N	8	I	Differential analog negative input of channel 1
REF INP	9	I	Positive input of reference voltage
REF INN	10	I	Negative input of reference voltage
AIN2N	11	I	Differential analog negative input of channel 2
OKL	12	O	AD conversion completion logic output flag bit
DOUT	13	O	Serial data output
DIN	14	I	Serial data input
VDD	15	-	Power supply
GND	16	-	Systematically

Communication interface

CI7705 uses serial communi cation to complete the read / write operation of on-chip register. The serial interface includes five signal interfaces: SCLK, DIN, DOUT, OKL and CSN. The data transmission sequence adopts the high order first.

DIN: data input port, which writes data on the rising edge of the clock.

DOUT: data output port, which outputs data on the falling edge of the clock.

SCLK: read / write serial clock input.

OKL: indication signal indicating whether the data of ADC result register is updated. A low level indicates that the ADC data has been converted. At this time, the ADC data can be read from the ADC result register. High level indicates that the ADC is converting or updating, and the data cannot be read at this time.

CSN: Chip selection signal. Only when the CSN is lowered first can the register be read and written. After reading and writing, the CSN should be raised.

Sequence waveform

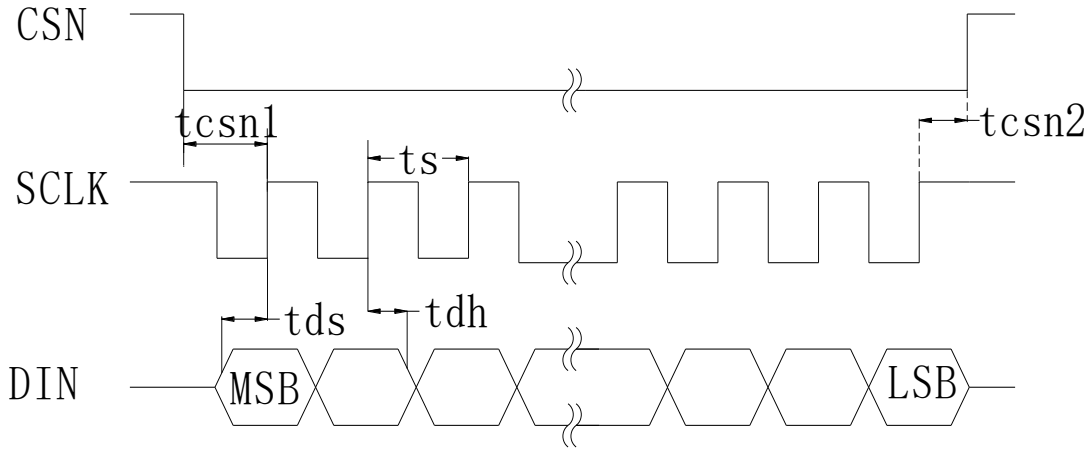


Figure 3 Write sequence

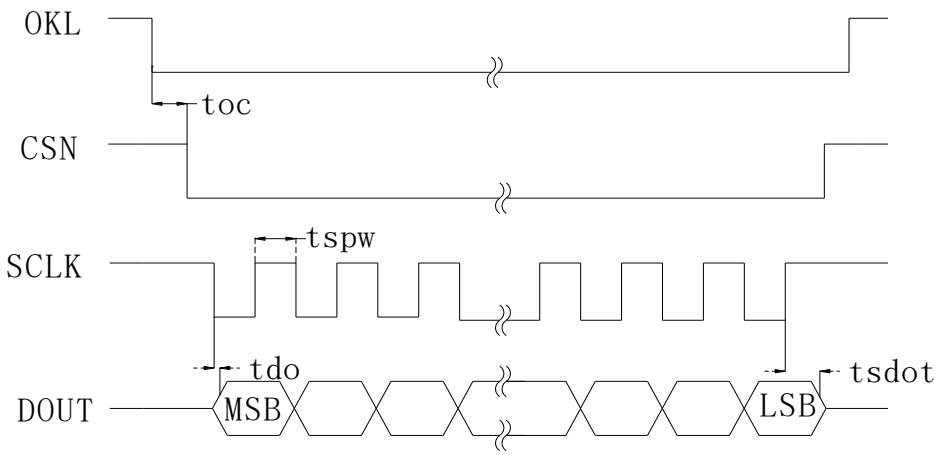


Fig. 4 Reading sequence

Sequence characteristic

Parameter Name	Parameter symbol	Test Conditions	Minimum	Type value	Maximum	Unit
Master clock frequency	f_{CLKIN}	-	400		2500	kHz
Master clock low level time	Tlow	t_{CLKIN}=1/ f_{CLKIN}	0.4*t_{CLKIN}			ns
Master clock high level time	Thigh		0.4*t_{CLKIN}			ns
OKL high pulse	t_O			500*t_{CLKIN}		ns
$\overline{RESET}$ pulse width	t_R		100			ns
Read and write sequence						
CSN ↓→ first rising edge of SLCK	Tcsn1		120			ns
Slck ↓→ DIN effective acquisition interval	tdo	V_{DD} =5V	0	-	80	ns
		V_{DD} =3V	0	-	100	ns
SCLK ↑→ CSN ↑ time	Tcsn2		0			ns
SCLK ↑ back bus withdrawal time	tsout	V_{DD}=5V	10		60	ns
		V_{DD}=3V			100	ns
Din valid → SCLK ↑ acquisition time	tds		30			ns
Din valid → SCLK ↑ holding time	tdh		20			ns
OKL ↓→ CSN ↓ time	toc		0			ns
Clock pulse width high (low) level	tspw		100			ns

Register description

CI7705 has 8 internal registers. The communication register is mainly introduced, because any operation of other registers must first operate the communication register before operating its registers. If more than 32 pulses are sent after the write operation of DIN high level, the chip will reset.

Table 1 8-bit description of communication register power on / reset status: 00 hex

MSB	**B7**	**0/OKL**	The chip reserves the use bit. The default value is "0". Writing "0" is writing. Do not write "1"		
	B6	**RSAD0**	Register address bit.	000: communication register 001: configuration register 010: frequency register 011: ADC result register 100: test register 101: NC register 110: zero offset register 111: gain coefficient register	
	B5	**RSAD1**			
	B4	**RSAD2**			
	B3	**R/WL**	Read/write selection bit, "0" indicates that the operation is write, "1" indicates that the operation is read.		
	B2	**PD**	Write "1", power down mode. Write "0", normal working mode.		
	B1	**CHH**	**0**	**0**	**1**

LSB	B0	CHL	0	1	0
	Channel selection		AIN1	AIN2	AIN1N internal short circuit
	Logarithm of correction register		Register pair 0	Register pair 1	Register pair 0

Table 2 Configuration register 8-bit description power on / reset status: 01 Hex

MSB	**B7**	**MDH**	Working mode selection bit: 00: normal working mode 01: self correction 10: Correction for zero offset system 11: System correction for gain coefficient							
	B6	**MDL**								
	/	**PGA configuration**	**1**	**2**	**4**	**8**	**16**	**32**	**64**	**128**
	B5	**PGA_ two**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
	B4	**PGA_ one**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**
	B3	**PGA_ 0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
	B2	U/BL	Unipolar "1" + FSR output 0xFFFFH,ZER0=0x0000H,-FSR=Ox0000H, Bipolar "0" + FSR output 0xFFFFH,ZER0=0x8000H,-FSR=Ox0000H,							
	B1	**BUFEN**	Input buffer enable, "0" prohibited, internal buffer short circuit, "1" enabled							
LSB	**B0**	**SYNC**	When the filter is synchronized, it defaults to 0. Reset the digital modulator if it is "1". Ability to collect samples from analog inputs starting from a known point in time, arriving at system synchronization.							

Table 3 8-bit description of power on/reset status of frequency register: 05 hex

MSB	**B7**	**Z0**	To ensure correct operation, zero must be written on these bits. Otherwise, the operation of the device is not specified.							
	B6	**Z1**								
	B5	**Z2**								
	B4	**OSCDIS**	Clock inhibit bit. The default value is 0. If "1" indicates that XO is low, power consumption can be reduced.							
	B3	**OSCDIV**	Clock divider bit. OSCDIV = 1, the clock frequency at pin XI is divided by 2 before being used by the device.							
	OSC clock		1MHz				2.4576MHz			
	Output update rate		20Hz	25 Hz.	100 Hz	200 Hz	50 Hz	60Hz	250 Hz	500 Hz
	Filter - 3dB cut-off frequency		5.24Hz	6.55Hz	26.2 Hz	52.4 Hz	13.1 Hz	15.7 Hz	65.5 Hz	131 Hz
	B2	**OSC**	0	0	0	0	1	1	1	1
	B1	**DRH**	0	0	1	1	0	0	1	1

LSB	**B0**	**DRL**	0	1	0	1	0	1	0	1

ADC result register is a 16 bit read-only register, which is used to store the latest conversion results. When reading data, the high-order first out.

Power on / reset status: 0000 Hex.

The test register is an 8-bit register used to test the device. Users are advised not to change it at will. (all zeros are automatically set when power on or reset). **Power on / reset status: 00 hex**

The zero offset register is a 24 bit read / write register. The CI7705 has several groups of independent zero offset registers, and the corresponding zero offset registers are responsible for different input channels. The 24 bit data must be written before it can be transferred to the zero offset register. **Power on / reset status: 1F4000 Hex**

The gain coefficient register is a 24 bit read / write register. The CI7705 has several groups of indepen dent gain coefficient registers, and the corresponding gain coefficient registers are responsible for different input channels. 24 bit data must be written before it can be transferred to the gain coefficient register. **Power on / reset status: 5761 AB Hex**

The gain coefficient register and zero offset register are used together to form a register pair. The communication register is introduced above.

Applied circuit

The basic circuit diagram of CI7705 (Figure 5), as shown in the figure, the analog vo ltage is + 5V / 3V; The precise + 2.5v/1.225v reference voltage provides the reference voltage for the device. On the digital signal side, the device is configured to work in three wires and the CSN is grounded.

Quartz crystal provides the main clock source. The resistance of R is 1MΩ, and the capacitance of C1 and C2 is generally in the range of 30pF to 50pF.

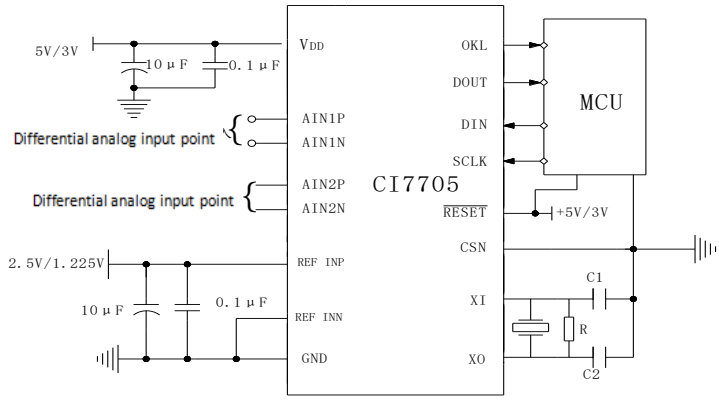


Figure 5 circuit diagram of CI7705

Methods of improving the accuracy of CI7705 in the application of electronic sca le

（1） When the master clock is 2.4576MHz, it is strongly recommended to set the clock register to 84h, as shown in the following table:

ZO	Z1	Z2	OSCDIS	OSCDIV	OSC	DRH	DRL
1	0	0	0	0	1	0	0

At this time, the data output update rate is 10Hz, that is, a new data is output every 0.1s.

（2） When the master clock is 1MHz, it is strongly recommended to set the clock register to 80H, as shown in the following table:

ZO	Z1	Z2	OSCDIS	OSCDIV	OSC	DRH	DRL
1	0	0	0	0	0	0	0

At this time, the data output update rate is 4Hz, that is, a new data is output every 0.25s.

Reset and power down mode

The reset input circuit resets all logic, digital filters and analog modulators, and sets all on-chip registers to their default state. In the way of reset, pull the pin $\overline{\text{RESET}}$ down or send the $\overline{\text{RESET}}$ = 0 command.

The PD bit in the communication register allows the user to set the device to operate in power-down mode to reduce power consumption. After coming out of power-down mode, the device enters normal mode. All registers remain as they were before power-down mode and do not need to be reconfigured.

External reference voltage

REFINP and REFINN provide CI7705 with differential reference voltage function. When working at 5V / 3V power supply voltage, the reference voltage is + 2.5v/1.225v. When the reference voltage is less than 1V, although the device can work, the output noise becomes larger, resulting in performance degradation. Therefore, REFINP>REFINN must be ensured to ensure that the device can work normally.

Error Correction

When the ambient temperature, operating voltage, selected gain, filter notch and unipolar / bipolar input range change. The device must be corrected to ensure the correctness of analog-to-digital conversion. CI7705 has a variety of correction options, which can be realized by MDH and MDL bit programming of configuration register. Correction can eliminate bias and gain errors on the device.

Self correction

When the self-calibration command is sent, the chip performs zero offset correction and gain coefficient correction at the channel specified in the communication register and at the set gain. For zero offset correction, the chip's specified input channel is internally shorted automatically (zero input). For gain coefficient correction, the chip's specified input channel is connected to the internal Vref/selected gain voltage (full scale). After correction, the zero offset register will be automatically updated
and the value of the gain coefficient register. And, during the calibration process, OKL is kept high. When OKL is pulled low, it indicates that the calibration is completed. And then it automatically returns to normal operation mode, i.e. MDH MDL=00 state.

System correction

System correction can correct the bias error and gain error inside the chip and the system, because the system must correct the input signal. System correction includes offset error correction and gain error correction.

When correcting the zero offset error, it is required to input the differential voltage of 0V, write MDH and MDL in the configuration register (1, 0) and start the zero offset. The chip calculates the zero offset error value of the system and writes it into the zero offset register. Compensation will be provided for subsequent work.

When correcting the gain coefficient error, it is required to input the voltage with positive and full amplitude, write MDH and MDL in the configuration register (1, 1), and start the gain error correction. The chip calculates the gain error value of the system and writes it into the gain coefficient register. Compensation will be provided for subsequent work.

Output noise

Table 4 and 6 show the reference value of output noise generated during analog input short circuit when V_{DD} = 5V and V_{DD} = 3V, V_{ref} =+2.5V/1.225V, the device works in buffer mode or non buffer mode, and the update frequency can be selected at - 3dB frequency. Tables 5 and 7 show the resolutions when V_{DD} = 5V and V_{DD} = 3V respectively. The number of significant digits of resolution represented by these numbers.

Table 4 Relationship between output noise and gain and update rate (5V voltage)

Data update rate	-3dB cut-off frequency	Typical value of output noise （ μV）							
		gain							
		1	2	4	8	16	32	64	128
BUFEN=0， F_{CLKIN} =2.4576MHz									
50Hz	13.1Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
60Hz	15.72Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
250Hz	65.5Hz	110	49	31	17	8	3.6	2.3	1.7
500Hz	131Hz	550	285	145	70	41	22	9.1	4.7
BUFEN=0， F_{CLKIN}=1MHz									
20Hz	5.24Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
25 Hz.	6.55Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
100 Hz	26.2Hz	110	49	31	17	8	3.6	2.3	1.7
200Hz	52.4Hz	550	285	145	70	41	22	9.1	4.7

Table 5 Relationship between resolution and gain and update rate (5V voltage)

Data update rate	-3dB cut-off frequency	Resolution (significant digits)							
		Gain							
		1	2	4	8	16	32	64	128
BUFEN=0， F_{CLKIN} =2.4576MHz									
50Hz	13.1Hz	16	16	16	16	16	16	15	14
60Hz	15.72Hz	16	16	16	16	15	14	14	13
250Hz	65.5Hz	13	13	13	13	13	13	12	12
500Hz	131Hz	10	10	10	10	10	10	10	10
BUFEN=0， F_{CLKIN} =1MHz									
20Hz	5.24Hz	16	16	16	16	16	16	15	14
25 Hz	6.55Hz	16	16	16	16	15	14	14	13
100 Hz	26.2Hz	13	13	13	13	13	13	12	12
200Hz	52.4Hz	10	10	10	10	10	10	10	10

Table 6 Relationship between output noise and gain and update rate (3V voltage)

Data update	-3dB cut-off	Typical value of output noise （ μV）
		Gain

rate	frequency	1	2	4	8	16	32	64	128
BUFEN=0， F_{CLKIN} =2.4576MHz									
50Hz	13.1Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
60Hz	15.72Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
250Hz	65.5Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
500Hz	131Hz	270	135	65	41	22	9.7	5.1	3.3
BUFEN=0， F_{CLKIN} =1MHz									
20Hz	5.24Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
25 Hz.	6.55Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
100 Hz	26.2Hz	50	25	14	9.9	5.1	2.6	23	2.0
200Hz	52.4Hz	270	135	65	41	22	9.7	5.1	3.3

Table 7 Relationship between resolution and gain and update rate (3V voltage)

Data update rate	-3dB cut-off frequency	Resolution (significant digits)							
		Gain							
		1	2	4	8	16	32	64	128
BUFEN=0， F_{CLKIN} =2.4576MHz									
50Hz	13.1Hz	16	16	15	15	14	13	13	12
60Hz	15.72Hz	16	16	15	14	14	13	13	12
250Hz	65.5Hz	13	13	13	13	12	12	11	11
500Hz	131Hz	10	10	10	10	10	10	10	10
BUFEN=0， F_{CLKIN} =1MHz									
20Hz	5.24Hz	16	16	15	15	14	13	13	12
25 Hz.	6.55Hz	16	16	15	14	14	13	13	12
100 Hz	26.2Hz	13	13	13	13	12	12	11	11
200Hz	52.4Hz	10	10	10	10	10	10	10	10

Limit parameter (TA = + 25 ℃, unless otherwise specified)

Parameter Name	Parameter symbol	Limit value	Unit
Logic Supply Voltage	VDD	-0.3V ～7	v
Analog input voltage	Vin	-0.3 ～V_{DD} +0.3	v
Digital input voltage			
Digital output voltage	Vout	-0.3 ～V_{DD} +0.3	v
Operating temperature range	Topr	-40～85	℃
Storage temperature range	Tstg	-65～150	℃
Junction Temperature	TJ	150	℃
Electrostatic ESD	Body mode (HBM)	4000	v

Electrical Properties

V DD = + 3V or + 5V, ref InP = + 1.225v or + 2.5V; Ref Inn = GND, xi = 2.4576mhz, Ta = 25 ℃, unless otherwise specified)					
Parameter Name	**Test Conditions**	**Minimum**	**Type value**	**Maximum**	**Unit**
Resolution	Ensure that the filter notch is < 60Hz		16		Bits
Integral nonlinearity			0	±0.003	%of FSR
Unipolar offset drift			0.5		μ V/℃
Bipolar zero drift	PGA=1-4		0.5		μ V/℃
	PGA=8-128		0.1		μ V/℃
Full scale drift			0.5		μ V/℃
Gain error drift			0.5		ppm of FSR/ ℃
Bipolar negative full scale error		0	±0.001	±0.003	%of FSR/℃
Bipolar negative full scale drift			1		μ V/℃
			0.6		μ V/℃
REF IN absolute/common mode voltage		0		V DD	v
AIN absolute / common mode voltage	BUFEN=0	-0.03		V_{DD} +0.03	v
	BUFEN=1	0.05		V_{DD} -1.5	v
AIN input current				1	nA
AIN acquisition capacitance				10	pF
AIN differential voltage	Unipolar input	0		V_{REP} /GAIN	
	Bipolar Inputs	-V_{REP} /GAIN		V_{REP} /GAIN	
AIN stable sampling rate	Gain 1-4	GAIN × f_{CLKIN} /64			
	Gain 8-128	f_{CLKIN} /8			
REFINP—REFINN difference	VDD=3V,Vref=1.225V	1		1.75	v
	VDD=5V,Vref=2.5V	1		3.5	
REF INN input stable sampling rate			f_{CLKIN} /64		
Input voltage (except SCLK and XI)					
VIL	V_{DD} =5V			0.8	v
	V_{DD} =3V			0.4	v

VIH		2.0			v
Schmidt trigger input SCLK					
V_{T+}	V_{DD} =5V	1.4		3	v
V T _		0.8		1.4	
V_{T+} —V_{T-}		0.4		0.8	
V_{T+}	V_{DD} =3V	1		2.5	
V_{T-}		0.4		1.1	
V_{T+} V_{T-}		0.375		0.8	
XI					
Input low level	V_{DD} =5V			0.8	v
Input high level		3.5			
Input low level	V_{DD} =3V			0.4	
Input high level		2.5			
Data output coding	Unipolarity	Binary system			
	Bipolar	Offset binary code			

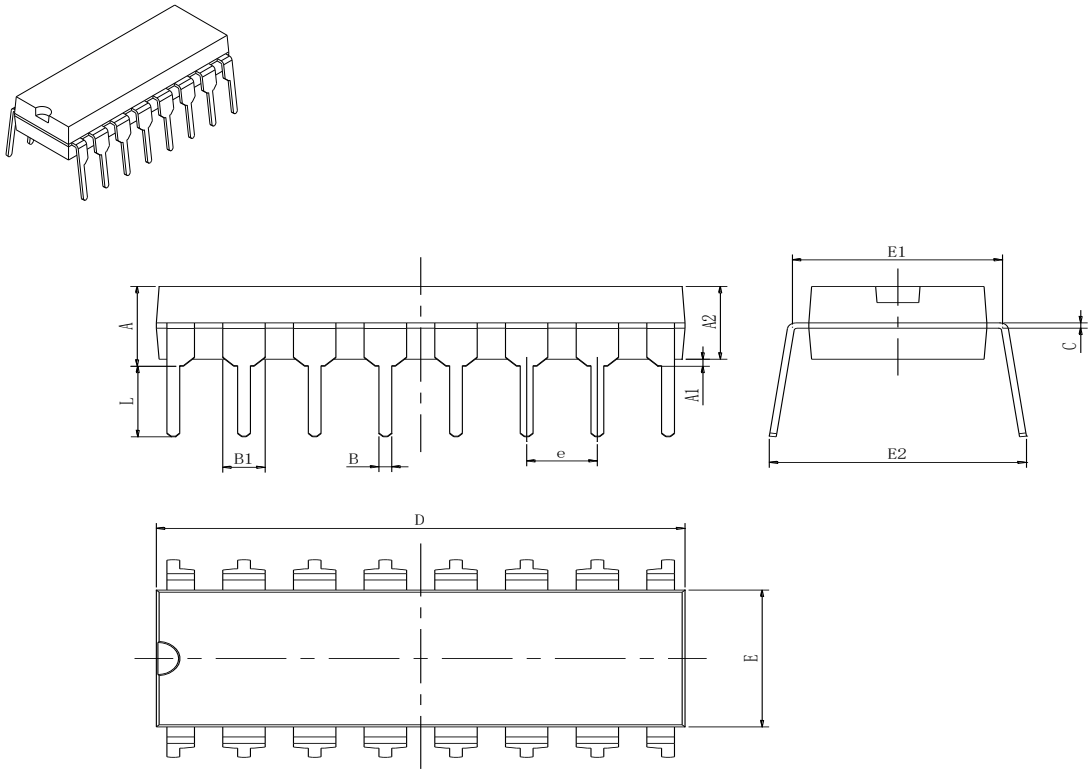
Power parameter characteristics

Parameter Name	Test Conditions			Minimum	Type value	Maximum	Unit
	BUFEN	f_{CLKIN} （MHZ）	Gain				
When the power supply voltage is 3V, the digital IO interface or control port is grounded or connected to VDD (XI and OSCDIS = 1)							
Supply current	0	1	1-128			0.32	mA
	1	1	1-128			0.6	
	0	2.4576	1-4			0.4	
	0	2.4576	8-128			0.6	
	1	2.4576	1-4			0.7	
	1	2.4576	8-128			1.1	
When the power supply voltage is 5V, the digital IO interface or control port is grounded or connected to VDD (XI and OSCDIS = 1)							
Supply current	0	1	1-128			0.45	mA
	1	1	1-128			0.7	
	0	2.4576	1-4			0.6	
	0	2.4576	8-128			.85	
	1	2.4576	1-4			0.9	
	1	2.4576	8-128			1.3	
Power down mode current	V_{DD} =5V, XI=0V /V_{DD}					16	UA
	V_{DD} =3V， XI=0V / V_{DD} .					8	
Power Supply Rejection Ratio	Supply voltage		Gain		86		DB
	VDD=3V		1				

	VDD=3V	2		78		
	VDD=3V	4		85		
	VDD=3V	8-128		93		
	VDD=5V	1		90		
	VDD=5V	2		78		
	VDD=5V	4		84		
	VDD=5V	8-128		91		

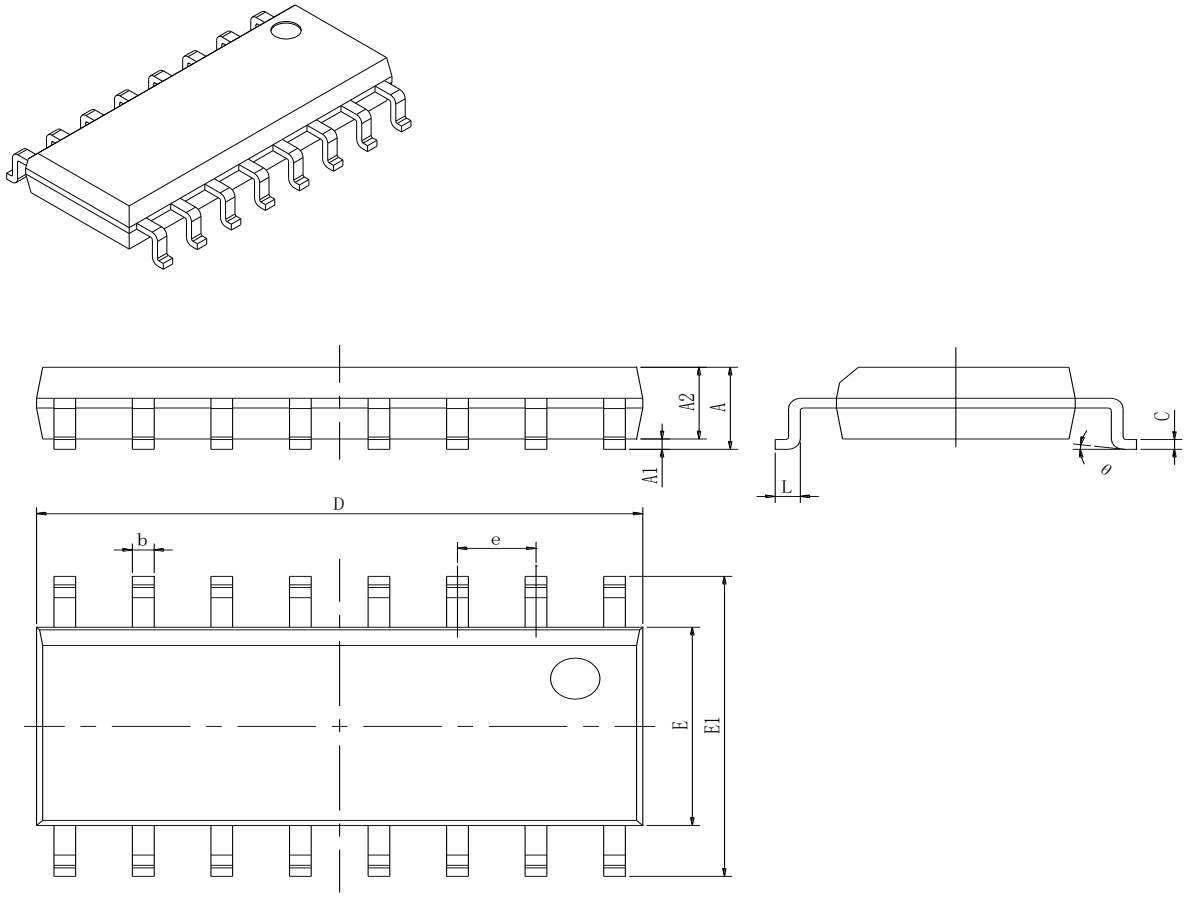
Packaging diagram

DIP16



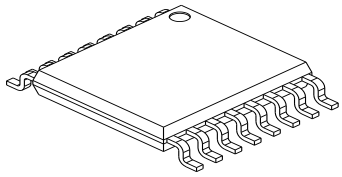
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

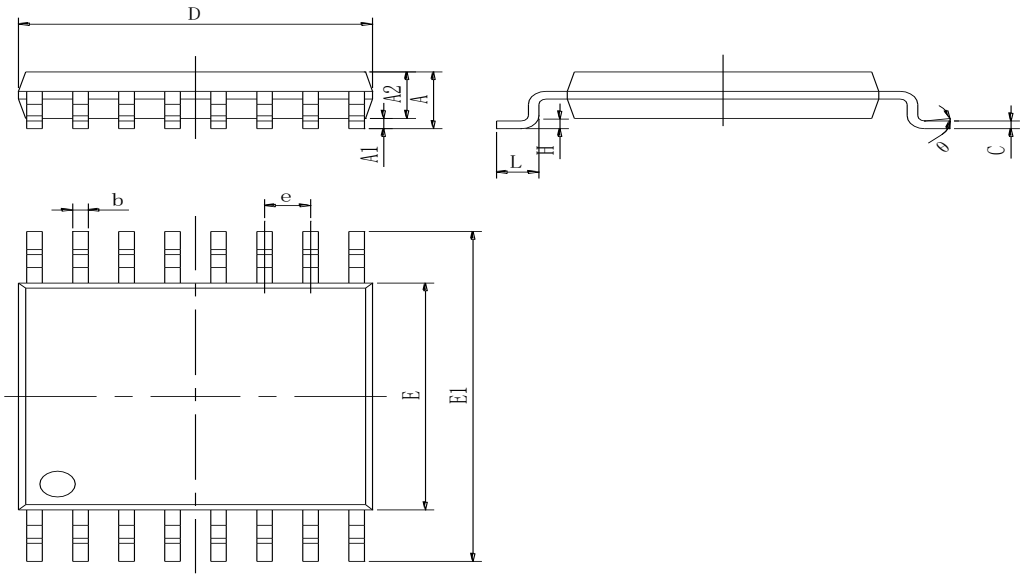
SOIC16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.35	2.65	0.0926	0.1043
A1	0.1	0,3	0.004	0.0118
A2	2.25	2.35	0.0922	0.0925
b	0.35	0.49	0.0138	0.0192
c	0.23	0.32	0.0091	0.0125
D	10	10.5	0.3977	0.4133
E	7.4	7.6	0.2914	0.2992
E1	10	10.65	0.3937	0.4
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.0157	0.050
θ	0°	8°	0°	8°

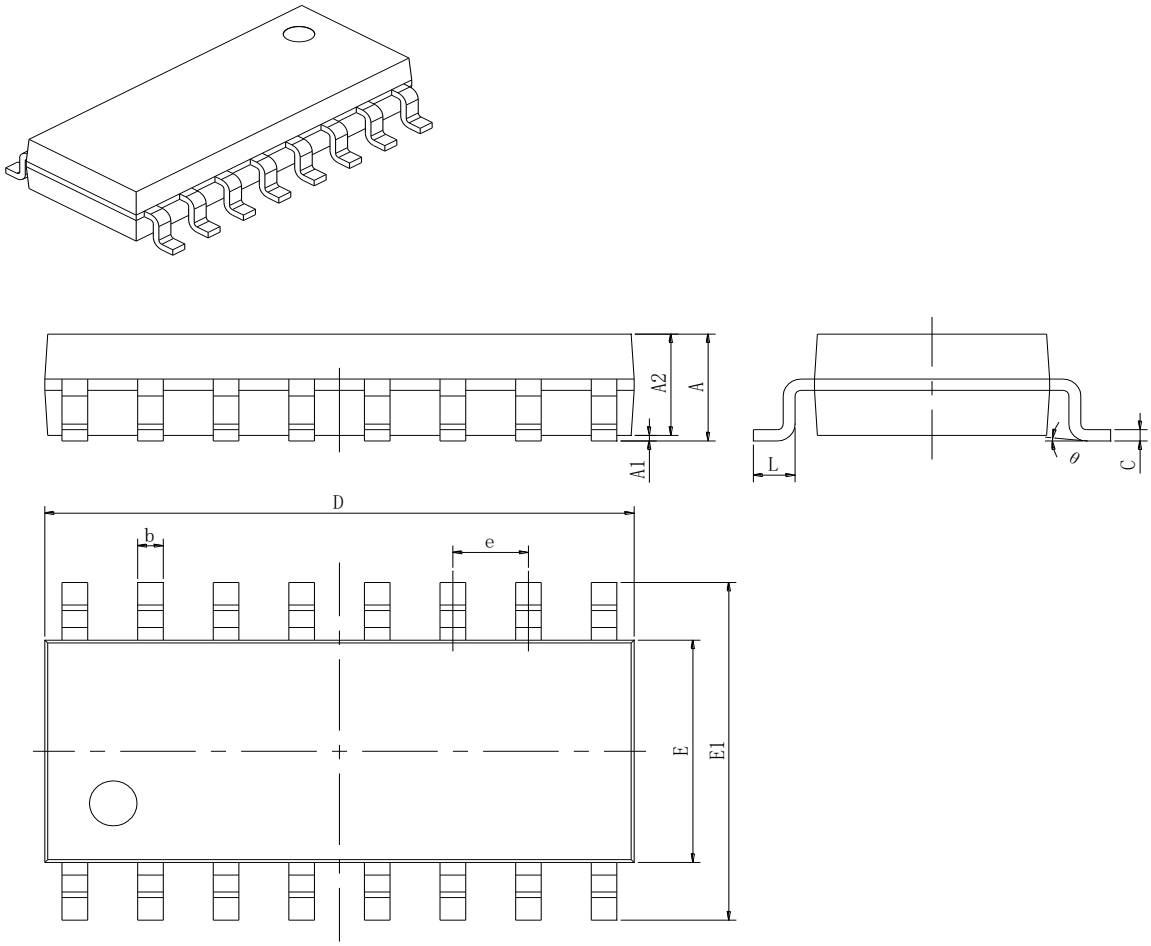
TSSOP16





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	4.900	5.100	0.193	0.201
D1	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.200	2.400	0.087	0.094
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65（BSC）		0.026(BSC)	
L	0.500	0.700	0.02	0.028
H	0.25(TYP)		0.01(T YP)	
θ	1°	7°	1°	7°

SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°