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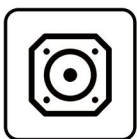
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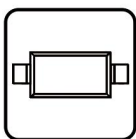
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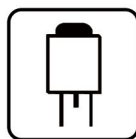
電源管理



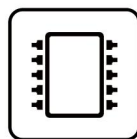
顯示驅動



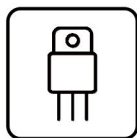
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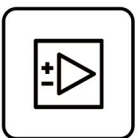
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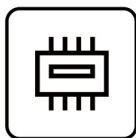
觸摸芯片



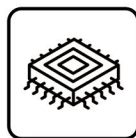
MOS管



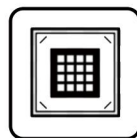
運算放大器



存儲芯片



MCU



串口通信

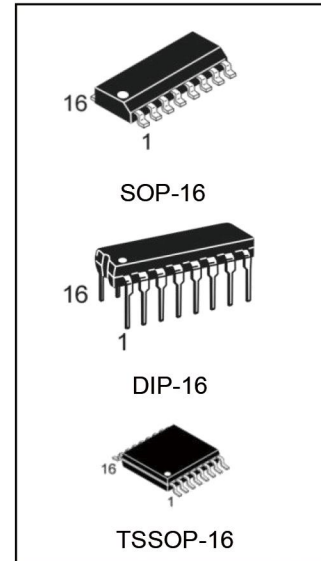
74HC192

產品規格說明書

Presettable synchronous BCD decade up/down counter

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI



PACKAGE/ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC192N	DIP-16	74HC192	TUBE	1000pcs/Box
74HC192M/TR	SOP-16	74HC192	REEL	2500pcs/Reel
74HC192MT/TR	TSSOP-16	HC192	REEL	2500pcs/Reel
74HCT192N	DIP-16	74HCT192	TUBE	1000pcs/Box
74HCT192M/TR	SOP-16	74HCT192	REEL	2500pcs/Reel
74HCT192MT/TR	TSSOP-16	HCT192	REEL	2500pcs/Reel

GENERAL DESCRIPTION

The 74HC/HCT192 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT192 are synchronous BCD up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The “192” contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock wave forms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CPD, CPU to Qn	$C_L = 15 \text{ pF}$; $V_{CC} = 5\text{V}$	20	20	ns
f_{max}	maximum clock frequency		40	45	MHz
T_L	Soldering temperature	10s	-	245	$^{\circ}\text{C}$
C_i	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	28	pF

Notes: 1、CPD is used to determine the dynamic power dissipation (PD in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times F_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times F_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2、For HC the condition is $V_i = \text{GND to VCC}$

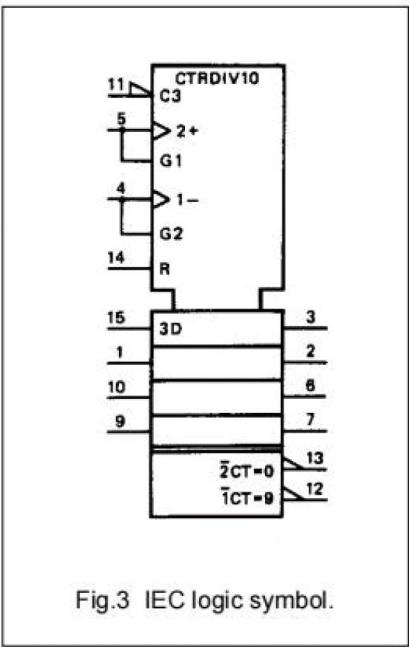
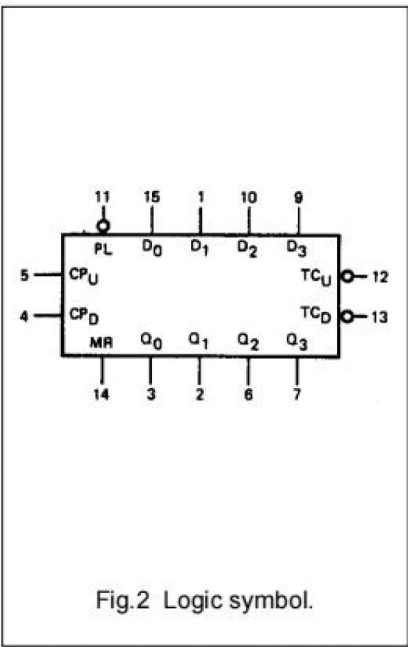
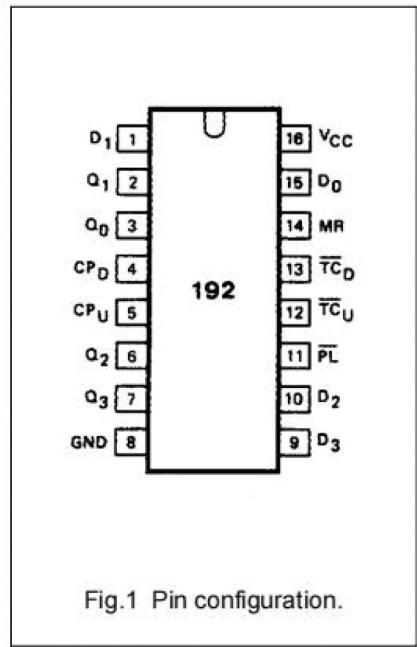
For HCT the condition is $V_i = \text{GND to VCC-1.5V}$

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q0 to Q3	flip-flop outputs
4	CP _D	count down clock input(1)
5	CP _U	count up clock input(1)
8	GND	ground (0 V)
11	$\overline{\text{PL}}$	asynchronous parallel load input (active LOW)
12	$\overline{\text{TC}}_{\text{U}}$	terminal count up (carry) output (active LOW)
13	$\overline{\text{TC}}_{\text{D}}$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D ₀ to D ₃	data inputs
16	V _{CC}	positive supply voltage

Note

1. LOW-to-HIGH, edge triggered



FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CPU	CPD	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	Qn = Dn				L	H
	L	L	H	X	H	X	X	H	Qn = Dn				H	H
count up	L	H		H	X	X	X	X	count up				H ⁽²⁾	H
count down	L	H	H		X	X	X	X	count down				H	H ⁽³⁾

Notes

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

$\overline{TC}_U$ = CPU at terminal count up (HLLH)

$\overline{TC}_D$ = CPD at terminal count down (LLLL)

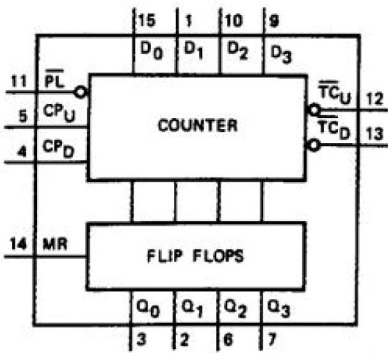
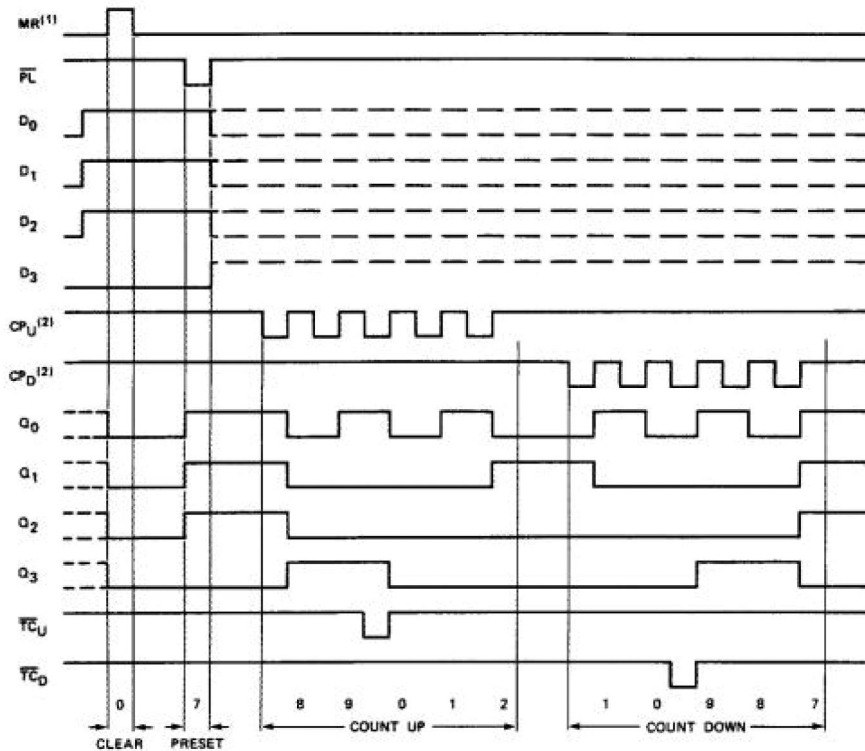


Fig.4 Functional diagram.



Clear overrides load, data and count inputs.

When counting up the count down clock input (CPD) must be HIGH, when counting down the count up clock input (CPU) must be HIGH.

Sequence

Clear (reset outputs to zero); load (preset) to BCD seven; count up to eight, nine, terminal count up, zero, one and two; count down to one, zero, terminal count down, nine, eight, and seven.

Fig.5 Typical clear, load and count sequence.

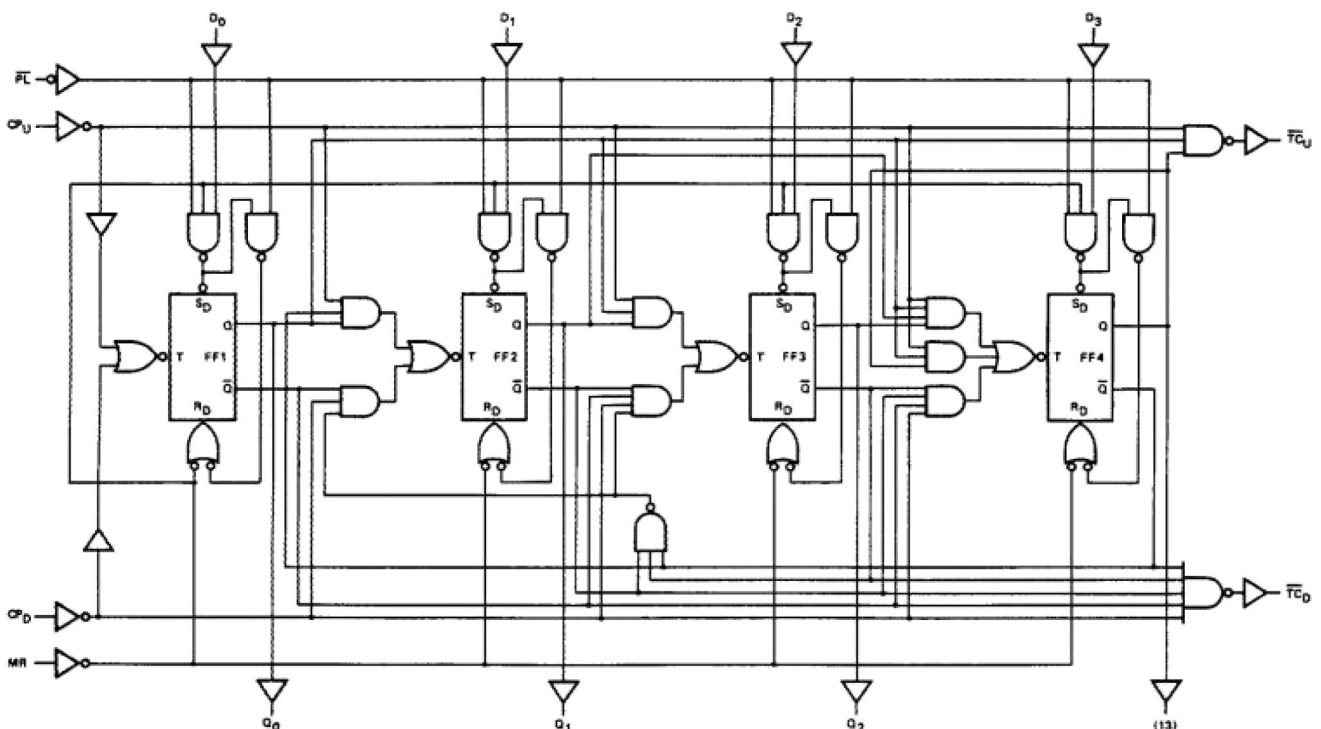


Fig.6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	Tamb (°C)							UNIT	TEST CONDITIONS	
		74HC								VCC (V)	WAVEFORMS
		25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP _U , CP _D to Qn		66	215		270		325	ns	2.0	Fig.7
			24	43		54		65		4.5	
			19	37		46		55		6.0	
t _{PHL} / t _{PLH}	propagation delay CP _U to TC _U		33	125		155		190	ns	2.0	Fig.8
			12	25		31		38		4.5	
			10	21		26		32		6.0	
t _{PHL} / t _{PLH}	propagation delay CP _D to TC _D		39	125		155		190	ns	2.0	Fig.8
			14	25		31		38		4.5	
			11	21		26		32		6.0	
t _{PHL} / t _{PLH}	propagation delay P _L to Qn		69	215		270		325	ns	2.0	Fig.9
			25	43		54		65		4.5	
			20	37		46		55		6.0	
t _{PHL}	propagation delay MR to Qn		63	200		250		300	ns	2.0	Fig.10
			23	40		50		60		4.5	
			18	34		43		51		6.0	
t _{PHL}	propagation delay Dn to Qn		91	275		345		415	ns	2.0	Fig.9
			33	55		69		83		4.5	
			26	47		59		71		6.0	
t _{PHL}	propagation delay Dn to Qn		80	240		300		360	ns	2.0	Fig.9
			29	48		60		72		4.5	
			23	41		51		61		6.0	
t _{PHL} / t _{PLH}	propagation delay P _L to TCU, P _L to T _C _D		102	315		395		475	ns	2.0	Fig.12
			37	63		79		95		4.5	
			30	54		67		81		6.0	
t _{PHL} / t _{PLH}	propagation delay MR to T _C _U , MR to T _C _D		96	285		355		430	ns	2.0	Fig.12
			35	57		71		86		4.5	
			28	48		60		73		6.0	
t _{PHL} / t _{PLH}	propagation delay Dn to T _C _U , Dn to T _C _D		83	290		365		435	ns	2.0	Fig.12
			30	58		73		87		4.5	
			24	49		62		74		6.0	
t _{THL} / t _{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.10
			7	15		19		22		4.5	
			6	13		16		19		6.0	

SYMBOL	PARAMETER	Tamb (°C)							UNIT	TEST CONDITIONS	
		74HC								VCC (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
tW	up clock pulse width HIGH or LOW	120	39		150		180		ns	2.0	Fig.7
		24	14		30		36			4.5	
		20	11		26		31			6.0	
tW	down clock pulse width HIGH or LOW	140	50		175		210		ns	2.0	Fig.7
		28	18		35		42			4.5	
		24	14		30		36			6.0	
tW	master reset pulse width HIGH	80	22		100		120		ns	2.0	Fig.10
		16	8		20		24			4.5	
		14	6		17		20			6.0	
tW	parallel load pulse width LOW	80	22		100		120		ns	2.0	Fig.9
		16	8		20		24			4.5	
		14	6		17		20			6.0	
trem	removal time PL to CPU, CPD	50	3		65		75		ns	2.0	Fig.9
		10	1		13		15			4.5	
		9	1		11		13			6.0	
trem	removal time MR to CPU, CPD	50	0		65		75		ns	2.0	Fig.10
		10	0		13		15			4.5	
		9	0		11		13			6.0	
tsu	set-up time Dn to PL	80	22		100		120		ns	2.0	Fig.11 note: CP _U = CP _D = HIGH
		16	8		20		24			4.5	
		14	6		17		20			6.0	
th	hold time Dn to PL	0	14		0		0		ns	2.0	Fig.11
		0	5		0		0			4.5	
		0	4		0		0			6.0	
th	hold time CPU to CPD, CPD to CPU	80	19		100		120		ns	2.0	Fig.13
		16	7		20		24			4.5	
		14	6		17		20			6.0	
fmax	maximum up, down clock pulse frequency	4.0	12		3.2		2.6		MHz	2.0	Fig.7
		20	36		16		13			4.5	
		24	43		19		15			6.0	

DC CHARACTERISTICS FOR 74HCT

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
Dn	0.35
CP _U , CP _D	1.40
PL	0.65
MR	1.05

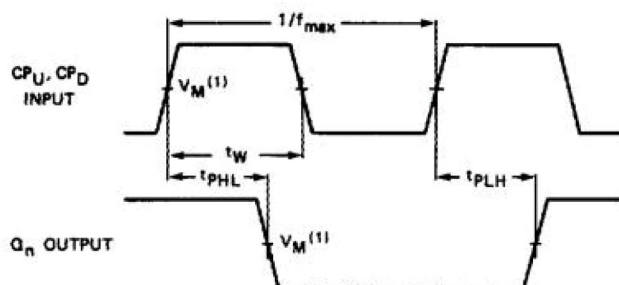
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	Tamb (°C)							UNIT	TEST CONDITIONS	
		74HCT								VCC (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP _U , CP _D to Qn		23	43		54		65	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay CPU to $\overline{TC}_U$		16	30		38		45	ns	4.5	Fig.8
t _{PHL} / t _{PLH}	propagation delay CPD to $\overline{TC}_D$		17	30		38		45	ns	4.5	Fig.8
t _{PHL} / t _{PLH}	propagation delay $\overline{PL}$ to Qn		28	46		58		69	ns	4.5	Fig.9
t _{PHL}	propagation delay MR to Qn		24	40		50		60	ns	4.5	Fig.10
t _{PHL} / t _{PLH}	propagation delay Dn to Qn		36	62		78		93	ns	4.5	Fig.9
t _{PHL} / t _{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}_U$, PL to $\overline{TC}_D$		36	64		80		96	ns	4.5	Fig.12
t _{PHL} / t _{PLH}	propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$		36	64		80		96	ns	4.5	Fig.12
t _{PHL} / t _{PLH}	propagation delay Dn to $\overline{TC}_U$, Dn to $\overline{TC}_D$		33	58		73		87	ns	4.5	Fig.12
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.10
t _w	up, down clock pulse width HIGH or LOW	25	14		31		38		ns	4.5	Fig.7

t_w	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig.10
t_w	parallel load pulse width LOW	20	10		25		30		ns	4.5	Fig.9
trem	removal time $\overline{PL}$ to CP_U, CP_D	10	1		13		15		ns	4.5	Fig.9
trem	removal time MR to CP_U, CP_D	10	2		13		15		ns	4.5	Fig.10
tsu	set-up time D_n to $\overline{PL}$	16	8		20		24		ns	4.5	Fig.11 note: $CP_U=CP_D =$ HIGH
th	hold time D_n to $\overline{PL}$	0	-6		0		0		ns	4.5	Fig.11
th	hold time CP_U to CP_D , CP_D to CP_U	20	9		25		30		ns	4.5	Fig.13
fmax	maximum up, down clock pulse frequency	20	41		16		13		MHz	4.5	Fig.7

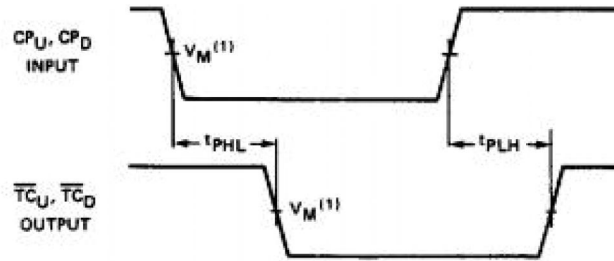
AC WAVEFORMS



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

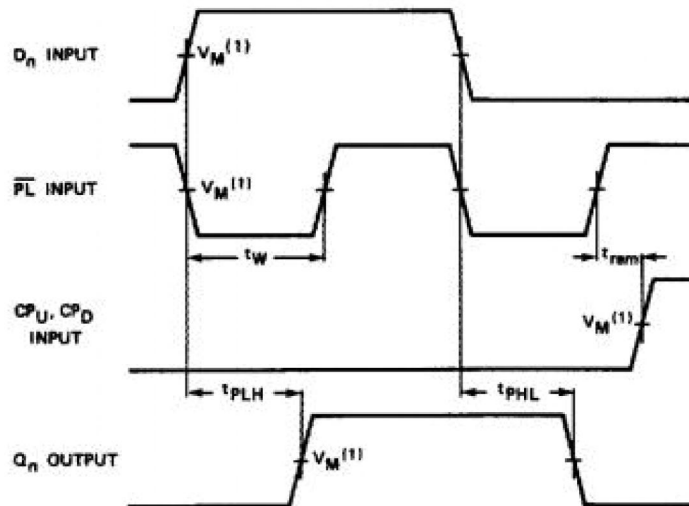
Fig.7 Wave forms showing the clock (CP_U, CP_D) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

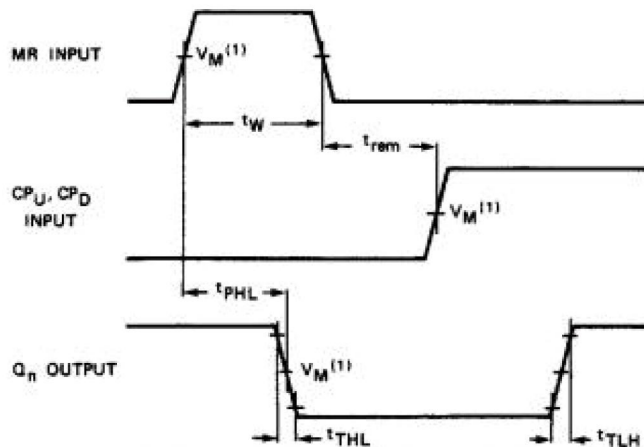
Fig.8 Wave forms showing the clock (CP_U , CP_D) to terminal count output ($\overline{TC}_U$, $\overline{TC}_D$) propagation delays.



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

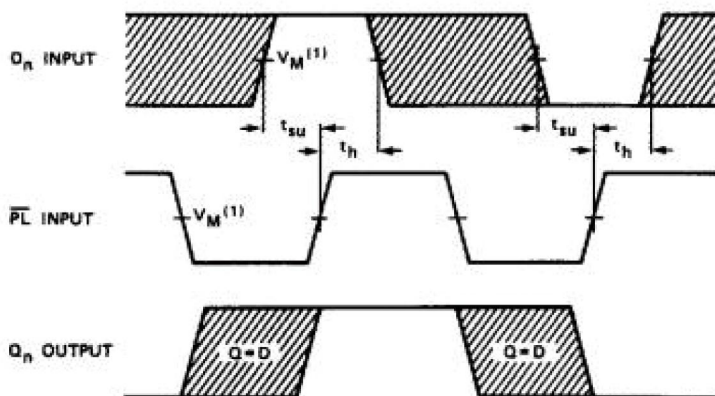
Fig.9 Wave forms showing the parallel load input ($\overline{PL}$) and data (D_n) to Q_n output propagation delays and $\overline{PL}$ removal time to clock input (CP_U , CP_D).



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.10 Wave forms showing the master reset input (MR) pulse width, MR to Q_n propagation delays, MR to CP_U , CP_D removal time and output transition times.

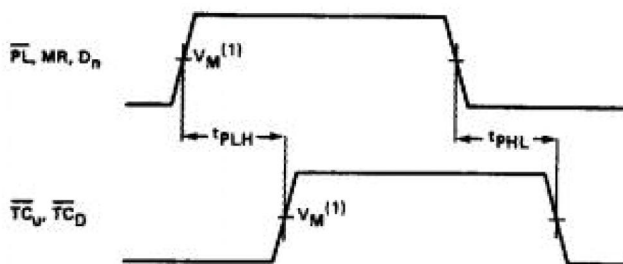


The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

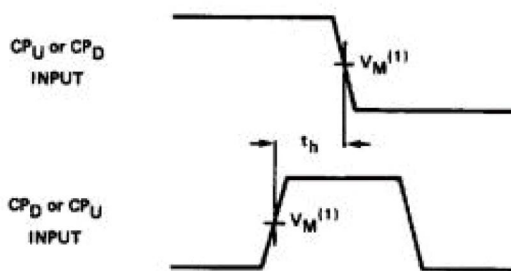
Fig.11 Waveforms showing the data input (D_n) to parallel load input ($\overline{PL}$) set-up and hold times.



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.12 Waveforms showing the data input (D_n), parallel load input ($\overline{PL}$) and the master reset input ($\overline{MR}$) to the terminal count outputs ($\overline{TC_U}$, $\overline{TC_D}$) propagation delays.



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.13 Waveforms showing the CP_U to CP_D or CP_D to CP_U hold times.

APPLICATION INFORMATION

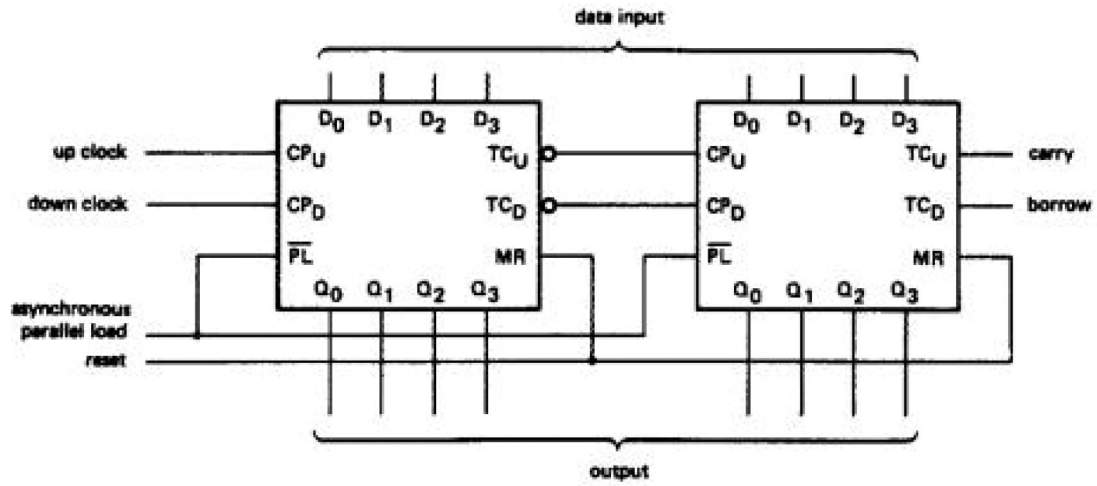
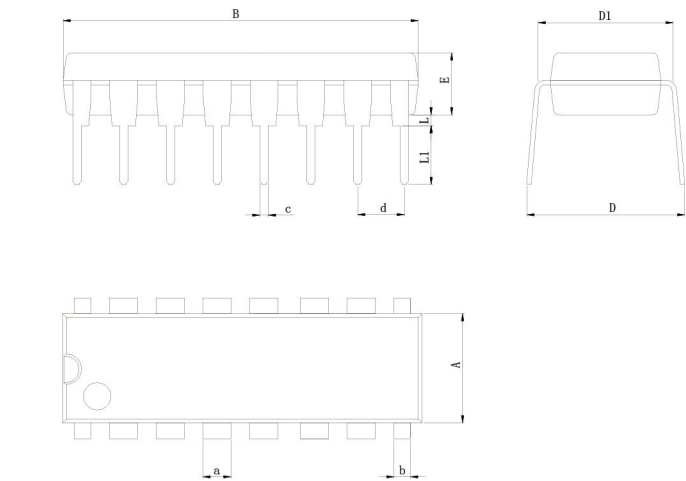


Fig.14 Cascaded up/down counter with parallel load.

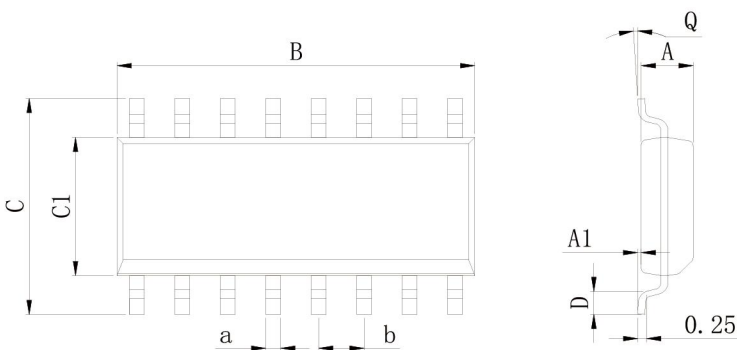
PHYSICAL DIMENSIONS

DIP-16



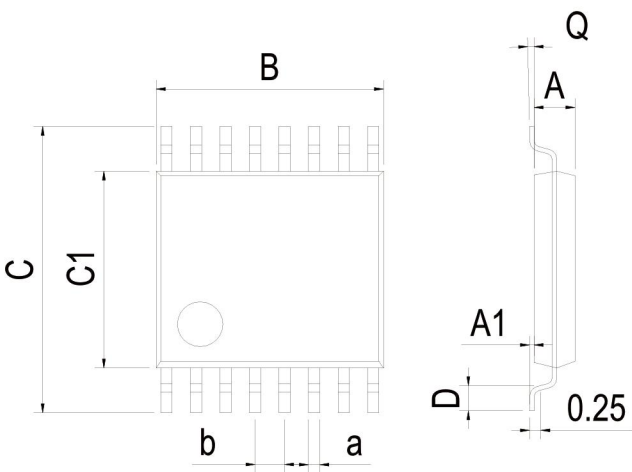
Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	