MPQ3438

2A, 10V, High-Efficiency, Fully Integrated, Synchronous Boost Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ3438 is a 2.6MHz, quasi-fixed frequency, highly integrated boost converter that operates across a wide 0.8V to 10V input voltage (V_{IN}) range. The MPQ3438 starts up from an input voltage (V_{ST}) as low as 2.7V and supports a switching current limit up to 2A with integrated, low on resistance ($R_{DS(ON)}$) power MOSFETs.

The MPQ3438 adopts adaptive constant-off-time (COT) control topology to provide fast transient response. An internal frequency loop ensures that the operating frequency is fixed in steady state. The low-side MOSFET (LS-FET)'s cycle-by-cycle current limit prevents current runaway, and the high-side MOSFET (HS-FET) eliminates the need for an external Schottky diode.

Full protections include configurable input under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MPQ3438 is available in a QFN-8 (1.5mmx2mm) package.

FEATURES

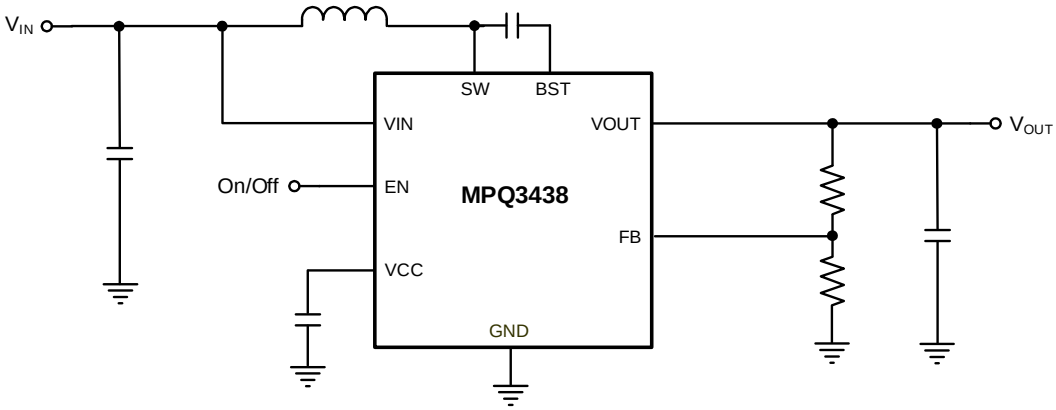
- Flexible Input Voltage (V_{IN}) and Output Voltage (V_{OUT}) Operating Range
  - 2.7V to 10V Start-Up Input Voltage (V_{ST})
  - 0.8V to 10V Operating V_{IN}
  - 1.25 x V_{IN} to 16V V_{OUT}
  - Switching Current Limit Up to 2A
- Reduces Board Size and BOM
  - 2.6MHz Fixed Switching Frequency (f_{SW})
  - Available in a QFN-8 (1.5mmx2mm) Package
  - Integrated 55mΩ and 100mΩ Power MOSFETs
- Additional Features
  - Adaptive Constant-Off-Time (COT) Control for Fast Transient Response
  - Power-Save Mode (PSM) at Light Loads
  - Internal Soft Start (SS) and Compensation
  - Frequency Foldback for Smooth Start-Up
  - Configurable Under-Voltage Lockout (UVLO) and Hysteresis
  - Over-Temperature Protection (OTP) and Over-Voltage Protection (OVP)
  - Available in AEC-Q100 Grade 1
- Functional Safety System Design Capability
  - MPSafe™-Compatible: Functional Safety Supporting Document Available

MPSafe™ FuSa Compatible

APPLICATIONS

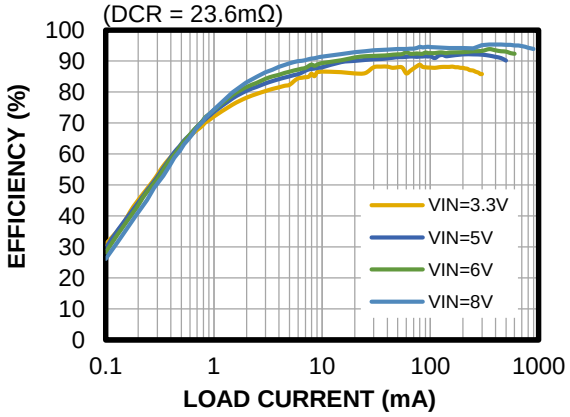
- Automotive Mechanical Power Supplies
- Automotive LED Drivers
- Automotive Infotainment

TYPICAL APPLICATION



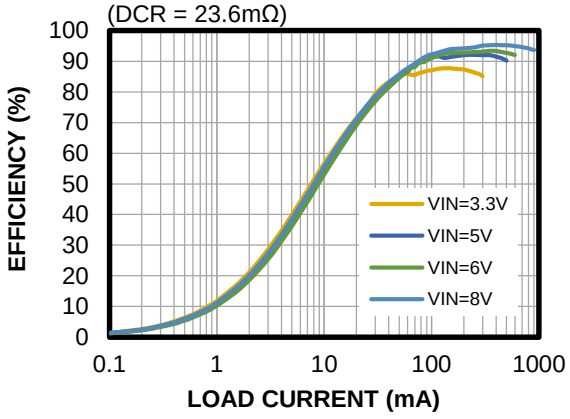
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH
(DCR = 23.6mΩ)



Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH
(DCR = 23.6mΩ)



ORDERING INFORMATION

Part Number* (1)	Operating Mode	Package	Top Marking	MSL Rating**
MPQ3438GQHE-xxxx-AEC1***	Default	QFN-8 (1.5mmx2mm)	*See Below*	1
MPQ3438GQHE-0000-AEC1***	Power-save mode (PSM) under light-load conditions	QFN-8 (1.5mmx2mm)	*See Below*	1
MPQ3438GQHE-0001-AEC1***	Forced continuous conduction mode (FCCM)	QFN-8 (1.5mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3438GQHE-0000-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

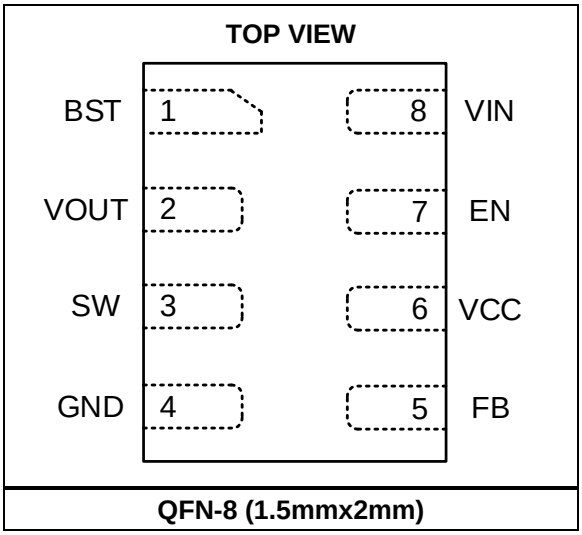
TOP MARKING

$\overline{\text{NL}}$

LL

NL: Product code of the MPQ3438GQHE-xxxx-AEC1
LL: Lot number

PACKAGE REFERENCE



QFN-8 (1.5mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between the BST and SW pins to power the synchronous high-side MOSFET (HS-FET).
2	VOUT	**Output.** The VOUT pin is connected to the drain of the HS-FET. If the output voltage (V_{OUT}) exceeds the input voltage (V_{IN}), and V_{IN} is below 3.4V, then VOUT powers VCC.
3	SW	**Converter switch.** The SW pin is connected to the drain of the internal low-side MOSFET (LS-FET) and the source of the internal synchronous HS-FET. Connect SW to the power inductor.
4	GND	**Power ground.**
5	FB	**Feedback input.** To set V_{OUT}, connect the FB pin to the external feedback divider's middle point between the output and AGND. The feedback voltage (V_{FB}) is 1V, and the set V_{OUT} must exceed V_{IN} by 1.25 times. Place the resistor divider as close to VOUT as possible. Avoid placing vias on the VOUT traces.
6	VCC	**Internal bias supply.** Decouple the VCC pin with a 1μF ceramic capacitor, placed as close to VCC as possible. When V_{IN} exceeds 3.4V, VCC is powered by VIN. Otherwise, VCC is powered by the higher voltage between V_{IN} and V_{OUT}. If the biased voltage connected to VCC exceeds 3.4V, the regulators connected between VIN and VOUT are disabled. The VCC regulator starts working when V_{IN} exceeds 0.9V and EN is high. Supply VIN with a power source exceeding 2.7V during VIN start-up to provide VCC with sufficient power voltage.
7	EN	**Chip enable control.** Connect the EN pin to VIN for automatic start-up. EN can configure the V_{IN} under-voltage lockout (UVLO) threshold. Do not float this pin. EN must be externally pulled up or pulled down. Pull EN above the specified threshold (1.2V) to initiate boost operation.
8	VIN	**Input supply.** Supply the VIN pin with a power source exceeding 2.7V during VIN start-up to provide VCC with sufficient power. V_{IN} must be below V_{OUT} / 1.25.

ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.3V (-2V for <10ns)
.....to +24V (28V for <10ns)
VIN, EN, VOUT .....-0.3V to +24V
BST ..... -0.3V to V_{SW} + 4.5V
All other pins .....-0.3V to +4.5V
HS-FET body diode inrush current 30A (2)
Continuous power dissipation (T_A = 25°C) (3)
..... 2.1W (9)
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (4)
Charged-device model (CDM) ..... Class C2b (5)

Recommended Operating Conditions (6)

Start-up input voltage (V_{ST}) .....2.7V to 10V
Operating input voltage (V_{IN}).....0.8V to 10V
Start-up input voltage with VCC bias (V_{ST2}) .....
.....0.9V to 10V
Maximum external VCC bias voltage..... 3.6V (7)
Boost output voltage (V_{OUT}) .....1.25 x V_{IN} to 16V
Operating junction temp (T_J) .....
..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

JESD51-7.....84....8.1...°C/W (8)
EVQ3438-QH-00A.....59.....°C/W (9)

Ψ_{JT}

JESD51-7.....2.85..°C/W (8)
EVQ3438-QH-00A.....6.5....°C/W (9)

Notes:

1) Exceeding these ratings may damage the device.
2) During input start-up, the inrush current through the HS-FET body diode should be limited to below 30A. See the Input Start-Up Inrush Current Control section on page 26 for more details.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002. With the exception of the VCC and VIN pins that can only withstand -1.5kV, all the other pins meet Class 2.
5) Per AEC-Q100-011.
6) The device is not guaranteed to function outside of its operating conditions.
7) When the external VCC biased voltage is below the normal VCC regulated voltage, the external power must prevent current flowing out of VCC.
8) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from junction-to-case bottom.
9) Measured on the EVQ3438-QH-00A, a 4-layer, 2oz copper PCB (6.3cmx6.3cm). The Ψ_{JT} value shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage (10)	V_{ST}	No VCC bias	2.7		10	V
		V_{CC} = 3V	0.9		10	V
Operating input voltage	V_{IN}		0.8		10	V
Operating VCC voltage (11)	V_{CC}	V_{IN} = 2.7V, 0mA	2.3	2.55		V
		V_{IN} = 10V, 0mA to 10mA		3.4		V
V_{CC} under-voltage lockout (UVLO) rising threshold (11)	$V_{CC\_UVLO\_RISING}$	V_{CC} rising	2.2	2.4	2.6	V
V_{CC} UVLO falling threshold	$V_{CC\_UVLO\_FALLING}$	V_{CC} falling	1.9	2.1	2.3	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN			2	µA
Quiescent current	I_Q	V_{FB} = 1.05V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on VIN			12	µA
		V_{FB} = 1.05V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on VOUT		150	200	µA
Enable (EN) Control						
EN turn-on threshold	V_{EN_ON}	V_{EN} rising (switching)	1.1	1.2	1.3	V
EN high threshold	V_{EN_H}	V_{EN} rising (micro power)			1	V
EN low threshold	V_{EN_L}	V_{EN} falling (micro power)	0.4			V
EN turn-on hysteresis current	I_{EN_HYS}	1V < V_{EN} < V_{EN_ON}	3.5	5	7	µA
EN input current	I_{EN}	V_{EN} = 0V,1.5V		0		µA
EN turn-on delay		EN enabled to switching, PSM		1800		µs
		EN enabled to switching, FCCM		500		µs
Frequency						
Switching frequency (12)	f_{SW}	V_{IN} = 3.3V, V_{OUT} = 12V, FCCM		2.6		MHz
Low-side MOSFET (LS-FET) minimum on time (13)	t_{MIN_ON}		80	100	125	ns
LS-FET minimum off time (13)	t_{MIN_OFF}		70	85	105	ns
Loop Control						
FB reference voltage	V_{FB}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.05V			50	nA
Soft-start time	t_{SS}		3.5	5	6	ms
Power MOSFET						
LS-FET on resistance	$R_{DS(ON)\_LS}$			55		mΩ
Synchronous high-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			100		mΩ
LS-FET leakage current		V_{SW} = 16V			1	µA
HS-FET leakage current		V_{OUT} = 16V, V_{SW} = 0V			1	µA

ELECTRICAL CHARACTERISTICS (*continued*)

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bootstrap (BST) Power						
BST voltage	V_{BST}	Boost mode		3.2		V
Current Limit						
Switching current limit	I_{PK_LIMIT}		1.7	2	2.7	A
HS-FET zero-current detection (ZCD)	I_{ZCD}		-50	0	+100	mA
Protections						
V_{OUT} over-voltage protection (OVP) threshold				24		V
V_{OUT} OVP hysteresis				0.5		V
FB OVP threshold				110		% of V_{REF}
FB OVP hysteresis				5		% of V_{REF}
Thermal Protection						
Thermal shutdown (13)	T_{SD}			165		°C
Thermal Shutdown hysteresis (13)	T_{SD_HYS}			25		°C

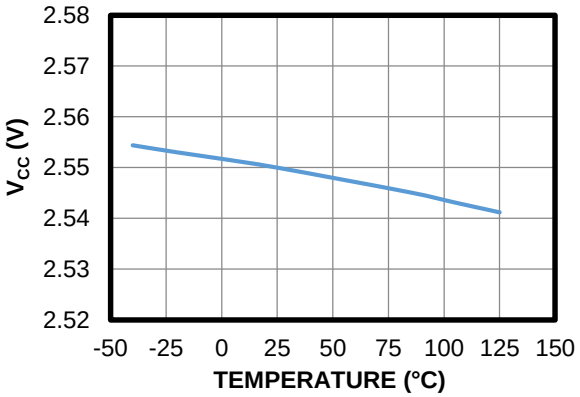
Notes:

10) During input start-up, the inrush current through the HS-FET body diode should be limited to below 30A. See the Input Start-Up Inrush Current Control section on page 26 for more details.
11) The VCC regulation voltage from 2.7V V_{IN} exceeds the V_{CC} UVLO rising threshold, which guarantees IC start-up with 2.7V V_{IN}.
12) The MPQ3438-0000's frequency is guaranteed by design and bench characterization.
13) Guaranteed by sample characterization. Not tested in production.

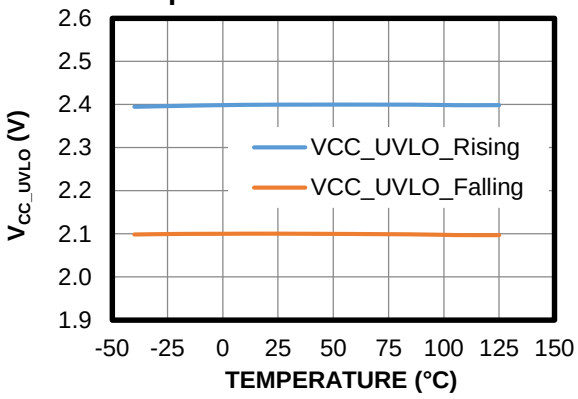
TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

V_{CC} vs. Temperature

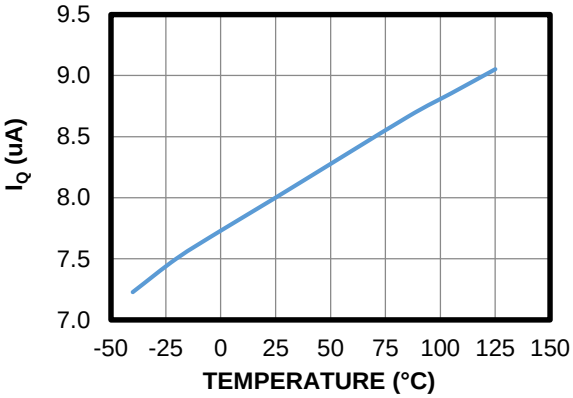


V_{CC} UVLO Threshold vs. Temperature



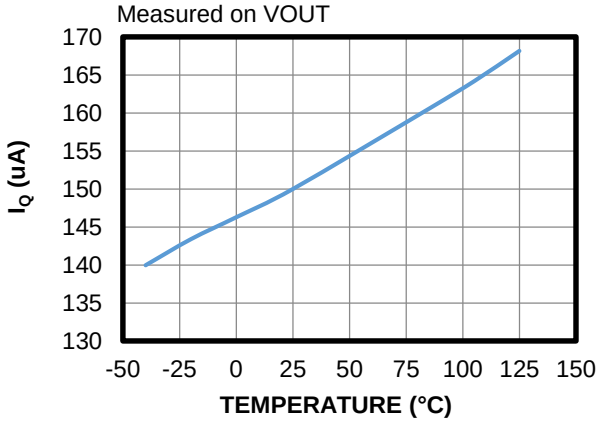
Quiescent Current vs. Temperature

Measured on VIN

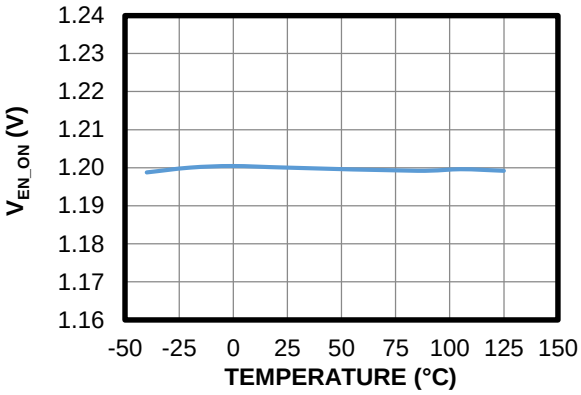


Quiescent Current vs. Temperature

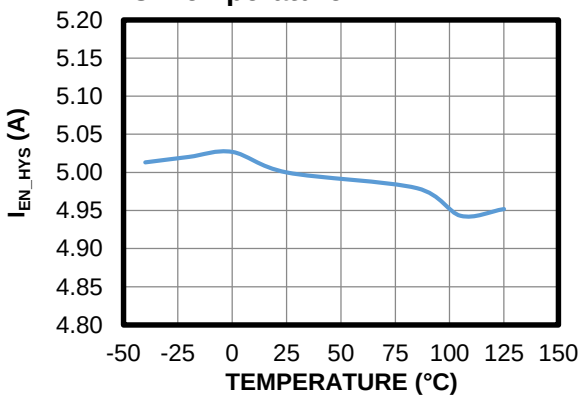
Measured on VOUT



EN Turn-On Threshold Voltage vs. Temperature



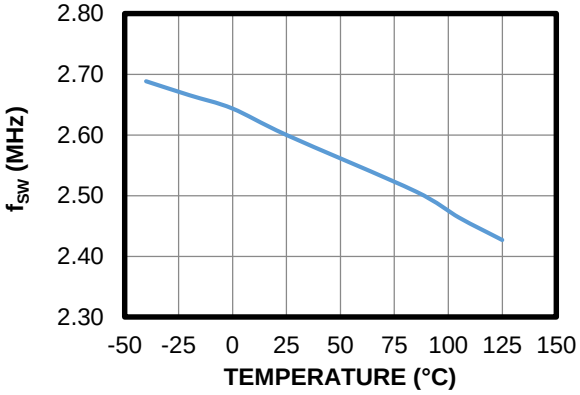
EN Turn-On Hysteresis Current vs. Temperature



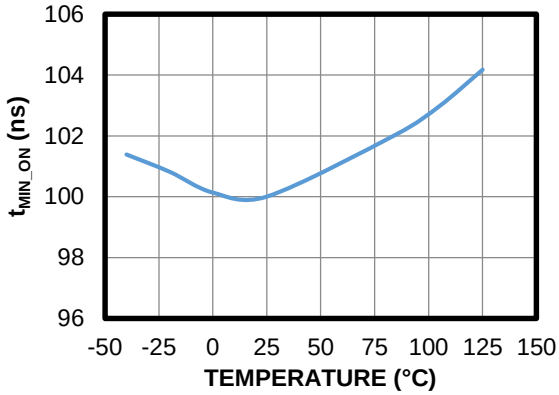
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

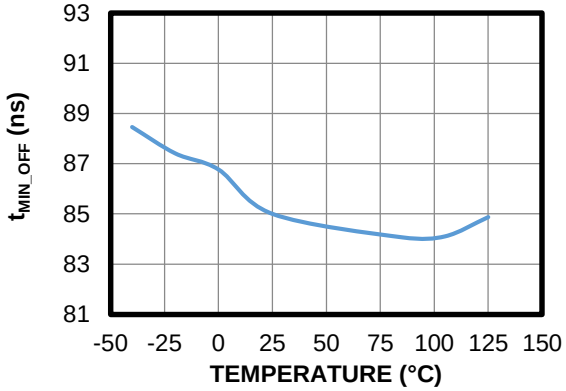
Switching Frequency vs. Temperature



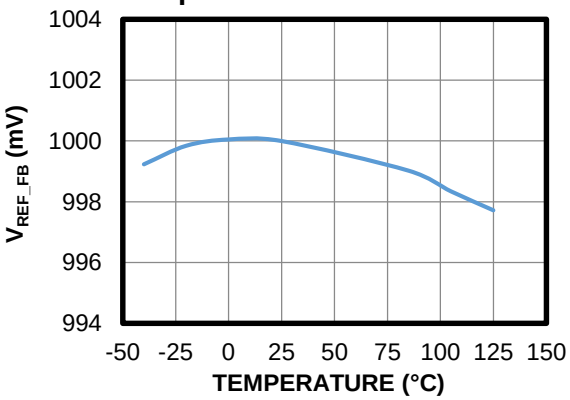
LS-FET Minimum On Time vs. Temperature



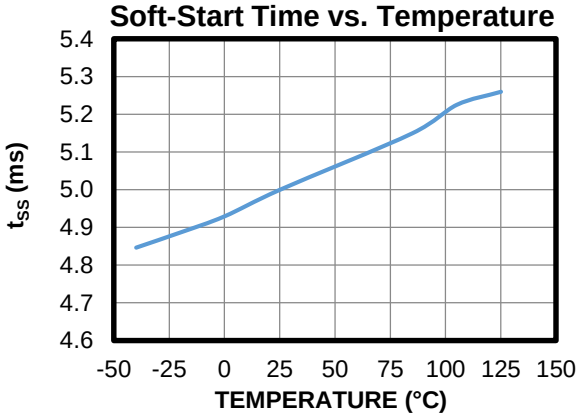
LS-FET Minimum Off Time vs. Temperature



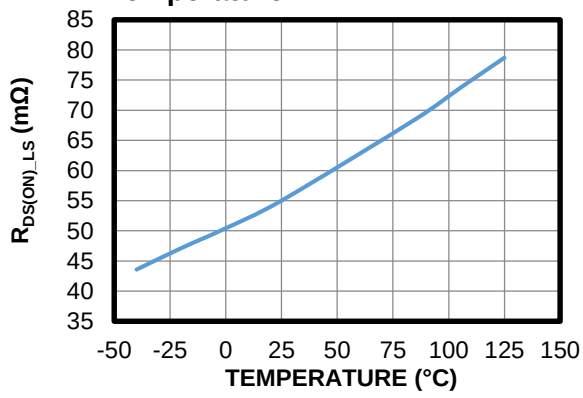
FB Reference Voltage vs. Temperature



Soft-Start Time vs. Temperature



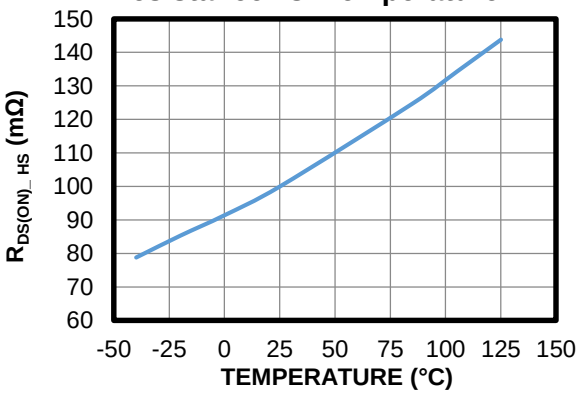
LS-FET On Resistance vs. Temperature



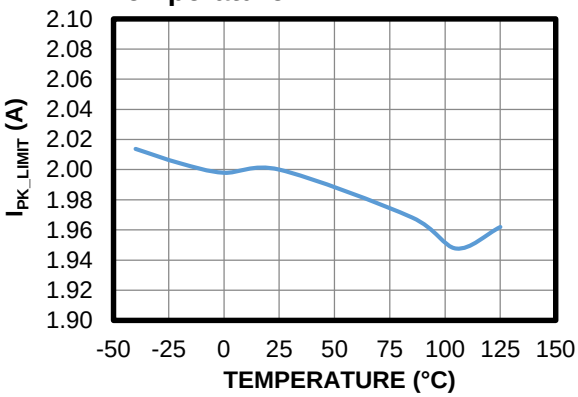
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

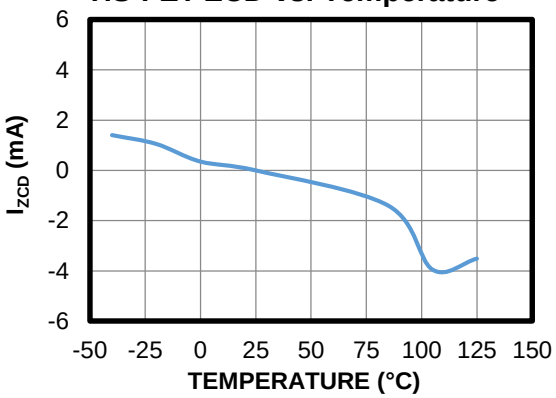
Synchronous HS-FET On Resistance vs. Temperature



Switching Current Limit vs. Temperature



HS-FET ZCD vs. Temperature

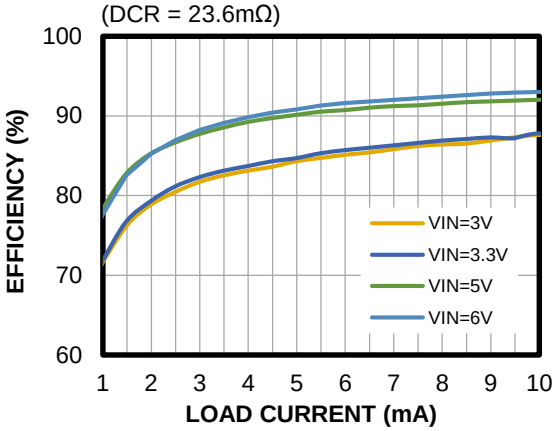


TYPICAL PERFORMANCE CHARACTERISTICS

MPQ3438-0000, V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 500mA, T_A = 25°C, unless otherwise noted.

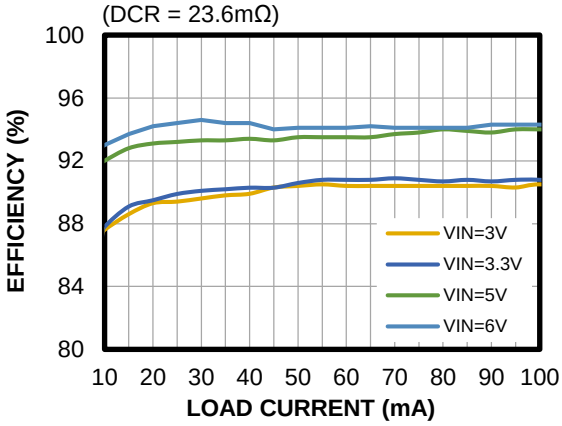
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 8V, f_{SW} = 2.6MHz, R_{FB1} = 100kΩ, R_{FB2} = 14.3kΩ, L = 1.5µH (DCR = 23.6mΩ)



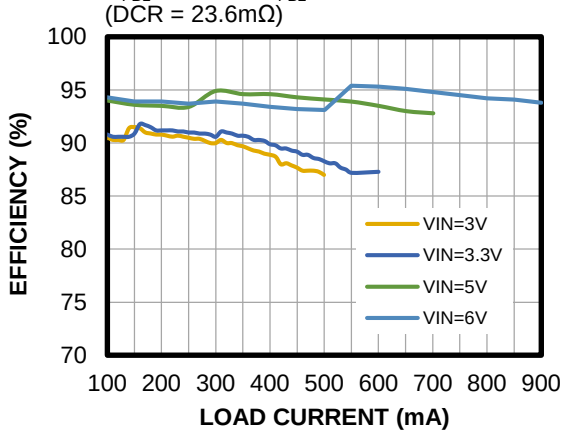
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 8V, f_{SW} = 2.6MHz, R_{FB1} = 100kΩ, R_{FB2} = 14.3kΩ, L = 1.5µH (DCR = 23.6mΩ)



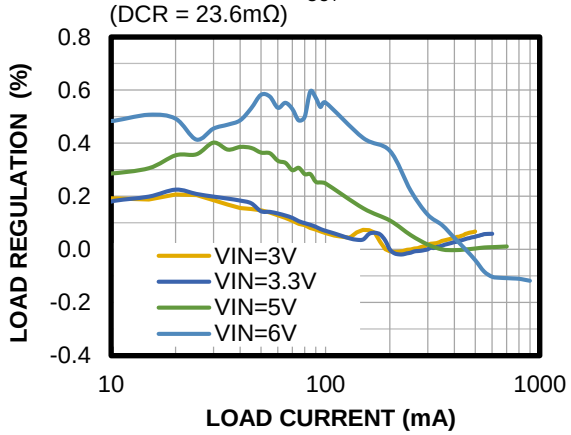
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 8V, f_{SW} = 2.6MHz, R_{FB1} = 100kΩ, R_{FB2} = 14.3kΩ, L = 1.5µH (DCR = 23.6mΩ)



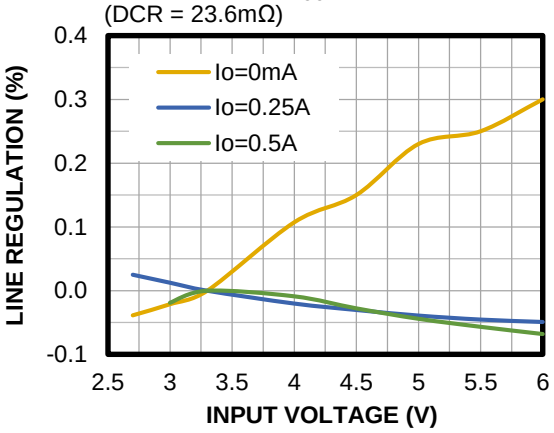
Load Regulation

MPQ3438-0000, V_{OUT} = 8V, L = 1.5µH (DCR = 23.6mΩ)



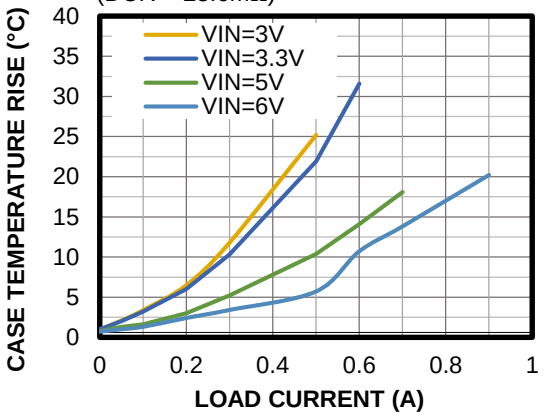
Line Regulation

MPQ3438-0000, V_{OUT} = 8V, L = 1.5µH (DCR = 23.6mΩ)



Case Temperature Rise

MPQ3438-0000, V_{OUT} = 8V, L = 1.5µH (DCR = 23.6mΩ)

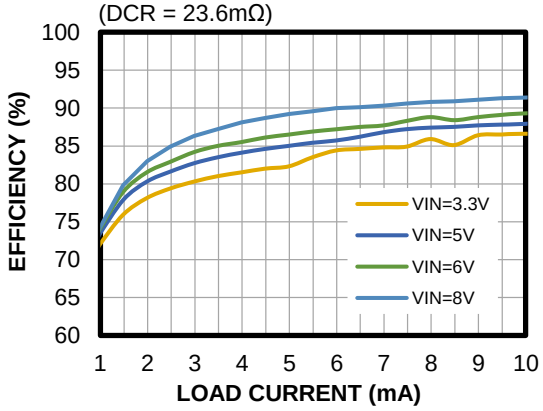


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0000, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

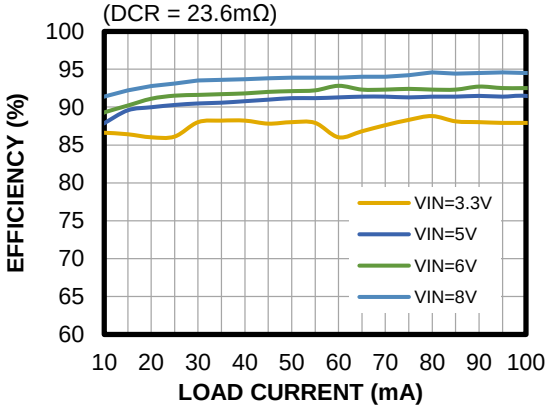
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH
(DCR = 23.6mΩ)



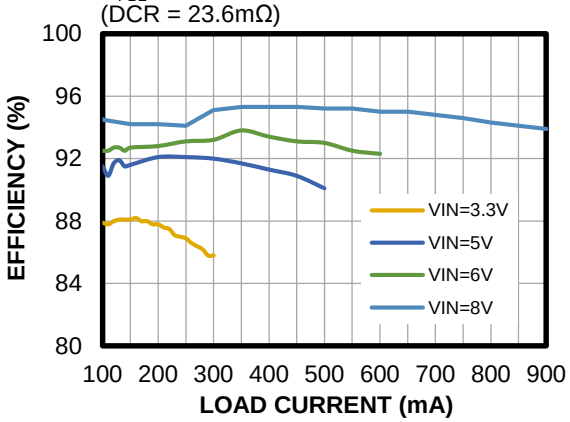
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH
(DCR = 23.6mΩ)



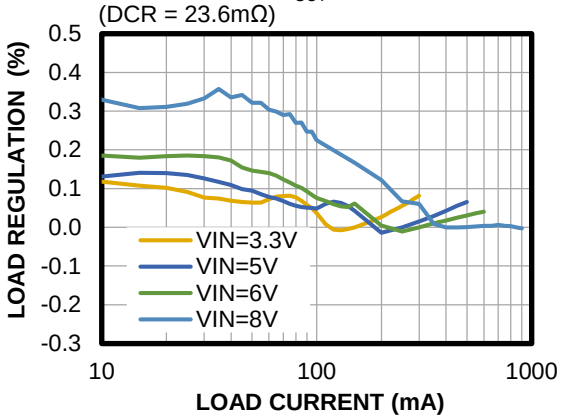
Efficiency vs. Load Current

MPQ3438-0000, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH
(DCR = 23.6mΩ)



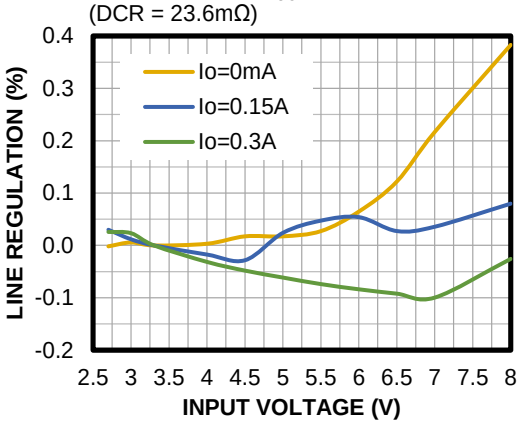
Load Regulation

MPQ3438-0000, V_{OUT} = 12V, L = 1.5µH
(DCR = 23.6mΩ)



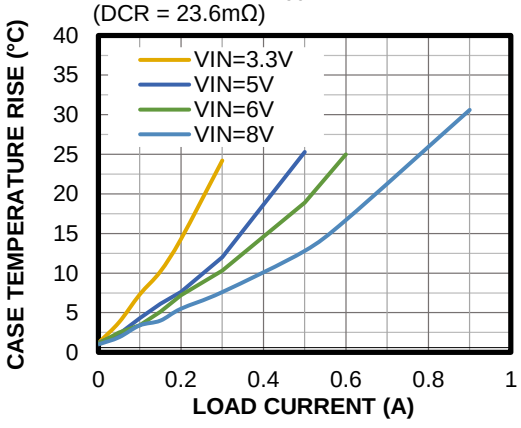
Line Regulation

MPQ3438-0000, V_{OUT} = 12V, L = 1.5µH
(DCR = 23.6mΩ)



Case Temperature Rise

MPQ3438-0000, V_{OUT} = 12V, L = 1.5µH
(DCR = 23.6mΩ)

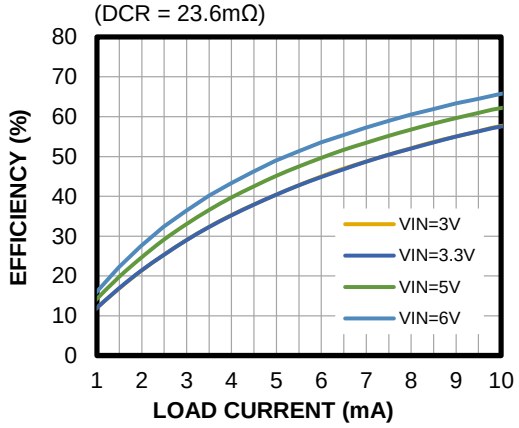


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0001, V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 500mA, T_A = 25°C, unless otherwise noted.

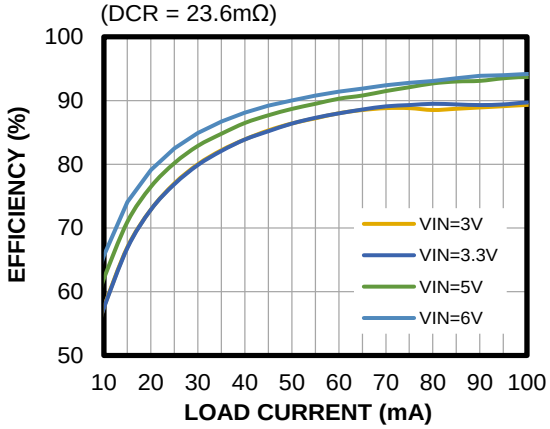
Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 8V, f_{SW} = 2.6MHz, R_{FB1} = 100kΩ, R_{FB2} = 14.3kΩ, L = 1.5µH (DCR = 23.6mΩ)



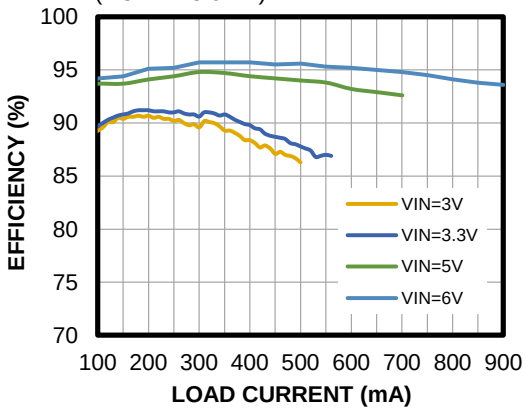
Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 8V, f_{SW} = 2.6MHz, R_{FB1} = 100kΩ, R_{FB2} = 14.3kΩ, L = 1.5µH (DCR = 23.6mΩ)



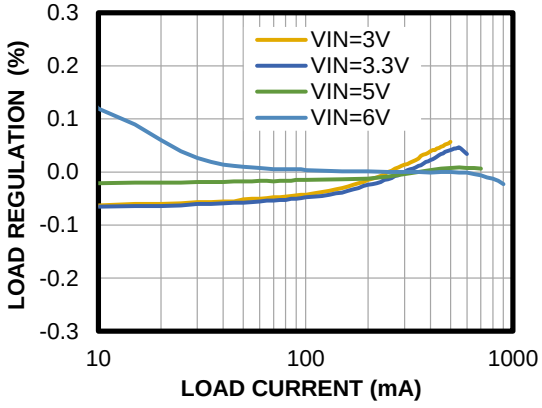
Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 8V, f_{SW} = 2.6MHz, R_{FB1} = 100kΩ, R_{FB2} = 14.3kΩ, L = 1.5µH (DCR = 23.6mΩ)



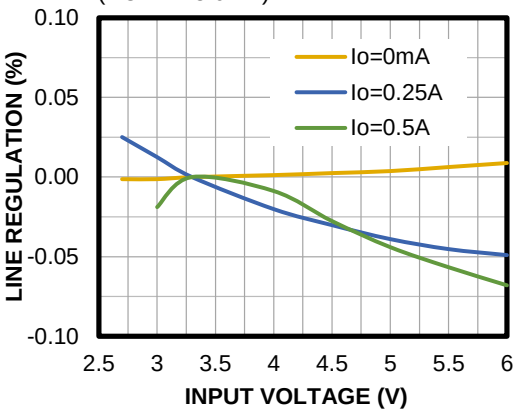
Load Regulation

MPQ3438-0001, V_{OUT} = 8V, L = 1.5µH (DCR = 23.6mΩ)



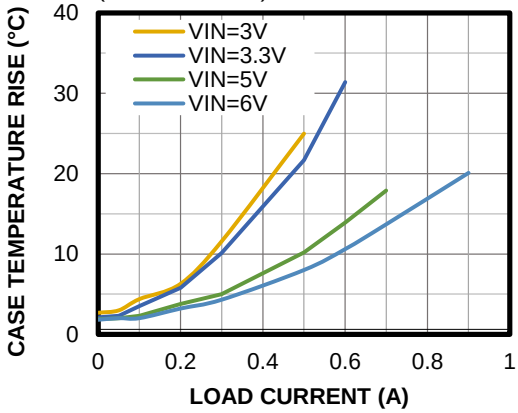
Line Regulation

MPQ3438-0001, V_{OUT} = 8V, L = 1.5µH (DCR = 23.6mΩ)



Case Temperature Rise

MPQ3438-0001, V_{OUT} = 8V, L = 1.5µH (DCR = 23.6mΩ)

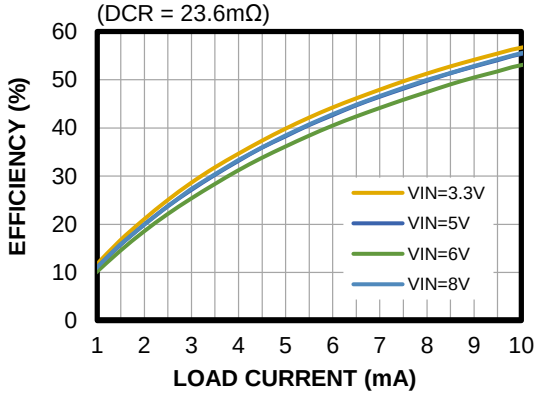


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0001, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

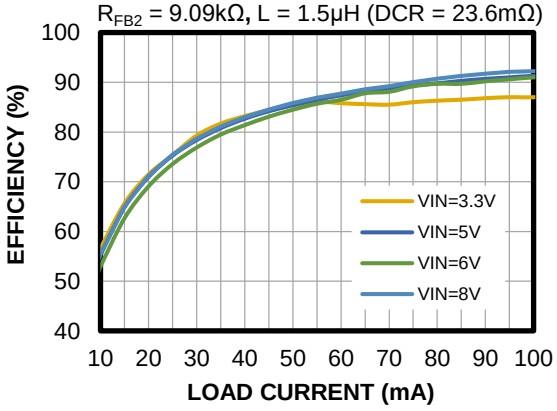
Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH
(DCR = 23.6mΩ)



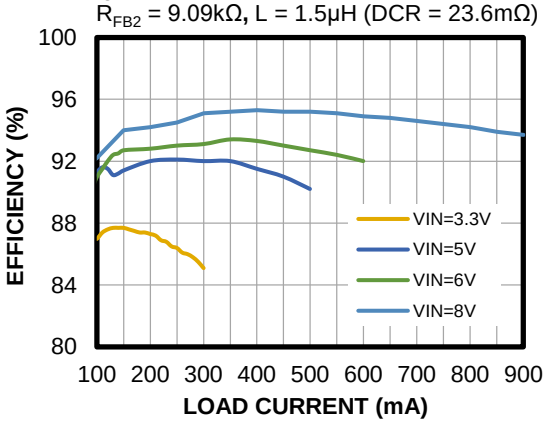
Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH (DCR = 23.6mΩ)



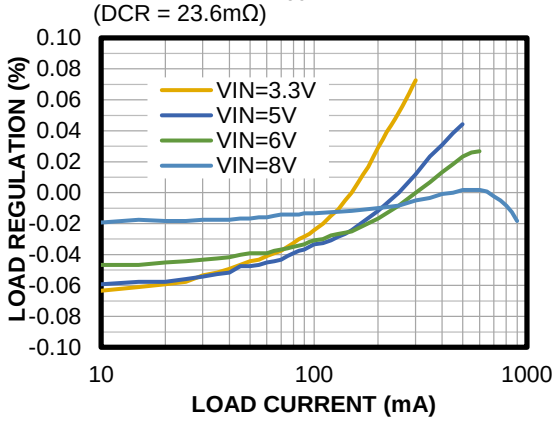
Efficiency vs. Load Current

MPQ3438-0001, V_{OUT} = 12V,
f_{SW} = 2.6MHz, R_{FB1} = 100kΩ,
R_{FB2} = 9.09kΩ, L = 1.5µH (DCR = 23.6mΩ)



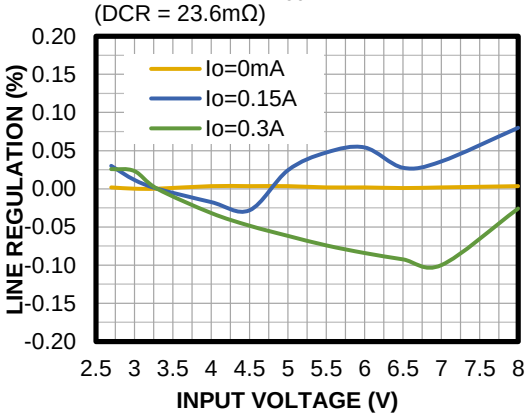
Load Regulation

MPQ3438-0001, V_{OUT} = 12V, L = 1.5µH
(DCR = 23.6mΩ)



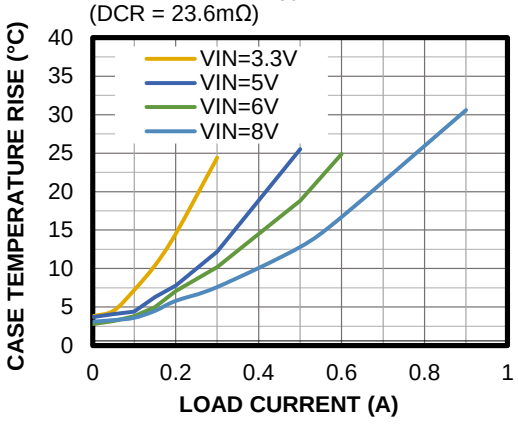
Line Regulation

MPQ3438-0001, V_{OUT} = 12V, L = 1.5µH
(DCR = 23.6mΩ)



Case Temperature Rise

MPQ3438-0001, V_{OUT} = 12V, L = 1.5µH
(DCR = 23.6mΩ)

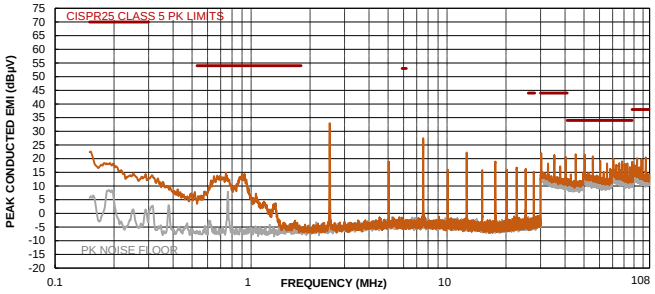


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 12V, L = 1.5µH (14), I_{OUT} = 500mA, T_A = 25°C, unless otherwise noted. (15)

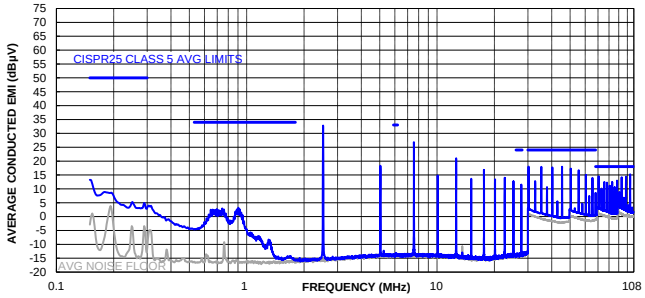
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



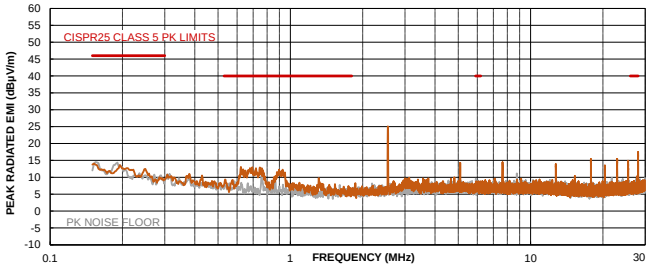
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



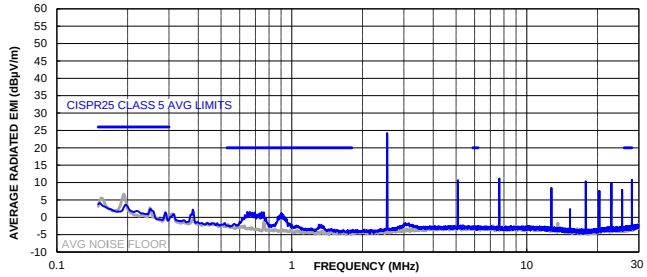
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



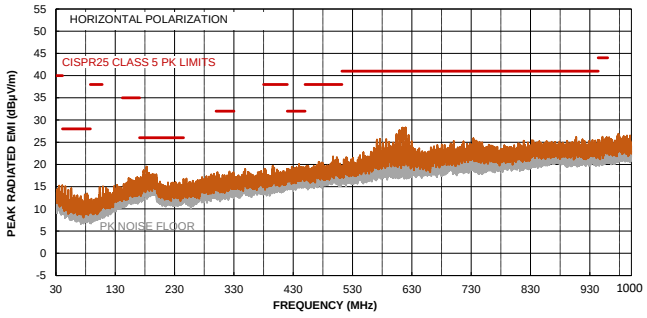
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



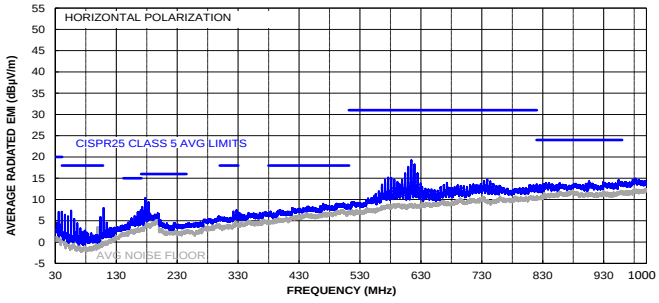
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

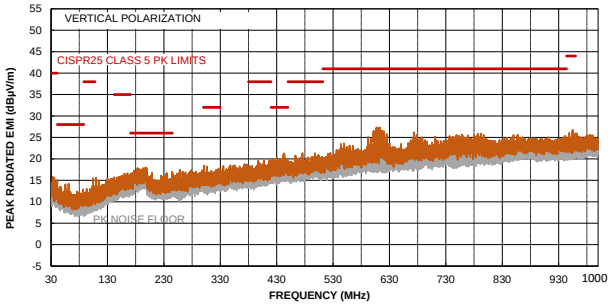


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 12V, L = 1.5µH (14), I_{OUT} = 500mA, T_A = 25°C, unless otherwise noted. (15)

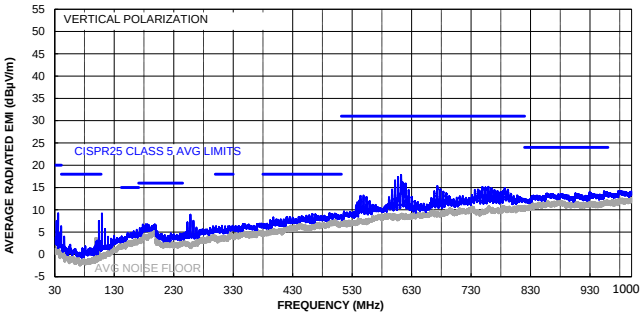
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

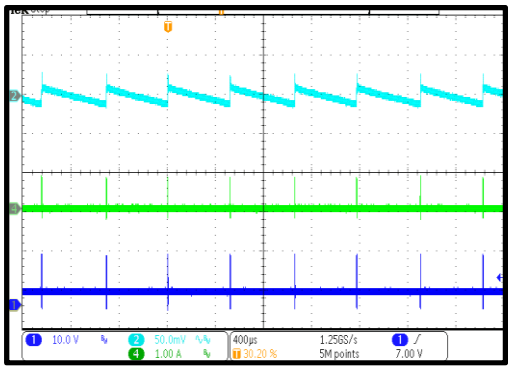
14) Inductor part number: VCTA25201B-1R5MS6. DCR = 50mΩ.
15) The EMC test results are based on the typical application circuit with EMI filters (see Figure 7 on page 31).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0000, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

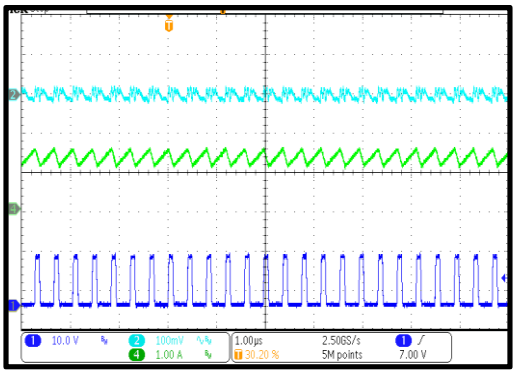
Steady State

I_{OUT} = 0A



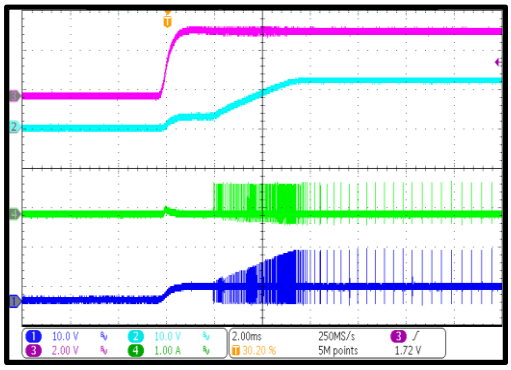
Steady State

I_{OUT} = 0.3A



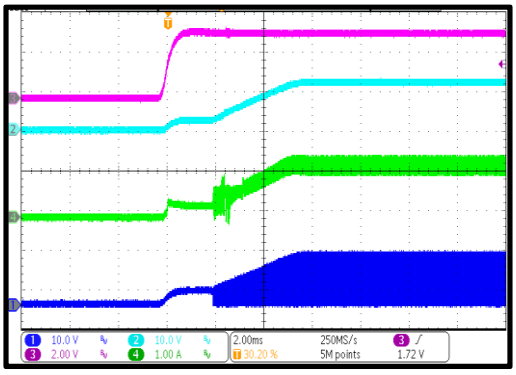
Start-Up through VIN

I_{OUT} = 0A



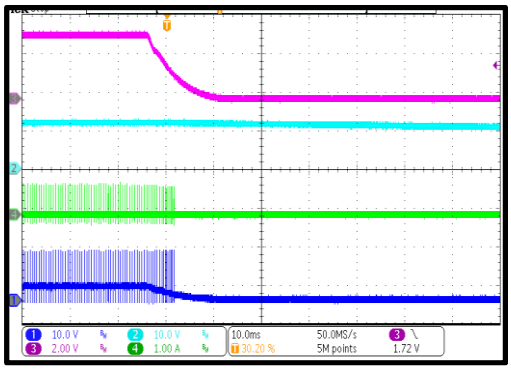
Start-Up through VIN

I_{OUT} = 0.3A



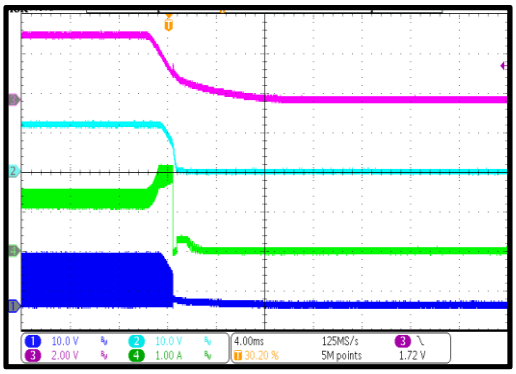
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 0.3A

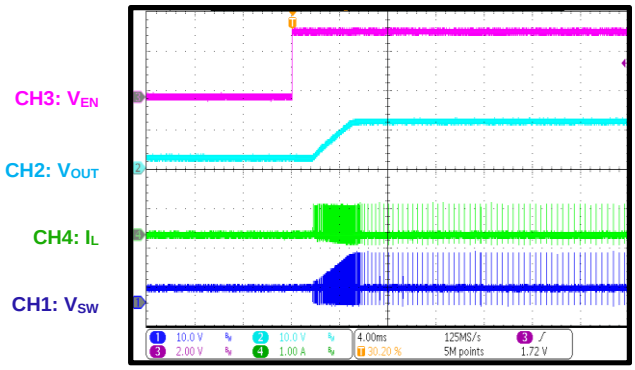


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0000, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

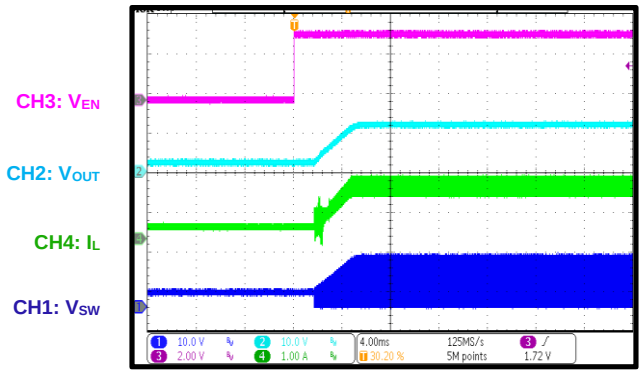
Start-Up through EN

I_{OUT} = 0A, AAM mode



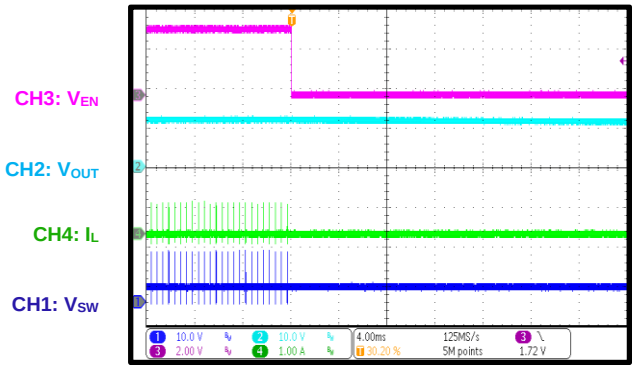
Start-Up through EN

I_{OUT} = 0.3A



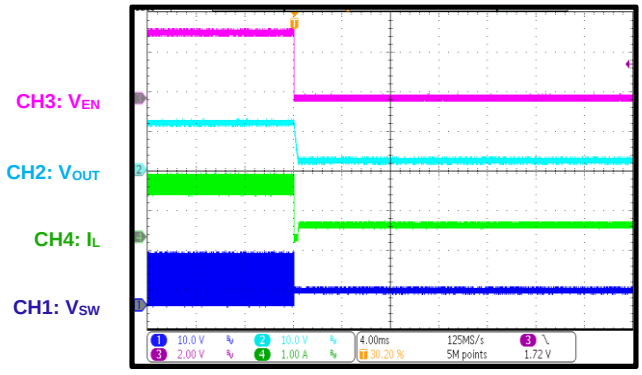
Shutdown through EN

I_{OUT} = 0A



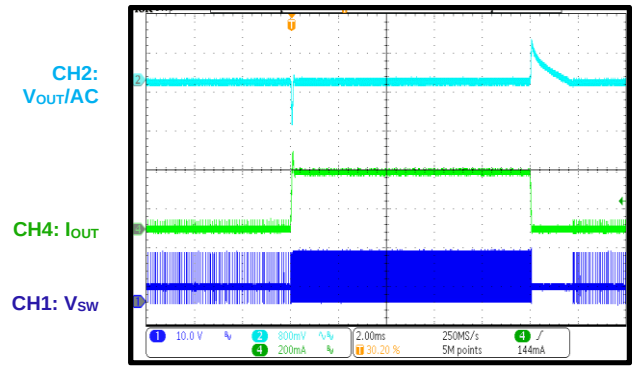
Shutdown through EN

I_{OUT} = 0.3A



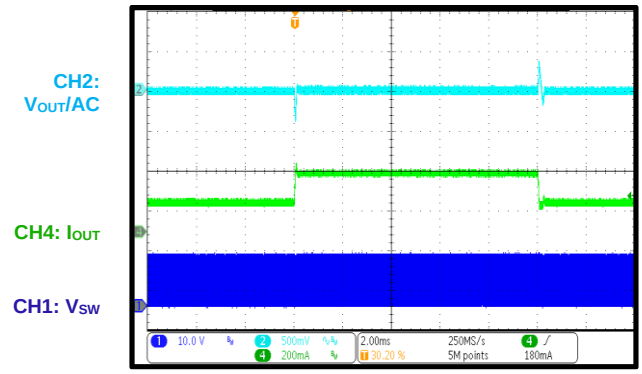
Load Transient

I_{OUT} = 0A to 0.3A, 1.6A/µs



Load Transient

I_{OUT} = 0.15A to 0.3A, 1.6A/µs

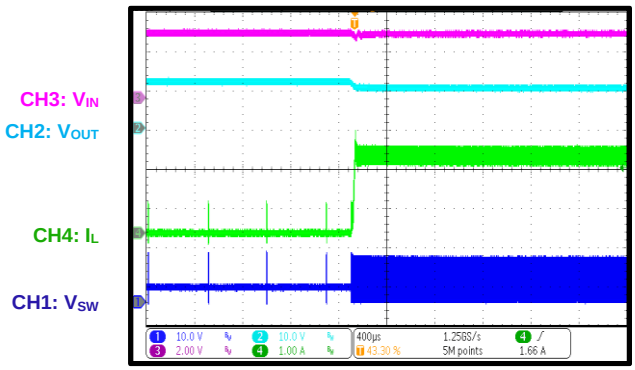


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0000, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

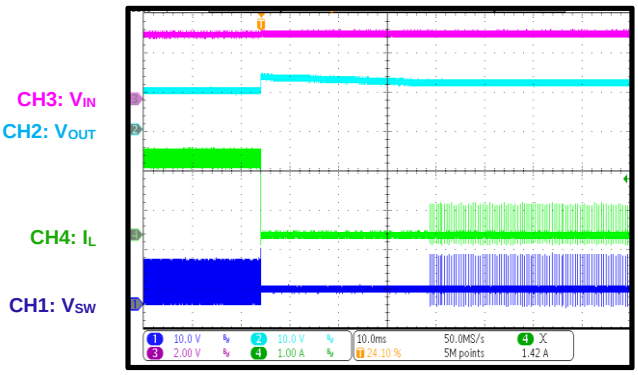
OCP Entry

Increase the load current to the overload threshold



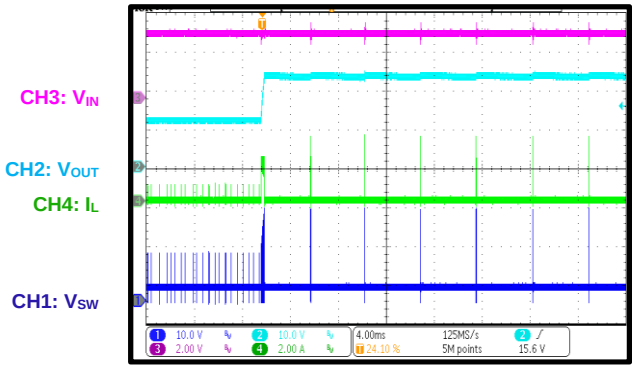
OCP Recovery

Decrease the load current to 0A



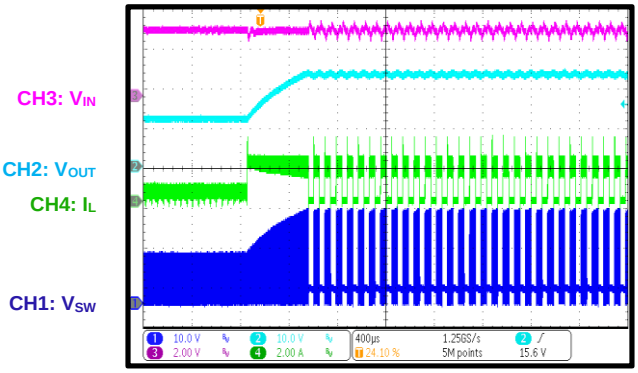
OVP Entry

I_{OUT} = 0A



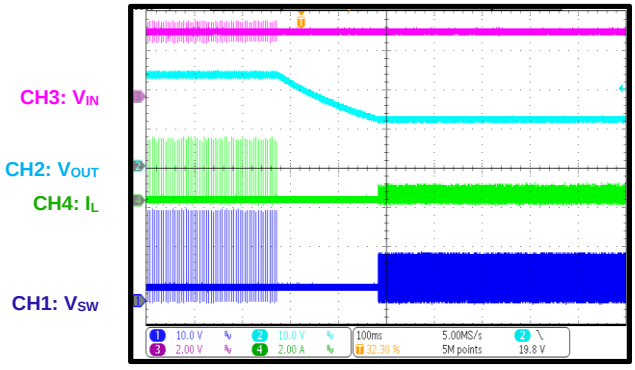
OVP Entry

I_{OUT} = 0.1A



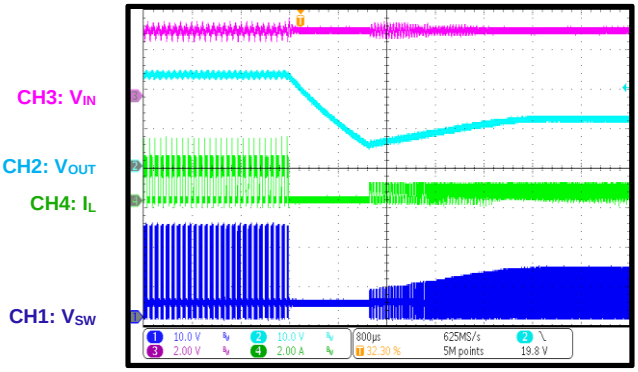
OVP Recovery

I_{OUT} = 0A



OVP Recovery

I_{OUT} = 0.1A

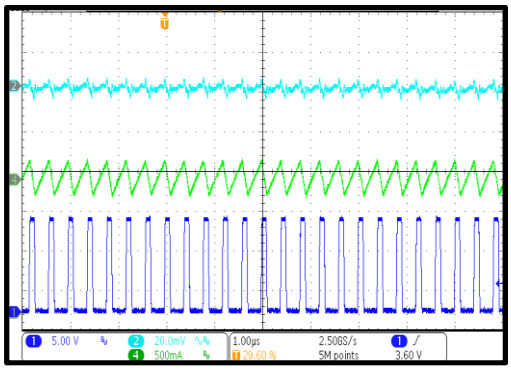


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0001, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

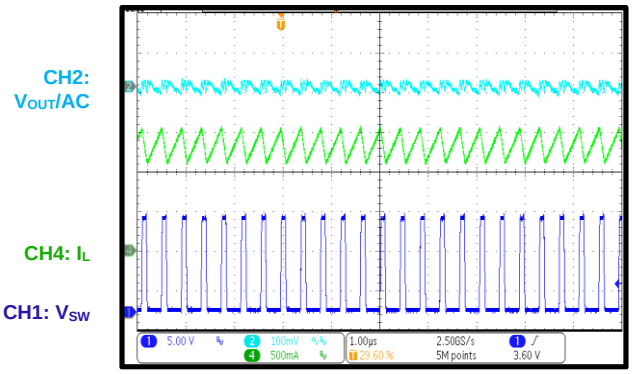
Steady State

I_{OUT} = 0A



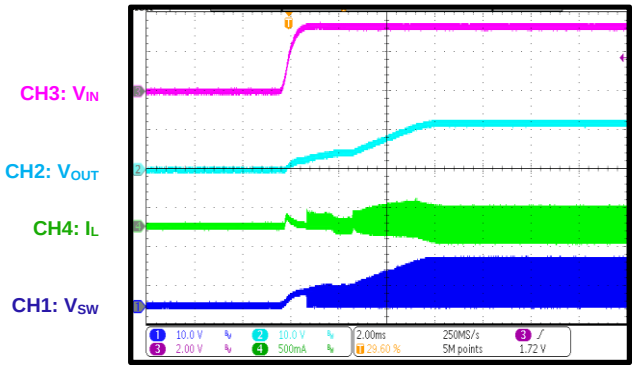
Steady State

I_{OUT} = 0.3A



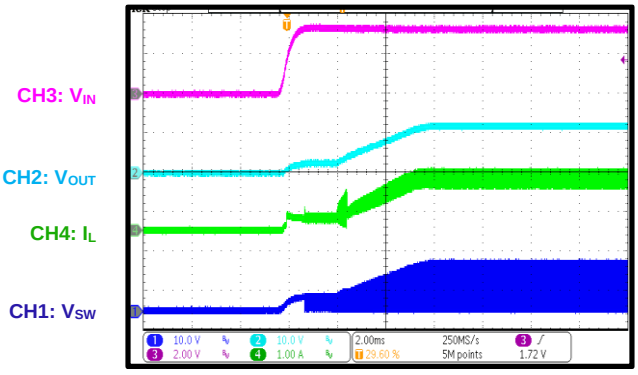
Start-Up through VIN

I_{OUT} = 0A



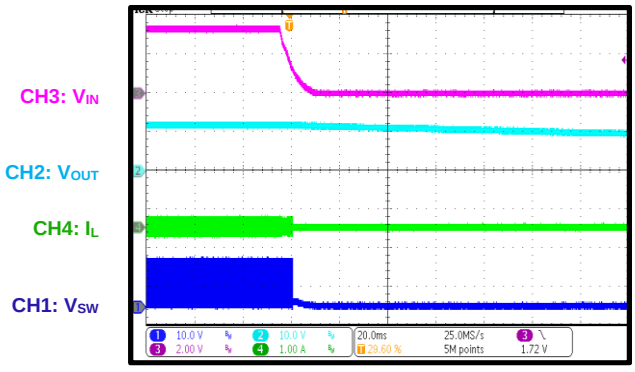
Start-Up through VIN

I_{OUT} = 0.3A



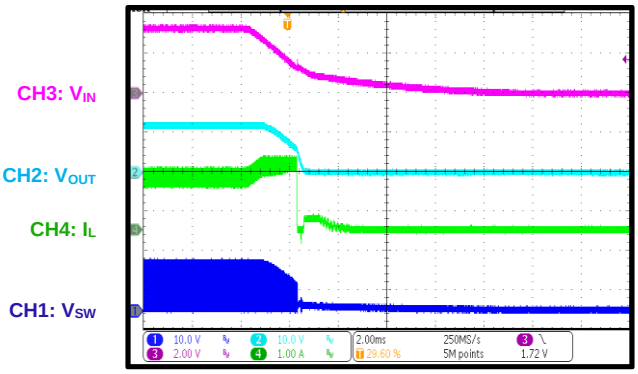
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 0.3A

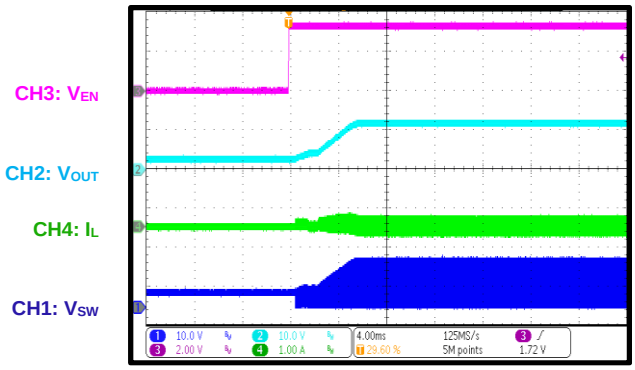


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0001, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

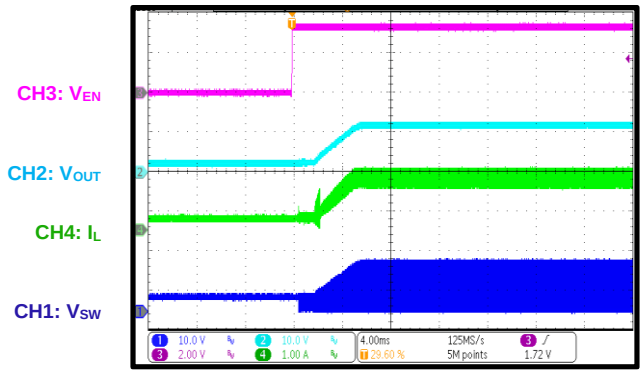
Start-Up through EN

I_{OUT} = 0A, AAM mode



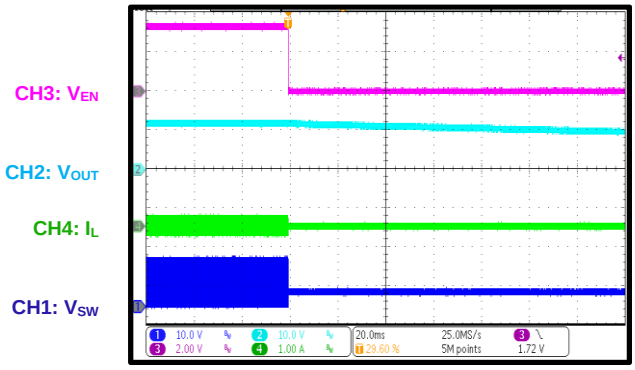
Start-Up through EN

I_{OUT} = 0.3A



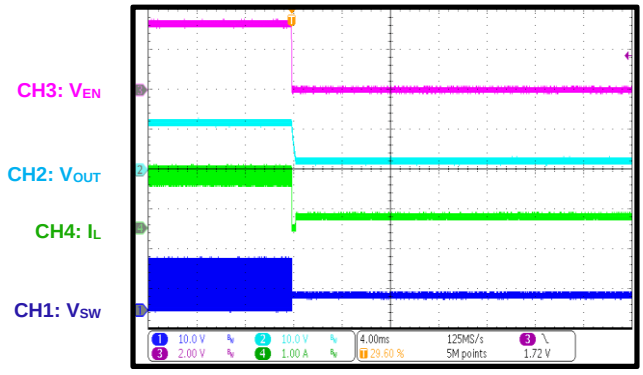
Shutdown through EN

I_{OUT} = 0A



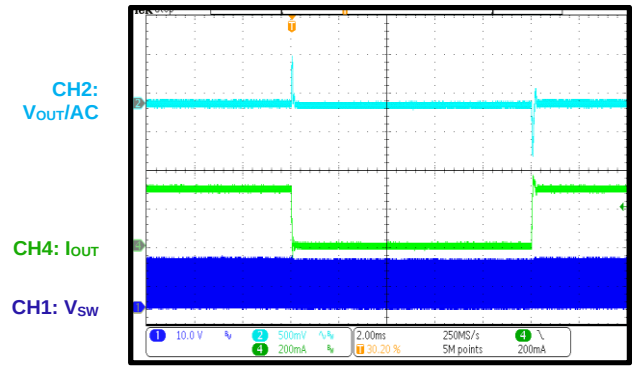
Shutdown through EN

I_{OUT} = 0.3A



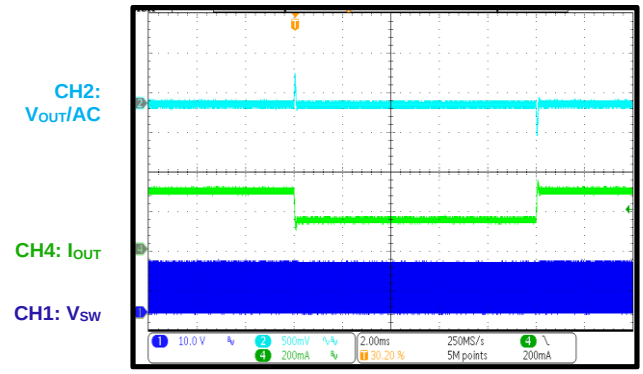
Load Transient

I_{OUT} = 0A to 0.3A, 1.6A/µs



Load Transient

I_{OUT} = 0.15A to 0.3A, 1.6A/µs

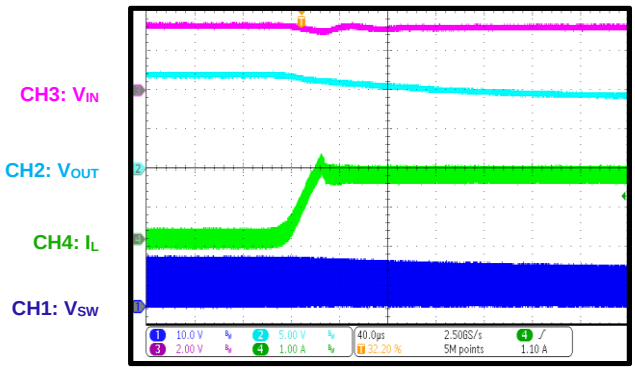


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ3438-0001, V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 300mA, T_A = 25°C, unless otherwise noted.

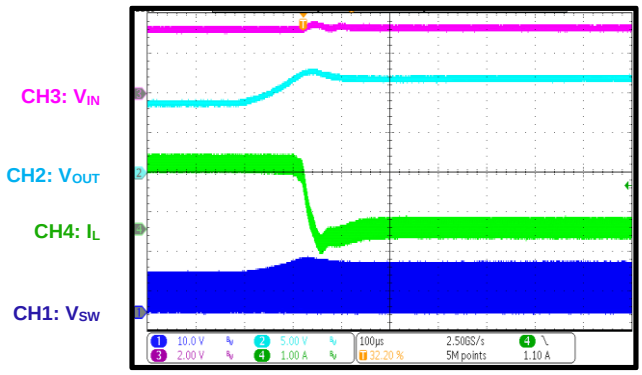
OCP Entry

Increase the load current to the overload threshold



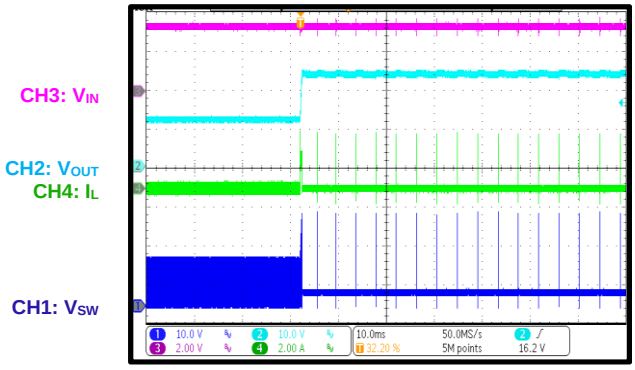
OCP Recovery

Decrease the load current to 0A



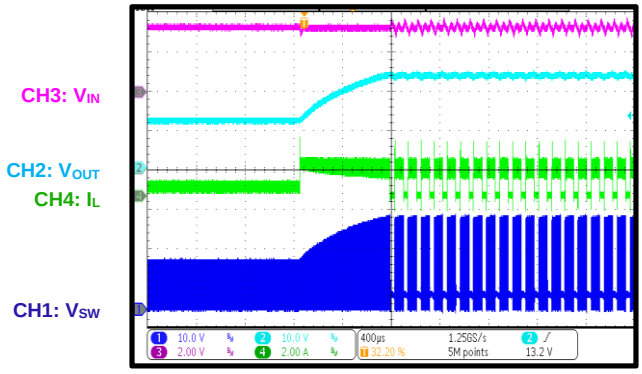
OVP Entry

I_{OUT} = 0A



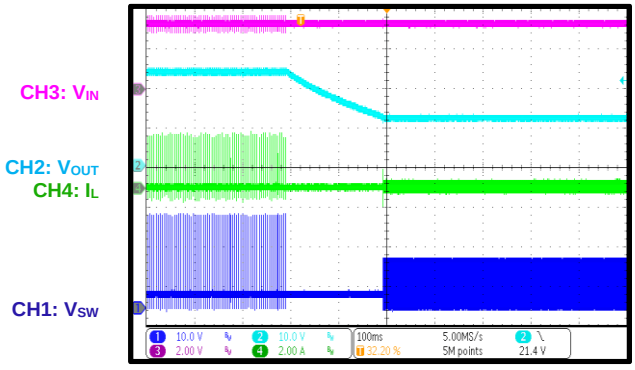
OVP Entry

I_{OUT} = 0.1A



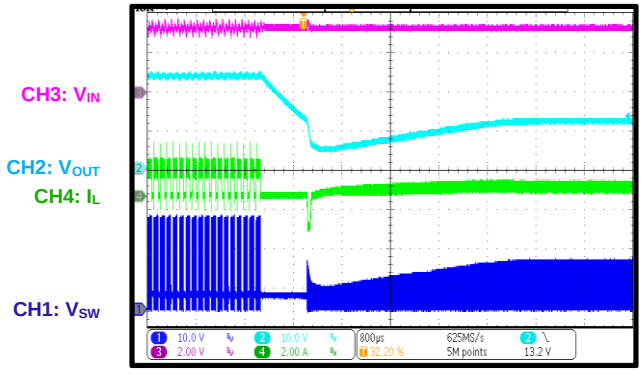
OVP Recovery

I_{OUT} = 0A



OVP Recovery

I_{OUT} = 0.1A



FUNCTIONAL BLOCK DIAGRAM

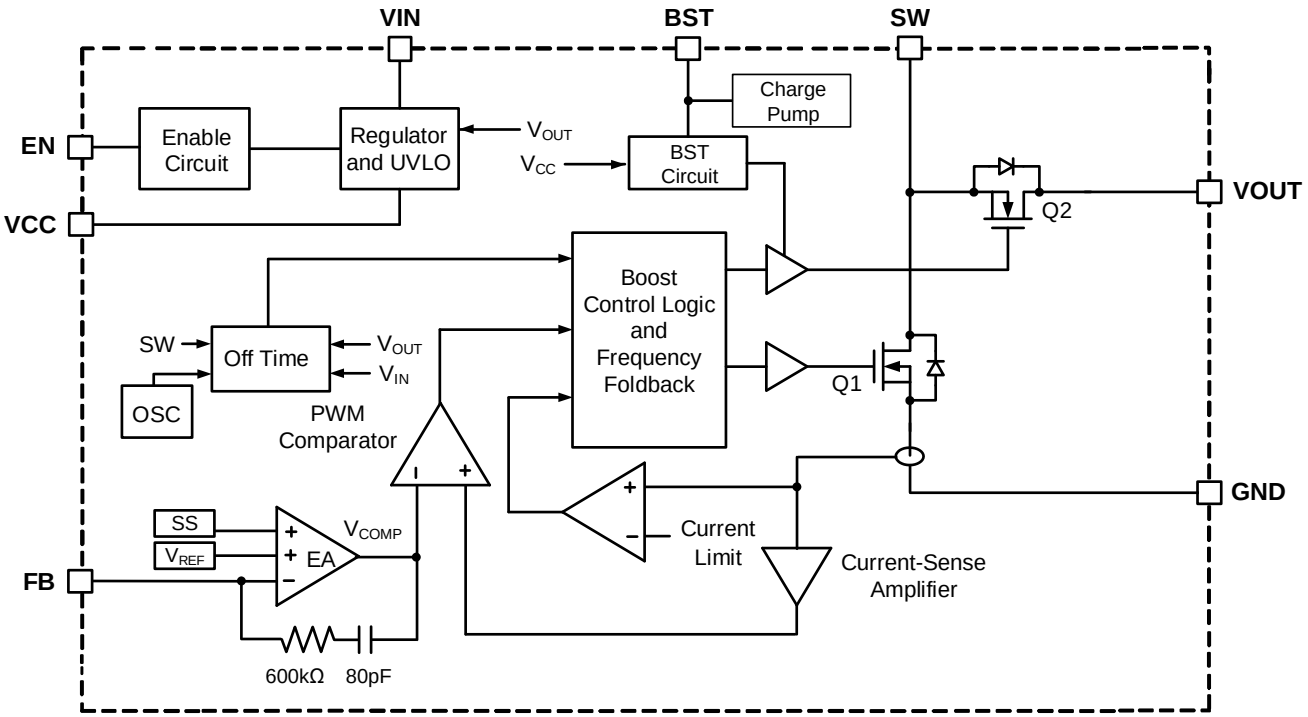


Figure 1: Functional Block Diagram

OPERATION

The MPQ3438 is a 2.6MHz, quasi-fixed frequency, high-efficiency boost converter with a wide input voltage (V_{IN}) range. Its fully integrated MOSFETs provide small size and high efficiency for voltage step-up applications. Adaptive constant-off-time (COT) control provides fast transient response. Figure 1 on page 23 shows the functional block diagram.

Boost Operation

The MPQ3438 uses COT control to regulate the output voltage (V_{OUT}). At the beginning of each cycle, the low-side N-channel MOSFET (LS-FET) (Q1) turns on and forces the inductor current (I_L) to rise.

The device senses the current through the LS-FET. If the current signal exceeds the COMP voltage (V_{COMP}), where COMP is an amplifier output comparing the FB voltage (V_{FB}) to the internal reference. Then the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. I_L flows to the output capacitor (C_{OUT}) through the high-side MOSFET (HS-FET) and decreases.

After a fixed off time, the LS-FET turns on again and the cycle repeats. During each cycle, the LS-FET off time is determined by the V_{IN} / V_{OUT} ratio, and the on time is controlled by V_{COMP}. The peak I_L is controlled by COMP, and COMP is controlled by the output voltage (V_{OUT}). Therefore, I_L regulates V_{OUT}.

Power-Save Mode (PSM) at Light Loads

The MPQ3438-0000 works in power-save mode (PSM) under light-load conditions. Once I_L drops to 0A, the HS-FET turns off to stop the current flowing from VOUT to VIN, and I_L is forced to work in discontinuous conduction mode (DCM). At the same time, the internal off time becomes longer when the MPQ3438-0000 enters DCM. The off-time is inversely proportional to the HS-FET on time in each cycle. In DCM conditions, the MPQ3438 slows down the switching frequency (f_{SW}) and reduces power loss.

If V_{COMP} drops to the PSM threshold, the MPQ3438 stops switching to further reduce switching power loss. Switching resumes once V_{COMP} exceeds the PSM threshold. The switching pulse skips based on V_{COMP} under extreme light-load conditions.

In DCM, the frequency is low, and the LS-FET does not turn on during the prolonged off time. If the load increases and V_{COMP} increases, the off time shortens, and the MPQ3438 returns to the 2.6MHz fixed frequency. The loop can then respond to higher load currents.

Forced Continuous Conduction Mode (FCCM)

The MPQ3438-0001 works in fixed-frequency PWM mode under all load conditions. In this mode, the off time is determined by the internal circuit to achieve the 2.6MHz frequency based on the V_{IN} / V_{OUT} ratio.

When the load decreases, the average input current drops, and I_L may become negative during the off time (while the LS-FET is off and the HS-FET is on). This forces I_L to work in forced continuous conduction mode (FCCM) with a fixed frequency, and generates a lower V_{OUT} ripple than in PSM.

VCC Power

The MPQ3438's internal circuit is powered by VCC. A minimum 1µF ceramic capacitor must be placed on VCC. When V_{IN} is below 3.4V, VCC is powered by the higher voltage between V_{IN} and V_{OUT}. This allows the MPQ3438 to maintain a low on resistance ($R_{DS(ON)}$) and high efficiency, even with low V_{IN}. When V_{IN} exceeds 3.4V, VCC is always powered by V_{IN}. This reduces V_{OUT} to the VCC regulator loss.

If VCC is powered by an external supply and the voltage exceeds 3.4V, the regulators from VIN and VOUT are disabled. Under this condition, the MPQ3438 starts up once the external VCC power supply exceeds the V_{CC} under-voltage lockout (UVLO) threshold (V_{CC_UVLO}), even if V_{IN} is as low as 0.9V. When VCC is powered by the external power supply, the MPQ3438 continues working if V_{IN} and V_{OUT} are dropping but still exceed 0.8V. The external VCC power source should be limited within 3.6V.

There is a reverse-blocking circuit to limit the current flowing between VIN and VOUT. If the external VCC power supply exceeds the VCC regulation voltage, the current is supplied by the external power, and there is no path for current from VCC to VIN, or from VCC to VOUT.

VCC is charged when V_{IN} exceeds 0.9V and EN exceeds the micro-power threshold. If EN is low, VCC is disconnected from VIN and VOUT. Supply VIN with a power source exceeding 2.7V during V_{IN} start-up to provide VCC with sufficient power.

Start-Up

When the MPQ3438's input starts up and EN is high, the MPQ3438 starts charging VCC from V_{IN}. Once V_{CC} exceeds V_{CC_UVLO}, the MPQ3438 starts switching with closed-loop control. If VCC is powered by an additional supply, the MPQ3438 starts switching once V_{CC} exceeds its UVLO rising threshold ($V_{CC\_UVLO\_RISING}$).

After the IC is enabled, the MPQ3438 starts up with soft-start (SS) control. The SS signal is controlled by charging the SS pin from 0V and comparing this internal signal with the internal reference voltage (V_{REF}). The lower of the two values is applied to the error amplifier (EA) to control V_{OUT}.

If V_{OUT} is below 1.25 x V_{IN}, the operating frequency is folded back to prevent current spikes and provide smooth start-up control. Once V_{OUT} exceeds 1.25 x V_{IN}, the operating frequency returns to the nominal 2.6MHz.

When V_{OUT} reaches its target value, the SS signal exceeds V_{REF}, and SS completes. The internal V_{REF} takes charge of the feedback loop regulation. Internal SS quickly pulls low after the IC shuts down during UVLO or under conditions when the protections are disabled.

If there is a biased voltage on VOUT, the MPQ3438 does not switch until the SS signal exceeds V_{FB} which is proportional to the VOUT biased voltage.

Synchronous Rectifier and Bootstrap (BST) Function

The MPQ3438 integrates both an LS-FET (Q1) and HS-FET (Q2) to reduce the external component count. During switching, the rectifier switch (Q2) is powered by the BST pin voltage (V_{BST}) (typically 3.2V above the SW voltage). This 3.2V V_{BST} is charged from VCC when the LS-FET turns on.

Switching Current Limit

The MPQ3438 provides a fixed, cycle-by-cycle, switching peak current limit. In each cycle, the internal current-sense circuit monitors the LS-FET's current signal. Once the sensed current reaches the current limit, the LS-FET (Q1) turns off. The LS-FET current signal is internally blanked for about 80ns to enhance noise immunity.

Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

The EN pin enables and disables the MPQ3438. When applying a voltage to EN exceeding its high threshold (1V max), the MPQ3438 starts up some of the internal circuits in micro-power mode. If the EN voltage (V_{EN}) exceeds the turn-on threshold (1.2V), the MPQ3438 enables all functions and starts boost operation.

Boost switching is disabled when V_{EN} drops below its 1.2V turn-on threshold. To completely shut down the MPQ3438, EN must have a low-level voltage below 0.4V. After shutdown, the MPQ3438 sinks a current from the input power (typically below 1μA). EN is compatible with voltages up to 16V. For automatic start-up, connect EN directly to VIN.

The MPQ3438 features a configurable UVLO hysteresis. When starting up in micro-power mode, EN sinks a 5μA current via an upper resistor (R_{TOP}) (see Figure 2).

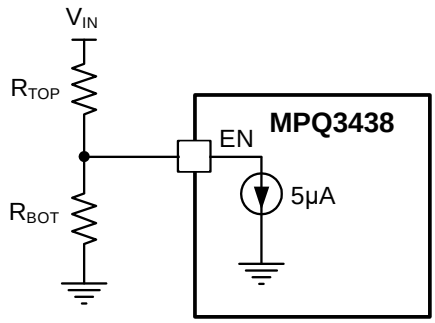


Figure 2: V_{IN} UVLO Configuration

V_{IN} must increase to overcome the current sink. The V_{IN} start-up threshold (V_{IN_ON}) can be calculated with Equation (1):

$$V_{IN\_ON} = V_{EN\_ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (1)$$

Where V_{EN_ON} is the EN voltage turn-on threshold (typically 1.2V).

Once V_{EN} reaches V_{EN_ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold ($V_{IN\_UVLO\_HYS}$), which can be calculated with Equation (2):

$$V_{IN\_UVLO\_HYS} = 5\mu A \times R_{TOP} \quad (2)$$

Over-Voltage Protection (OVP)

If the device detects that V_{OUT} exceeds its 24V threshold, the MPQ3438 immediately stops switching until V_{OUT} drops to 23.5V. This prevents an over-voltage (OV) condition on the output and internal power MOSFETs.

The MPQ3438 also supports FB over-voltage protection (OVP). Once V_{FB} exceeds 110% of V_{REF}, the MPQ3438 turns off the LS-FET and does not recover until V_{FB} drops below 105% of V_{REF}.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. When the die temperature exceeds 165°C, the IC shuts down. Once the die temperature drops to 140°C, the device resumes normal operation.

APPLICATION INFORMATION

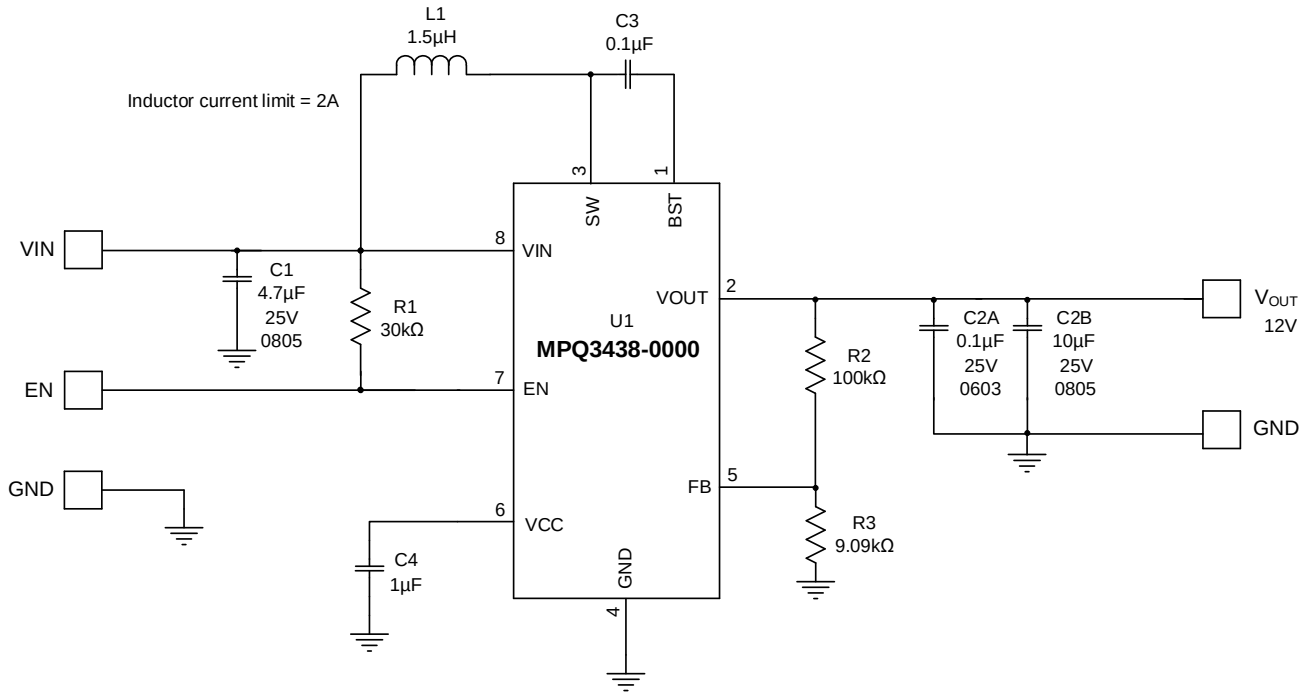


Figure 3: Typical Application Circuit for the MPQ3438-0000-AEC1 (V_{OUT} = 12V)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Value	Design Guide Index
1	BST	C3	0.1µF	Bootstrap (BST) Capacitor (BST, Pin 1)
2	VOUT	C2A, C2B	0.1µF, 10µF	Setting the Output Voltage (VOUT, Pin 2)
3	SW	L1	1.5µH	Selecting the Inductor (SW, Pin 3)
4	GND	-	-	Ground Connection (GND, Pin 4)
5	FB	R2, R3	100kΩ, 9.09kΩ	Feedback Divider (FB, Pin 5)
6	VCC	C4	1µF	Selecting the VCC Capacitor (VCC, Pin 6)
7	EN	R1	30kΩ	Chip Enable Control (EN, Pin 7)
8	VIN	C1	4.7µF	Selecting the Input Capacitors (VIN, Pin 8)

Bootstrap (BST) Capacitor (BST, Pin 1)

The MPQ3438 uses a bootstrap (BST) circuit to power the output N-channel MOSFET. An external BST capacitor (C_{BST}) is required for the charge pump power. It is recommended to place a 0.1µF ceramic capacitor between the BST and SW pins.

Setting the Output Voltage (VOUT, Pin 2)

The external resistor divider sets V_{OUT}. The FB resistor (R2) must consider stability and dynamic response. If R2 is typically 100kΩ, then R3 can be calculated with Equation (3):

$$R3 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R2 \quad (3)$$

Where V_{REF} is 1V.

The set V_{OUT} must exceed V_{IN} by 1.25 times. Otherwise, V_{OUT} is not suitable for applications.

Selecting the Inductor (SW, Pin 3)

An inductor is required to transfer the energy between the input source and the output capacitors. A larger-value inductor results in reduced ripple current and peak I_L, which decreases stress on the power MOSFET. However, the larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

For most designs, the inductance (L) can be calculated with Equation (4):

$$L = \frac{V_{IN}\left(V_{OUT} - V_{IN}\right)}{f_{SW} \times V_{OUT} \times \Delta I_L} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be about 20% to 50% of the maximum average I_L. Ensure that the inductor does not saturate under worst-case conditions. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

Ground Connection (GND, Pin 4)

See the PCB Layout Guidelines section on page 30 for more details.

Feedback Divider (FB, Pin 5)

For the adjustable-output version, V_{FB} is typically 1V. The external resistor divider connected to FB sets V_{OUT} (see Figure 4).

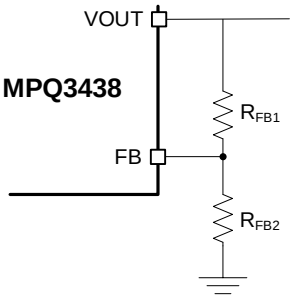


Figure 4: Feedback Divider Network for Adjustable Output

Table 2 lists the recommended feedback resistor values for common V_{OUT} values.

Table 2: Feedback Resistor Selection for Adjustable Output Version

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
8	100 (1%)	14.3 (1%)
12	100 (1%)	9.09 (1%)
16	100 (1%)	6.65 (1%)

Selecting the VCC Capacitor (VCC, Pin 6)

The MPQ3438 integrates the VCC power at about 3.4V to power the internal MOSFET gate driver and internal control circuit. A minimum 1µF ceramic bypass capacitor is required for the internal regulator. Do not connect the external load to the VCC power.

Chip Enable Control (EN, Pin 7)

The EN pin is a digital control pin that turns the device on and off.

Enabled by an External Logic High/Low Signal

EN must be externally pulled up or pulled down. Pull EN above the specified threshold (1.2V) to initiate boost operation. Pull EN below 0.4V to shut down the device.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Threshold

EN can configure the V_{IN} UVLO threshold (see Figure 2 on page 25). For automatic start-up, typically connect EN via a 30kΩ R_{TOP} to achieve a hysteresis of 150mV.

Selecting the Input Capacitors (VIN, Pin 8)

The input capacitor (C1) maintains the DC V_{IN}. Low-ESR ceramic capacitors are recommended. The input voltage ripple (ΔV_{IN}) can be calculated with Equation (5) on page 29:

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^{2} \times L \times C1} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (5)$$

Selecting the Output Capacitors

The output current (I_{OUT}) to the boost converter is discontinuous, and therefore requires an output capacitor (C2) to supply AC current to the load. For the best performance, low-ESR ceramic capacitors are recommended. The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times R_L \times C2} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (6)$$

Where R_L is the load resistance.

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low-ESR and small-temperature coefficients.

Input Start-Up Inrush Current Control

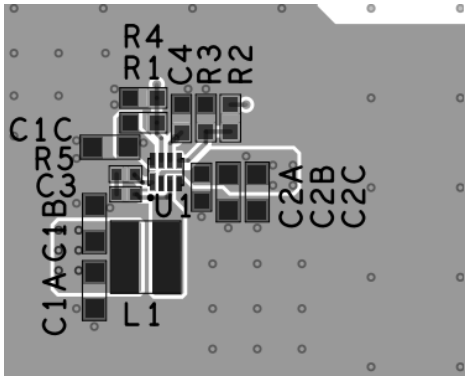
During input start-up, the inrush current through the HS-FET body diode should be limited to be below 30A. If the start-up inrush current exceeds 30A during the board evaluation, the system must be optimized. There are two possible approaches to optimize the system:

1. Reduce the start-up initial V_{IN}, or reduce the V_{IN} start-up slew rate.
2. Reduce the large output capacitor volume, or add a MOSFET between the MPQ3438's C_{OUT} and bulk capacitor to smoothly charge up the bulk capacitor.

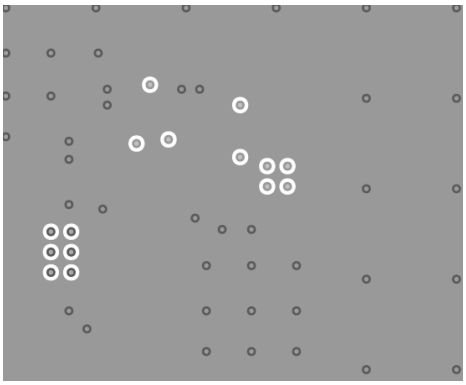
PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 5 and follow the steps below:

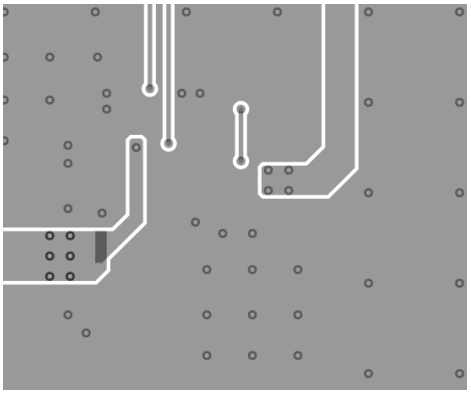
1. Place the output capacitors (C2A and C2B) as close to VOUT and GND as possible.
2. It is highly recommended to place a 0.1µF capacitor (C2A) close to the IC to reduce parasitic inductance.
3. Keep a short and wide connection between VOUT and GND to the output capacitor (C2A) using copper.
4. Place the copper, IC, and output capacitor (C2A) on the same layer.
5. Place the FB dividers (R2 and R3) as close to FB as possible.
6. Keep the FB trace far away from noise sources, such as the SW node.
7. Connect the VCC capacitor (C_{VCC}) to GND using a short loop.
8. Keep the input loop (C1A, L1, SW, and GND) as small as possible.
9. Place enough GND vias close to the MPQ3438 to achieve good thermal dissipation.



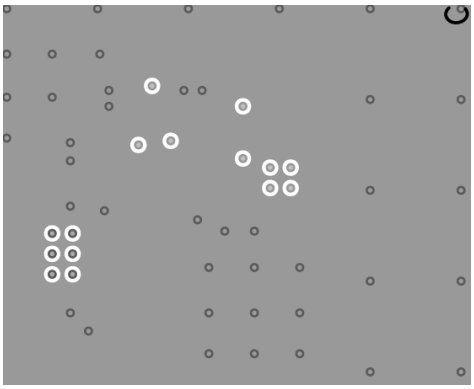
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

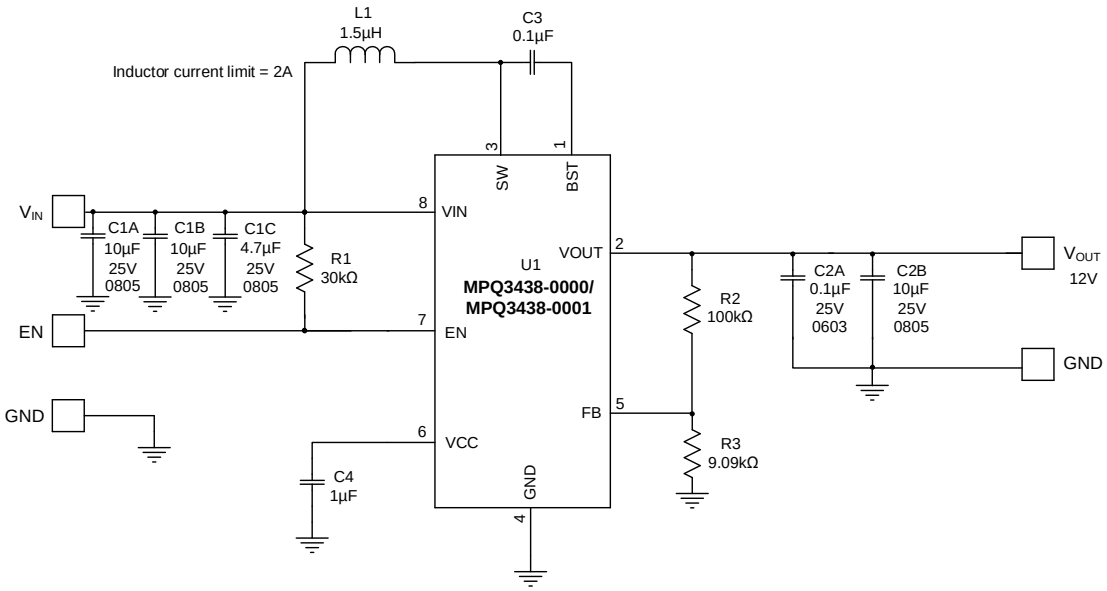


Figure 6: Typical Application Circuit (12V Output)

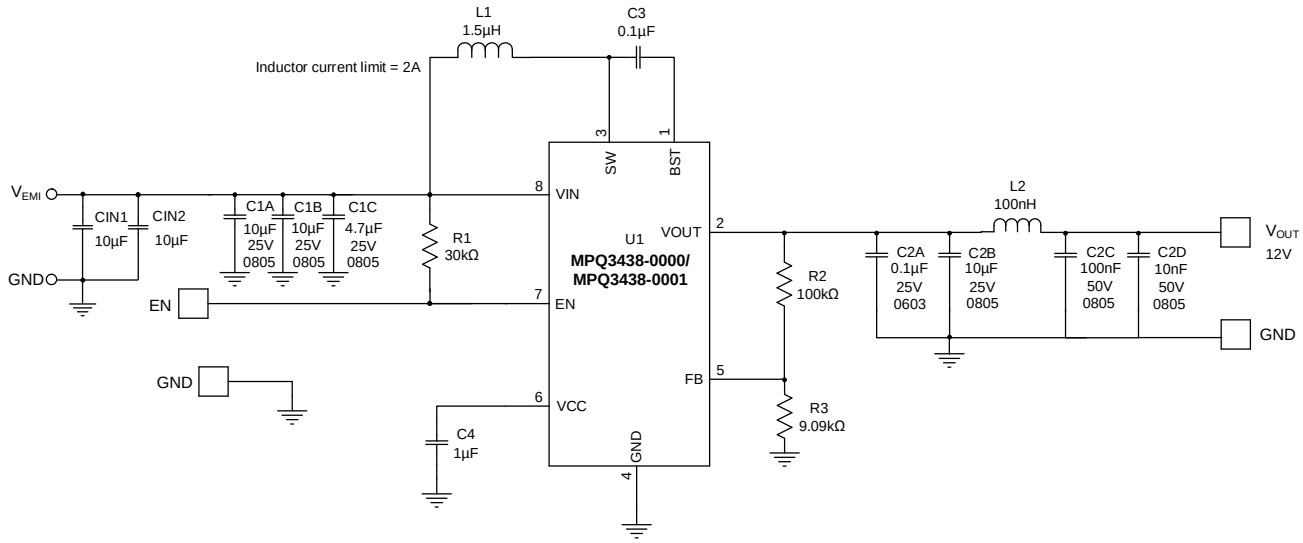
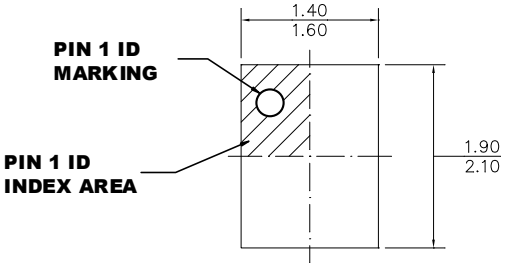


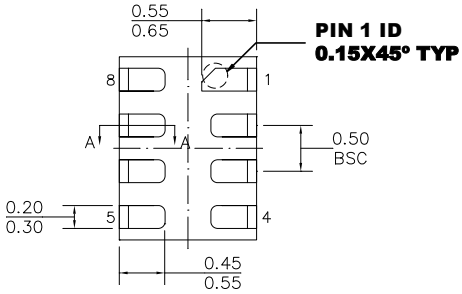
Figure 7: Typical Application Circuit (12V Output with EMI Filter)

PACKAGE INFORMATION

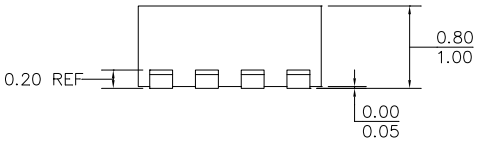
QFN-8 (1.5mmx2mm)
Wettable Flank



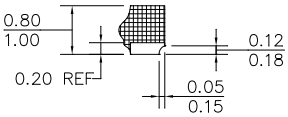
TOP VIEW



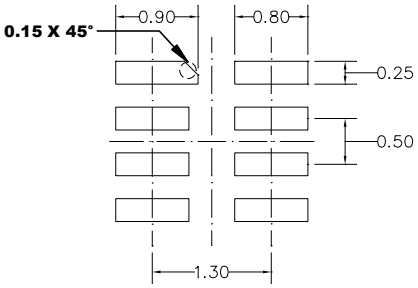
BOTTOM VIEW



SIDE VIEW



SECTION A-A

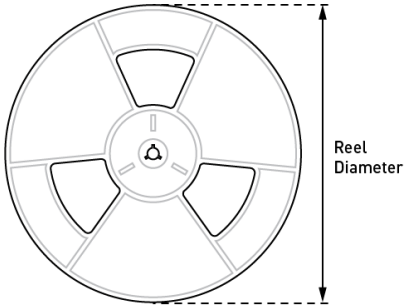


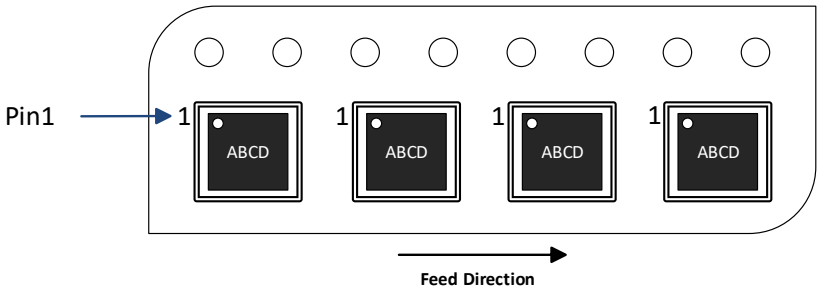
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3438GQHE-xxxx-AEC1-Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ3438GQHE-0000-AEC1-Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ3438GQHE-0001-AEC1-Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/20/2023	Initial Release	-