

N-Ch 60V Fast Switching MOSFETs

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

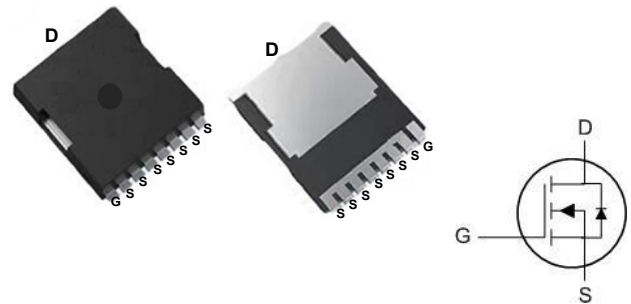
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Product Summary



BVDSS	RDSON	ID
60V	1.8mΩ	200A

TOLL-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	200	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	100	A
I_{DM}	Pulsed Drain Current ²	810	A
EAS	Single Pulse Avalanche Energy ³	352.8	mJ
I_{AS}	Avalanche Current	42	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	96	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	48	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.3	$^\circ\text{C/W}$

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	---	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	1.8	2.4	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2	2.8	4	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=60V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=60V$, $V_{GS}=0V$, $T_J=100^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=10V$, $I_D=20A$	---	89	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	2.2	---	Ω
Q_g	Total Gate Charge	$V_{DS}=30V$, $V_{GS}=10V$, $I_D=20A$	---	68	---	nC
Q_{gs}	Gate-Source Charge		---	16	---	
Q_{gd}	Gate-Drain Charge		---	20.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V$, $V_{DD}=30V$, $R_G=3\Omega$, $I_D=20A$	---	17	---	ns
T_r	Rise Time		---	17.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	40	---	
T_f	Fall Time		---	21	---	
C_{iss}	Input Capacitance	$V_{DS}=30V$, $V_{GS}=0V$, $f=1MHz$	---	4070	---	pF
C_{oss}	Output Capacitance		---	1053	---	
C_{rss}	Reverse Transfer Capacitance		---	31	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	200	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	800	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=20A$, $di/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	56	---	nS
Q_{rr}	Reverse Recovery Charge		---	67.5	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $T_J = 25^\circ\text{C}$, $V_{DD}=25V$, $V_{GS}=10V$, $L=0.4mH$, $I_{AS}=42A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

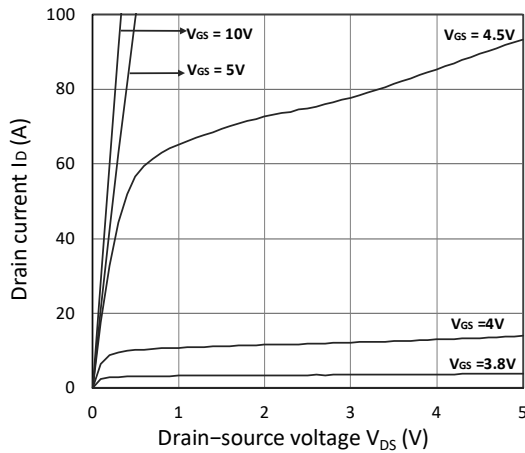


Figure 1. Output Characteristics

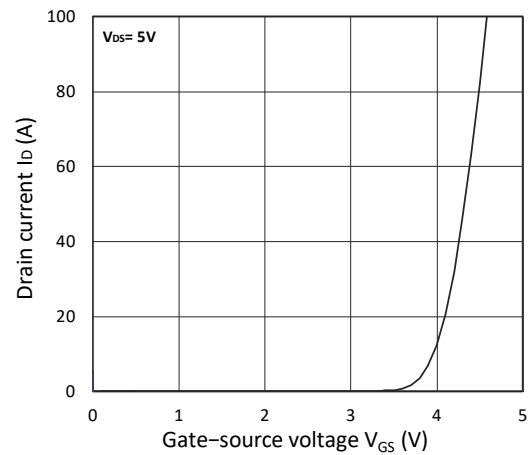


Figure 2. Transfer Characteristics

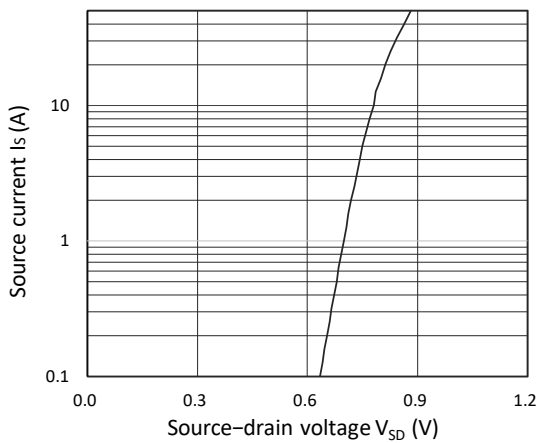


Figure 3. Forward Characteristics of Reverse

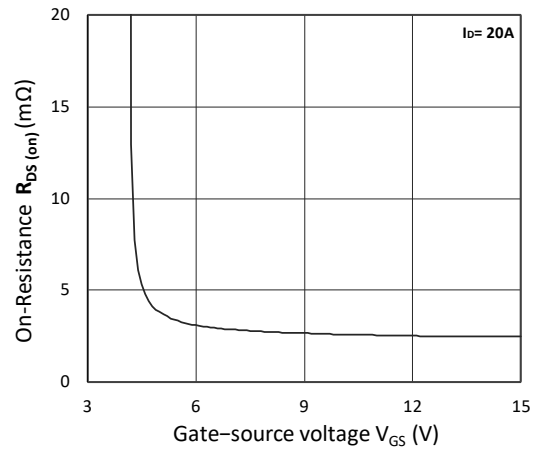


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

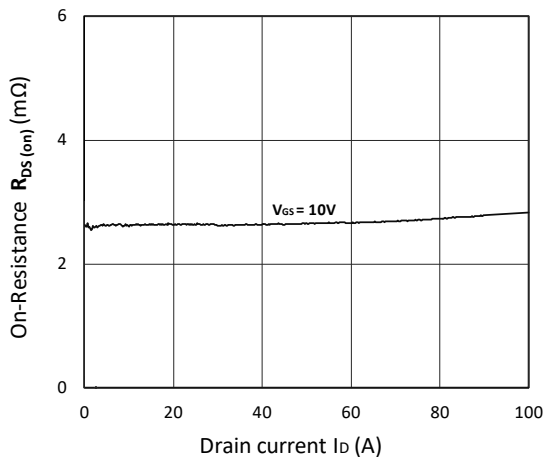


Figure 5. $R_{DS(ON)}$ vs. I_D

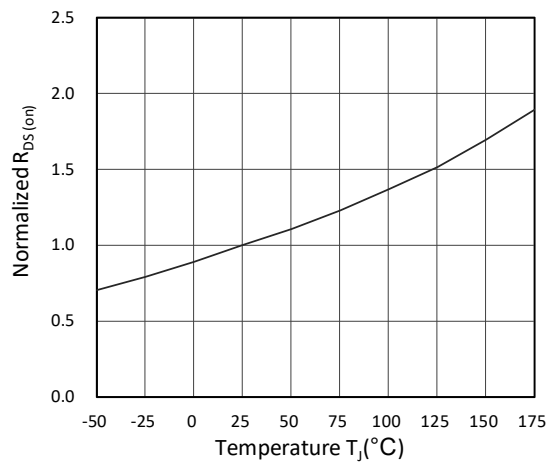


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

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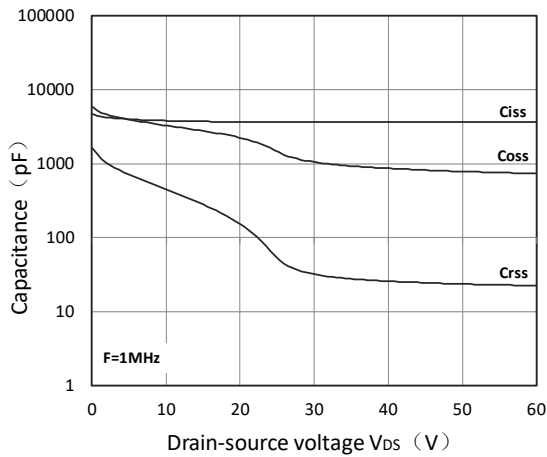


Figure 7. Capacitance Characteristics

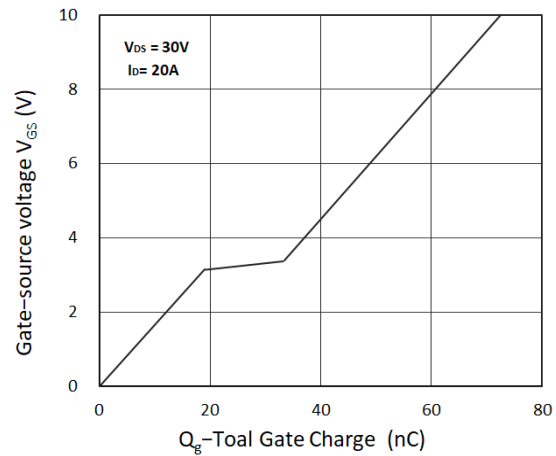


Figure 8. Gate Charge Characteristics

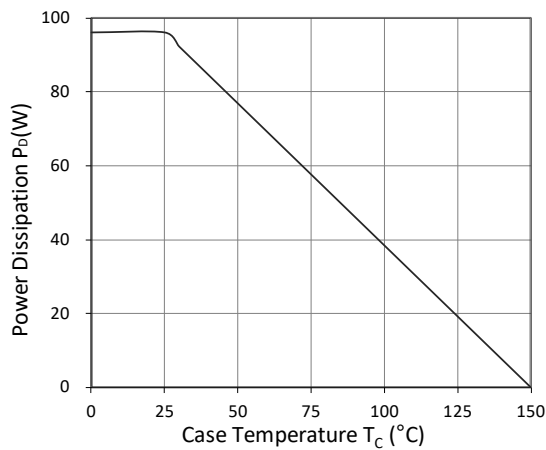


Figure 9. Power Dissipation

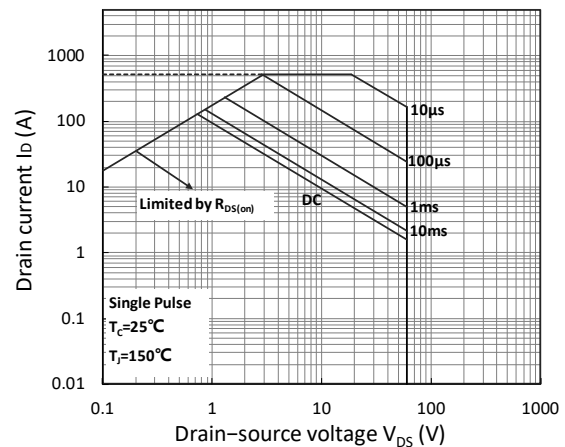


Figure 10. Safe Operating Area

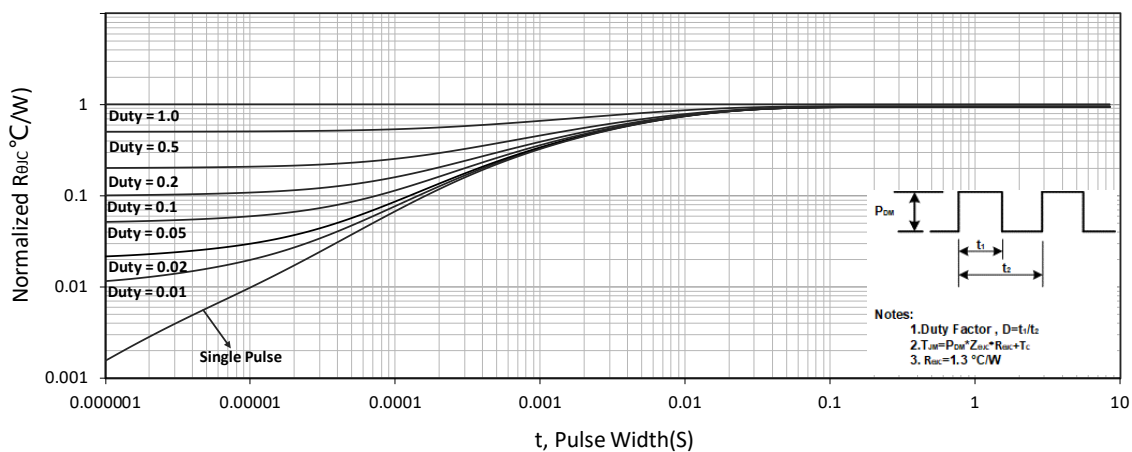
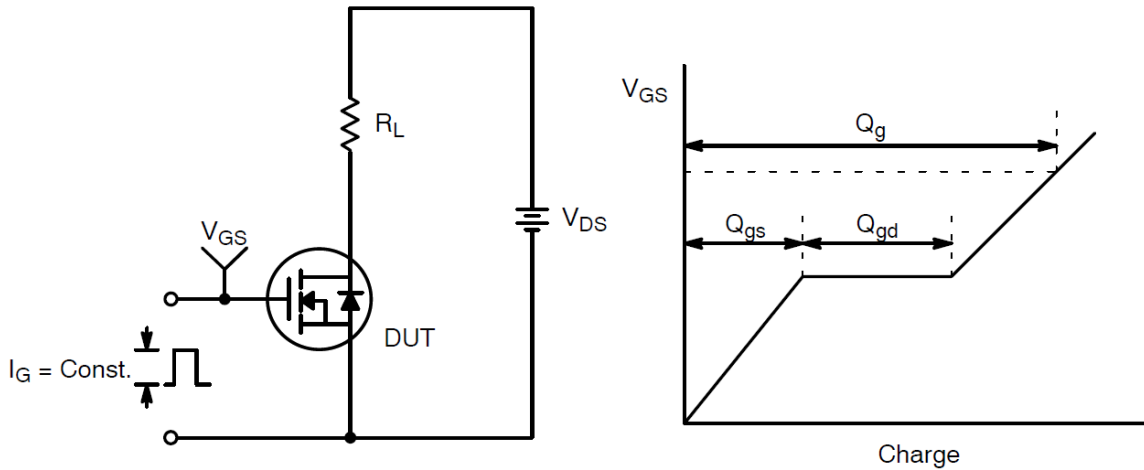
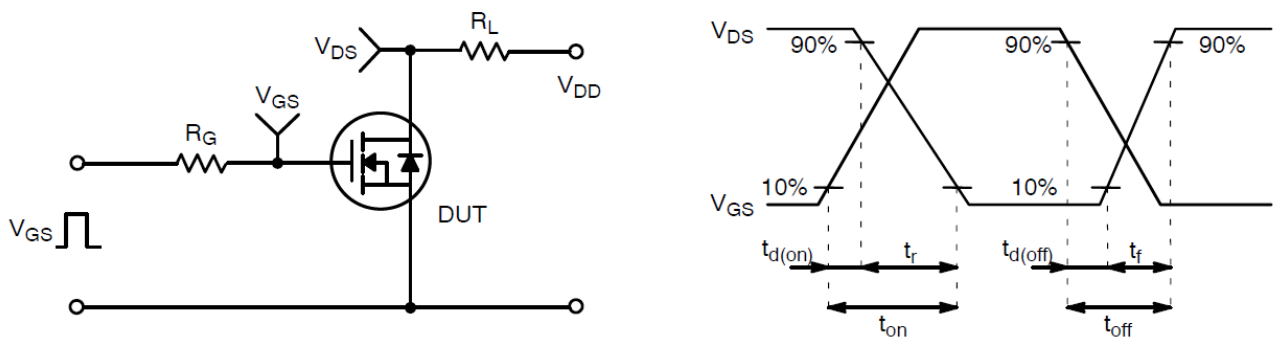


Figure 11. Normalized Maximum Transient Thermal Impedance

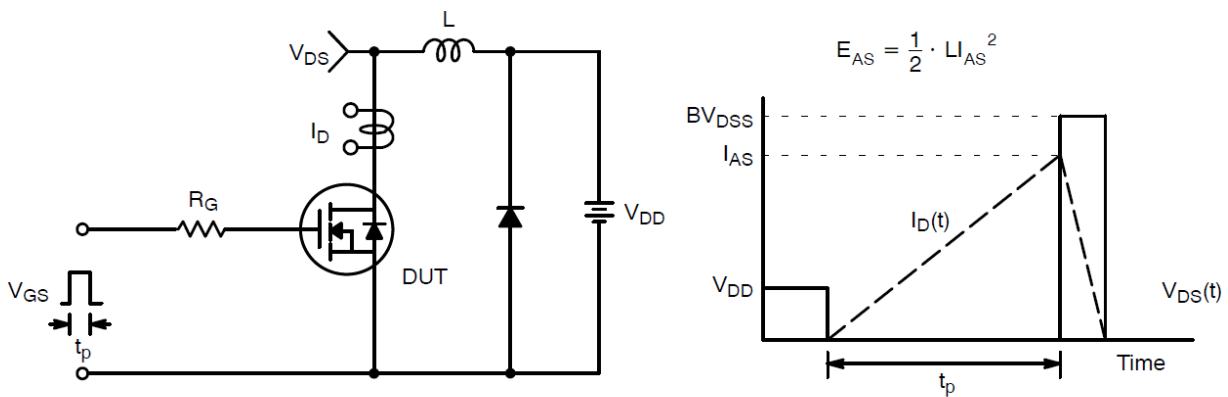
Test Circuit and Waveform:



Gate Charge Test Circuit & Waveform

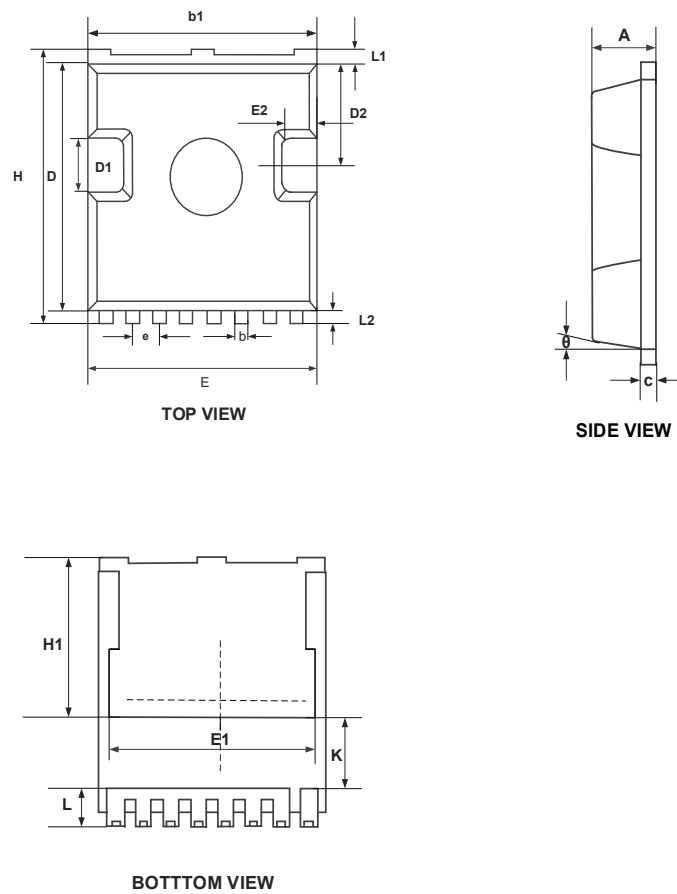


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

Mechanical Dimensions for TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	