RN830x_RN730x V3 Data Sheet

Available for V3 version chips

Version: V1.2

Revision History

Version	Date	Operators	Major Changes
V1.0	2023-4-24	Renergy	First release
V1.1	2023-5-17	Renergy	1.Revised Rogowski coil sensor register description 2.Added description of error wiring registers
V1.2	2023-6-20	Renergy	1.Modify the HSDC section description 2.Added a description of SAR registers to the ECT section 3.The EMUIF register attribute is revised to R/W 4.Revised description of relationships when HFCONST cascade is used

Content

1 General Description

The RN8302B\ RN8302C\ RN8306\ RN7302\ RN7306 is a multi-functional, high accurate, high-reliability, low-power energy metering device, which can be widely used in smart meters, energy consumption analysis, power monitoring, power safety and other fields of instrument design.

The RN8302B\ RN8302C\ RN8306\ RN7302\ RN7306 Support current transformers, shunt and Rogowski coil sensor, typical applications include: Power Grid Smart Meter (current transformer, shunt), Power Grid IoT meter (current transformer, shunt), Power Grid Guide Rail meter (Rogowski coil sensor).

This manual mainly introduces the system functions, register definitions, calibration methods and communication interfaces of polyphase energy metering device. Pin configuration and other model information, please refer to the ***Renergy Polyphase Energy Metering IC Data Sheet***. At present, Renergy has developed several versions of polyphase energy metering device, and this manual applies to the V3 version. For the difference between the V3 version and other versions of the polyphase energy metering device and the software adjustment temperature coefficient scheme, please refer to the ***Renergy polyphase energy metering IC Introduction***.

1.1 Features

- Metrology
  - ✓ Total/fundamental active energy, dynamic range: 10000:1, error <0.1%, accuracy: 0.5S and 0.2S. Support bidirectional metering, accumulation modes: algebraic sum, absolute sum, positive or negative direction, accumulation source: instantaneous power or half-cycle power. Support active energy standards: IEC62053-22:2020, GB/T 17215.321-2021 and OLML R 46-1/2:2012.
  - ✓ Total/fundamental reactive energy, dynamic range: 10000:1, error <0.1%. Support bidirectional metering, accumulation modes: algebraic sum, absolute sum, positive or negative direction, and accumulation source: instantaneous power or half-cycle power. Support reactive energy standards: IEC62053-23:2020, GB/T 17215.323-2008 and OLML R 46-1/2:2012.
  - ✓ Total/fundamental apparent energy, accumulation source: instantaneous power or half-cycle power.
  - ✓ Active and reactive power directions, support four-quadrant judgment
  - ✓ No-load/Start-up mode under power or current is selectable, and the threshold is adjustable
  - ✓ Adjustable Electricity Meter Constant
  - ✓ Fast pulse counting of active, reactive, and apparent power
  - ✓ 5 configurable CF pulse outputs (total/fundamental active/reactive/apparent is selectable)
  - ✓ Per-phase metrology with 3 configurable per-phase CF pulse outputs (total/fundamental active/reactive/apparent is selectable)
  - ✓ 12 custom power registers and 3 custom CF pulse outputs, independent pulse constants, support harmonic energy meters, and support the standard: GB/T 17215.302-2013
  - ✓ Include RMS, PQS two kinds of apparent power/energy metrology, support IEEE1459-2010, GB/T 18216_12-2010 and the latest standards
- Measurement
  - ✓ Total/fundamental active/reactive/apparent power, support IEEE1459-2010, GB/T 18216_12-2010 and the latest standards
  - ✓ Per-phase total active and reactive power with half-cycle update, update mode: zero-crossing mode or half-cycle mode, support the IEC61000-4-30:2008 standard

- ✓ Per-phase fundamental active and reactive power with half-cycle update, update mode: zero-crossing mode or half-cycle mode, support the IEC61000-4-30:2008 standard
- ✓ Polyphase voltage/current RMS of total/fundamental/harmonics
- ✓ 8kSPS fundamental instantaneous RMS
- ✓ Two kinds of half-cycle RMS: metering channel and simultaneous sampling channel
- ✓ The RMS output of three-phase voltage vector sum and current vector sum, and the participation mode of A\B\C phases in voltage vector and calculation can be configured
- ✓ Total/fundamental power factor
- ✓ Voltage line frequency, accuracy < 0.02%, update period:1-cycle or 32-cycle
- ✓ Phase angle of voltage and current of each phase, accuracy < 0.02°, update period: 1-cycle or 32-cycle
- ✓ Seven zero-crossing detection, and threshold can be configured
- ✓ Voltage phase sequence error detection
- ✓ No-voltage indication, and the no-voltage threshold can be configured
- ✓ Voltage sag detection
- ✓ Overvoltage and overcurrent detection
- ✓ Support Rogowski coils sensor

◆ Power quality

- ✓ Support power quality analysis, waveform data required for non-intrusive load identification, multi-channel combinations of different points.
- ✓ Support S-class power quality analysis, implementation standard: IEC61000-4-30:2008. Including harmonics, interharmonics, unbalance, voltage fluctuations, flicker, surging, dipping, etc;
- ✓ Two sets of half-cycle RMS measurements for calculations such as swells and sags
- ✓ Fault waveform recording
- ✓ Implement flicker calculation according to IEC standards. Support instantaneous flicker calculation result output

◆ Waveform output

- ✓ Variety of instantaneous/synchronous, total/fundamental, voltage/current/power waveform data
- ✓ Up to 512 points/cycle fixed sampling/synchronous sampling rate data. Automatic compensation of harmonic gain in the entire band. DC offset/phase/gain calibration of waveform data
- ✓ 896 address units (3 bytes per unit) for ADC data buffer, supporting multi-channel combinations of different points
- ✓ Up to 64 consecutive address units (3 bytes per unit) SPI burst read waveform buffer

◆ Automatic error temperature offset (ECT)

- ✓ SAR&TPS temperature measurement, measurement requirement: ±2°C
- ✓ Hardware automatic temperature offset/semi-automatic temperature offset/software automatic temperature offset, etc. High/low temperature segment linear gain offset

◆ Electricity anti-tamper

- ✓ Support neutral current measurement, Maximum PGA gain of neutral current ADC:16 times, which is convenient for shunt sampling
- ✓ Low-power mode NVM2 for current comparison prediction, four selectable thresholds, consumption <150μA
- ✓ Low-power mode NVM1 for low-power RMS current measurement, consumption< 2.5mA
- ✓ No-voltage active reporting, typical applications consumption only 7μA on average

◆ Software calibration

- ✓ Seven ADC channel gain calibration
- ✓ Seven ADC channel phase calibration, where A/B/C phase current channel support segment phase calibration
- ✓ Power gain calibration
- ✓ Active/reactive segment phase calibration
- ✓ Active/reactive/RMS Offset calibration
- ✓ AUTODC DCOffset calibration
- ✓ Check sum register, which can check calibration dates automatically
- ✓ Pulse acceleration for small signal calibration

◆ Support the new test requirements in OLML R 46 for spike waves, flat top waves, etc

◆ Support the requirements of dynamic load metering and rapid change of load current

◆ Suitable for 3-phase 3-wire, 3-phase 4-wire system. Support 3-phase 3-wire and 3-phase 4-wire adaptation

◆ Supply monitoring

◆ Internal 1.25V ADC reference voltage, temperature coefficient: ±5ppm/°C typically. External reference can also be applied

◆ High-speed SPI interface, maximum transmission rate: 3.5Mbps. Support burst read waveform buffer or registers

◆ High-speed waveform data text HSDC interface, maximum transmission rate: 4.096Mbps, and CRC verification is supported

◆ Two interrupt output pins

◆ Crystal oscillator: 8.192MHz, the chip integrates a 10MΩ bias resistor

◆ Operating voltage range: 3.3V±10%

◆ Operating temperature range: -40℃~+85℃

◆ Support LQFP32/LQFP44/LQFP48 green package

◆ Support the test requirements of amendment (EU) 2015/863 of the Annex to the EU RoHS Directive 2011/65EU

1.2 Functional Block Diagram

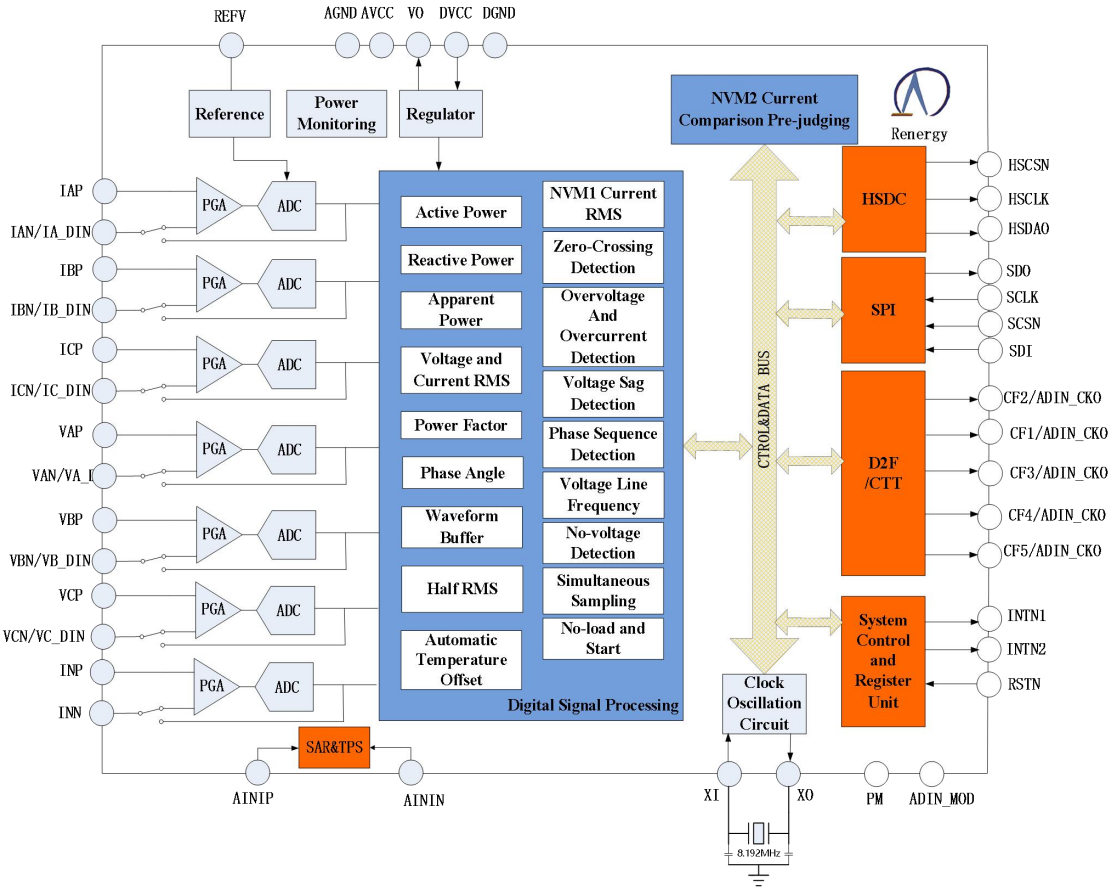


Figure 1-1 Functional Block Diagram

2 Features comparison

Renergy polyphase metering device has planned different product models for different application needs. The specific instruction are as follows:

RN8302B applied to traditional ordinary three-phase metrology scheme, packaged as LQFP44;

RN7302 is suitable for low-cost small size electrical metrology meter, packaged as LQFP32;

RN8302C has ADCIN mode, in which the chip and three Renergy ADC device RN8207D cooperate to realize a three-phase shunt meter, the specific ADCIN mode entry method and application wiring refer to 4.7 "RN8302C applied to three-phase shunt meter –case1" and 4.8" RN8302C applied to three-phase shunt meter –case2";

RN8306 (LQFP44)/RN7306 (LQFP48) has dual SPI ports, with waveform data real-time output function, which can be used in three-phase metering fields with high-end needs such as harmonic measurement, power quality, topology identification, and non-intrusive load identification; The RN7306 also features a SAR ADC for DC voltage measurement.

Specific product models and their sources refer to "Table 2-1 Model source Comparison"

Table 2-1: Model source comparison

	Model				
Source	RN8302B	RN8302C	RN8306	RN7302	RN7306
Total pin number	44	44	44	32	48
CF number	5	5	5	3	5
INT2	×	√	√	×	√
ADCIN mode	×	√	×	×	×
EMM mode	√	×	√	√	√
NVM1 mode	√	×	√	×	√
NVM2 mode	√	×	√	×	√
SLEEP mode	√	×	√	√	√
PM pin	√	√	×	×	×
ADIN_MOD pin	×	√	×	×	×
ADIN_CKO	×	√	×	×	×
HSCLK	×	×	√	×	√
HSDAO	×	×	√	×	√
HSCSN	×	×	√	×	√
AINIP	×	×	×	×	√
AININ	×	×	×	×	√

Note: × in the table indicates that there is no corresponding function, and √ indicates that there is a corresponding function

3 Pin configuration

The RN7302 is in LQFP32 green package; RN8302B, RN8302C and RN8306 are all LQFP44 green packages; The RN7306 is in LQFP48 green package; Different types of packaged products, the pin definition is slightly different, mainly reflected in whether there is a waveform data output pin HSCLK/HSDAO/HSCSN, ADCIN MODE SELECTION PIN, PM MODE SELECTION PIN and SARADC analog sampling input pin; The source of the difference in chip functionality is also the difference in pin support. For specific pin differences, please refer to "Table 3-1 Model Pin Comparison".

Table 3-1 Model Pin Comparison

Pin number					Name	Feature	Descreption
RN8302B	RN8302C	RN8306	RN7302	RN7306			
1	1	1		1	HSCSN	Output	The RN8306/RN7306 are HSCSN pins for ADC waveform buffering dedicated HSDC interface chip select signal pins, low active.
					NC	Floating	RN8302B. The RN8302C is NC pin, floating
2	2	2		2/3	NC	Floating	NC pin, floating
3	3	3	32	4	REFV	Input/Output	This pin is either an internal reference output or an external REF input pin. An external 1μF capacitor needs to be connected in parallel to the analog ground for decoupling.
4	4	4	1	5	NC		RN8302C is NC pin, floating or analog grounding
					IAP	Input	RN8302B\RN8306\RN7302\RN7306 is IAP pin, the positive analog input pin of current sampling channel A.
5	5	5	2	6	IAN	Input	RN8302C is the input pin of the current external ADC and the A channel current sampling data of the external input.
							RN8302B\RN8306\RN7302\RN7306 is the negative analog input pin of channel A sampling current. IAP and IAN adopt a fully differential input mode, and the maximum differential input amplitude is 830mVp peak during normal operation.
6	6	6	3	7	AGND	Supply	Analog ground
7	7	7	4	8	NC		RN8302C is NC pin, floating or analog grounding

					IBP	Input	RN8302B\RN8306\RN7302\RN7306 is IBP pin, the positive analog input pin of channel B sampling current.
8	8	8	5	9	IBN	Input	RN8302C is external ADC current input, which input the external channel B sampling data
							RN8302B\RN8306\RN7302\RN7306 is the negative channel B sampling current input. IBP and IBN adopt a fully differential input method, and the maximum differential input amplitude is 830mVp peak in normal operation.
9	9	9	6	10	AVCC	Supply	Analog power supply. Operating range: 3.3V±10%, 5V±10%. This pin should be decoupled to analog ground using a 4.7μF capacitor in parallel with a 0.1μF capacitor.
10	10	10	7	11	NC		RN8302C is NC pin, floating or grounding
					ICP	Input	RN8302B\RN8306\RN7302\RN7306 is ICP pin, the active channel B sampling current input
11	11	11	8	12	ICN	Input	RN8302C is the external ADC current input, which input the external channel B sampling data
							RN8302B\RN8306\RN7302\RN7306 is the negative channel C sampling current input. ICP and ICN adopt a fully differential input method, and the maximum differential input amplitude is 830mVp peak in normal operation.
12	12	12	9	13	VAP		When this channel in RN8302C selects an external ADC input, this pin is NC pin and it is recommended not to connect it.
						Input	Positive analog input of channel A sampling voltage
13	13	13	10	14	VAN	Input	When this channel in RN8302C selects an external ADC input, this pin is external ADC input, which input external channel A sampling voltage dates
							Negative analog input pin of channel A sampling voltage. VAP and VAN adopt a fully differential input mode, and the maximum differential input amplitude is 830mVp peak in normal operation.
14	14	14	11	15	VBP		When this channel in RN8302C selects an external ADC input, this pin is NC pin and it is recommended not to connect it.
						Input	Positive and negative analog input pins of channel B sampling voltage. With a fully differential input method, the normal maximum differential input amplitude is 830mVp peak.

15	15	15	12	16	VBN	Input	When this channel in RN8302C selects an external ADC input, this pin is external ADC input, which input external channel B sampling voltage dates
							Positive and negative analog input pins of channel B sampling voltage. With a fully differential input method, the normal maximum differential input amplitude is 830mVp peak.
16	16	16	13	17	VCP		When this channel in RN8302C selects an external ADC input, this pin is NC pin and it is recommended not to connect it.
						Input	Positive and negative analog input pins of channel C sampling voltage. With a fully differential input method, the normal maximum differential input amplitude is 830mVp peak.
17	17	17	14	18	VCN	Input	When this channel in RN8302C selects an external ADC input, this pin is external ADC input, which input external channel C sampling voltage dates
							Positive and negative analog input pins of channel C sampling voltage. With a fully differential input method, the normal maximum differential input amplitude is 830mVp peak.
18	18	18	15	19	INP		When this channel in RN8302C selects an external ADC input, this pin is NC pin and it is recommended not to connect it.
						Input	Positive and negative analog input pins of neutral line sampling current. With a fully differential input method, the normal maximum differential input amplitude is 830mVp peak.
19	19	19	16	20	INN	Input	When this channel in RN8302C selects an external ADC input, this pin is external ADC input, which input external neutral line sampling current dates
							Positive and negative analog input pins of neutral line sampling current. With a fully differential input method, the normal maximum differential input amplitude is 830mVp peak.
				21	AIN1	Input	SARADC sampling channel 1 analog input pin. Input range 0~1.25V. The V31 version of the chip recommends using this pin as an analog test input pin.
				22	AIN2	Input	SARADC sampling channel 2 analog input pin. Input range 0~1.25V. This pin is not recommended for the V31 version of the chip.
20	20	20		23	RA		Reserved, analog grounding

21	21	21		24	NC		NC pin, analog grounding
22	22	22		25	CF5	Output	The energy check pulse output can be flexibly configured as a fundamental/total, active/reactive/apparent all-phase pulse or high-frequency all-phase pulse output via the CFCFG register.
23	23	23		26	CF4		
24	24	24	17	27	CF3		
25	25	25	18	28	CF2		
26	26	26	19	29	CF1		
27	27	27	20	30	RSTN	Input	Reset pin, active low. Internal floating, need to connect external supply or external 1 KΩ Pull-up Resistor
28	28	28	21	31	DVCC	Supply	Digital supply. Operating range: 3.3V±10%/5V±10%. This pin should be decoupled using a 4.7μF capacitor in parallel with a 0.1μF capacitor to digital ground.
29	29	29		32	DGND		Digital ground
30	30	30		33	NC		RN8302B is NC pin, floating or digital grounding
					INTN2	Output	It is interrupt output in RN8302C/RN8306/RN7306, active low, and high level default. When an interrupt event allowed by the interrupt enable register occurs, the pin level flips. When the CPU clears the corresponding interrupt flag bit through the SPI interface, the pin returns high.
31	31	31	22	34	INTN1	Output	Interrupt output pin, active low. The default high level flips the pin level when an interrupt event allowed by the interrupt enable register occurs. When the CPU clears the corresponding interrupt flag bit through the SPI interface, the pin returns high.
32	32	32	23	35	SDO	Output	SPI serial data output, SCLK rising edge chip sends data; When SCSN is high, the output is high impedance.
33	33	33	24	36	SCLK	Input	SPI serial clock input. A serial clock configured for a synchronous serial interface, generated by the MCU. The host writes data at the SCLK high level, and the chip takes data on the SCLK falling edge.
34	34	34	25	37	SCSN	Input	SPI select signal, low active.
35	35	35	26	38	SDI	Input	SPI serial data input, serial interface data input; The SCLK falling edge is valid data.
36	36	36	27	39	XO	Output	The output of the clock crystal.
37	37	37	28	40	XI	Input	The input of the clock crystal, or the external system clock input. The typical frequency of the clock crystal is 8.192MHz; Load capacitance is typically 15pF. In order to ensure a starting margin of more than 10 times, it is recommended to choose a crystal

							oscillator with an ESR value of less than 100 ohms. The crystal oscillator 10MΩ bias resistor is integrated, it is recommended that there is no need to span the 10MΩ resistor externally, and if the 10MΩ resistor is crossed, the starting margin can also meet the application requirements greater than 5 times.
38	38	38		41	VO	Output	Built-in regulator module output. This pin should be decoupled using a 4.7μF capacitor in parallel with a 0.1μF capacitor to digital ground. Note that this pin cannot be connected to external loads.
39	39	39	30	42	DGND	Supply	Digital ground
40	40	40	31	43	DVCC	Supply	Digital supply. Operating range: 3.3V±10%/5V±10%. This pin should be decoupled using a 4.7μF capacitor in parallel with a 0.1μF capacitor to digital ground.
				44	NC		NC pin, digital grounding
				45	NC		NC pin, digital grounding
41	41	41			RB		Reserved. RN8306 need digital grounding
							Reserved. RN8302B/RN8302C need connecting to DVCCor digital grounding
42	42	42		46	HSCLK	Output	It is HSCLK pin in RN8306/RN7306, which is the ADC waveform buffer dedicated HSDC interface serial clock output pin
					PM	Input	The default operating mode of the chip selects the input pins inRN8302B\RN8302C. PM=1, the default operating mode is sleep mode (SLM); PM=0, the default operating mode is metering mode (EMM). This pin is internally suspended and requires an external pull-up 1KΩ resistor or grounding.
43	43	43		47	ADIN_MOD	Input	It is ADIN_MOD pin in RN8302C, which is used to control ADC mode. ADIN_MOD = 1 and PM = 0, the ADC is external, and the chip receives the ADC sampling data.
					RC		It is reserved pin in RN8302B/RN8306/RN7306, digital grounding
44	44	44		48	ADIN_CKO	Output	It is ADIN_CKO pin in RN8302C, which output the clock signal, and can be the external ADC external clock.
					HSDAO	Output	It is HSDAO pin in RN8306/RN730, which is the ADC waveform buffer dedicated HSDC interface serial clock output pin , and active when building data at HSCLK rising edge
					NC		It is NC pin in RN8302B, floating

3.1 RN8302B Pin Configuration

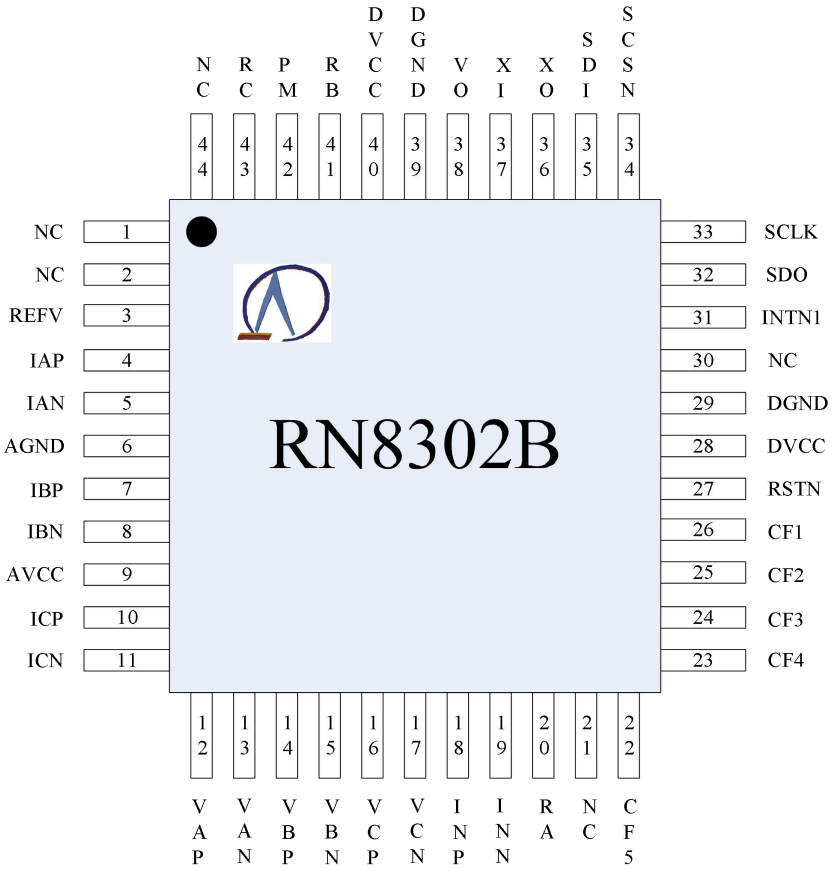


Figure 3-1 Pin configuration of RN8302B V3 version

3.2 RN8302C Pin Configuration

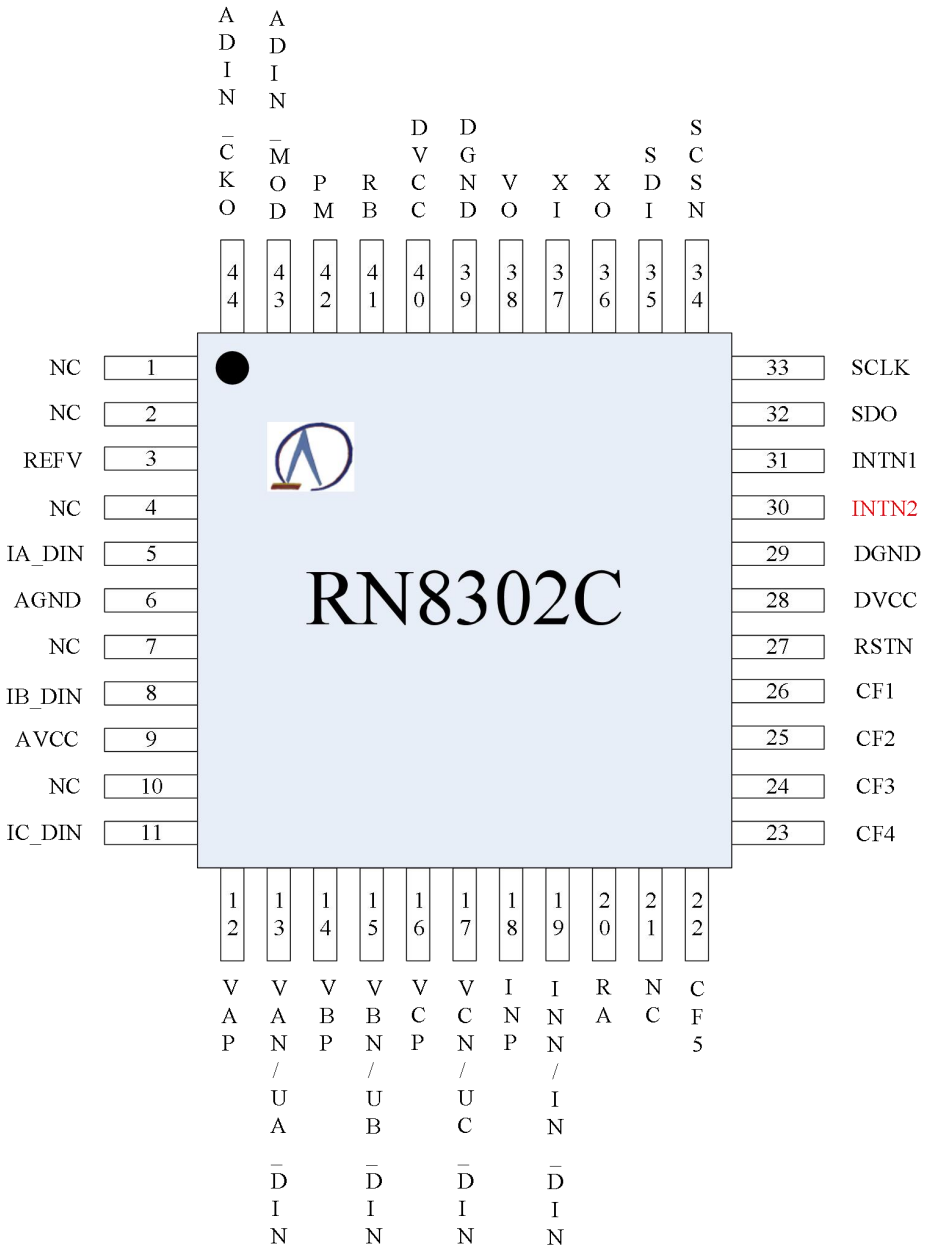


Figure 3-2 Pin configuration of RN8302C V3 version

3.3 RN8306 Pin Configuration

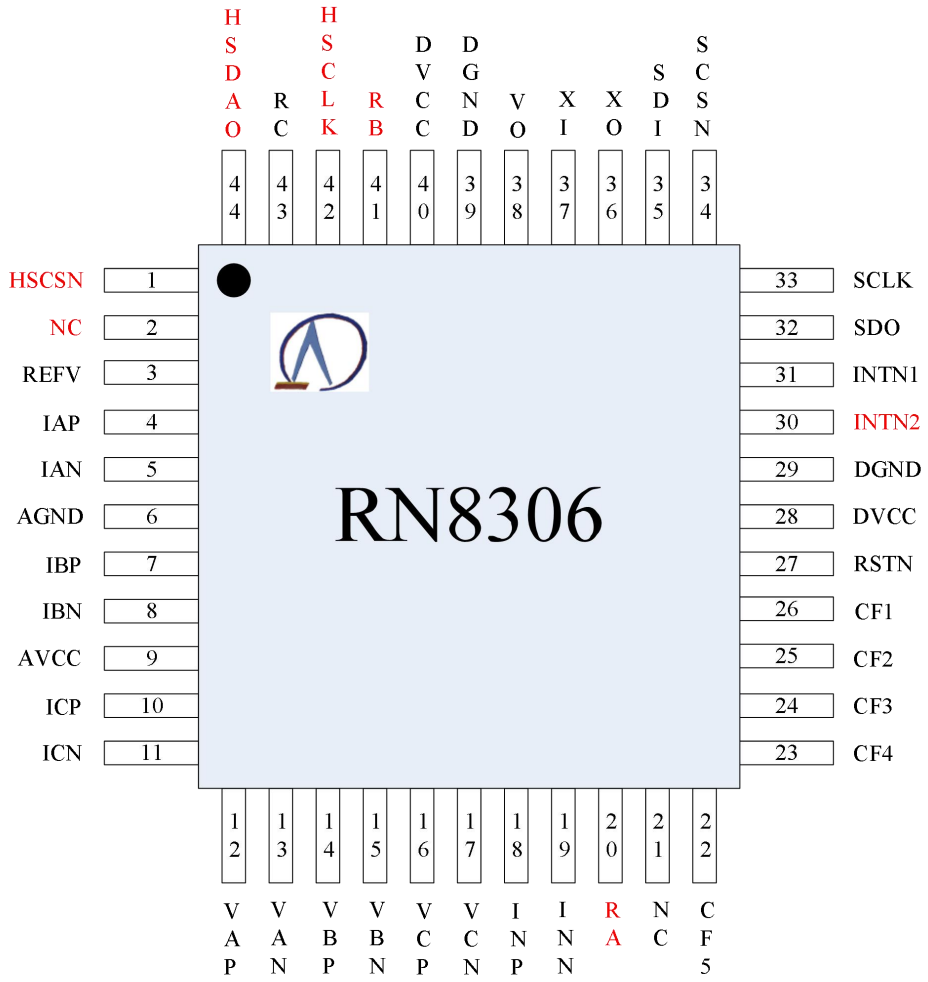


Figure 3-3 Pin configuration of RN8306 V3 version

3.4 RN7302 Pin Configuration

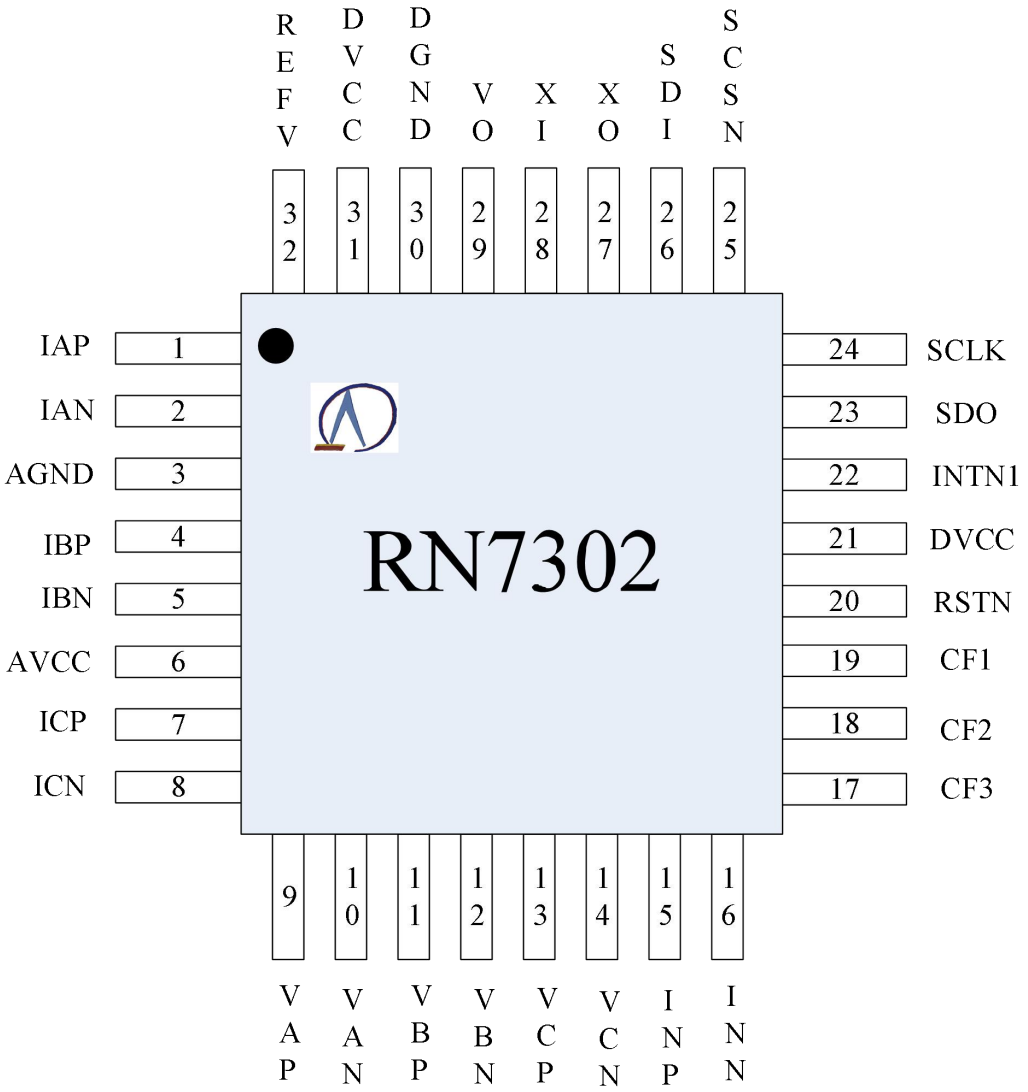


Figure 3-4 Pin configuration of RN7302 V3 version

3.5 RN7306 Pin Configuration

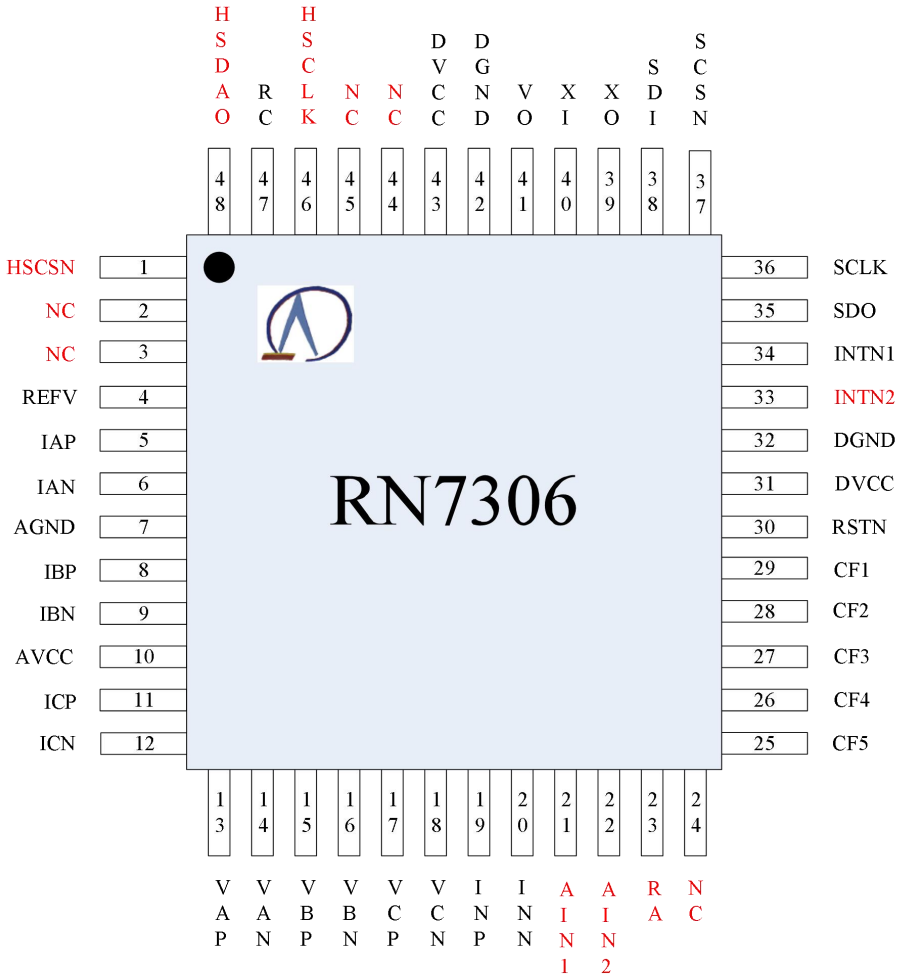


Figure 3-5 Pin configuration of RN7306 V3 version

4 Typical Application Circuit

4.1 RN8302B/RN7302 applied to a three-phase four-wire meter

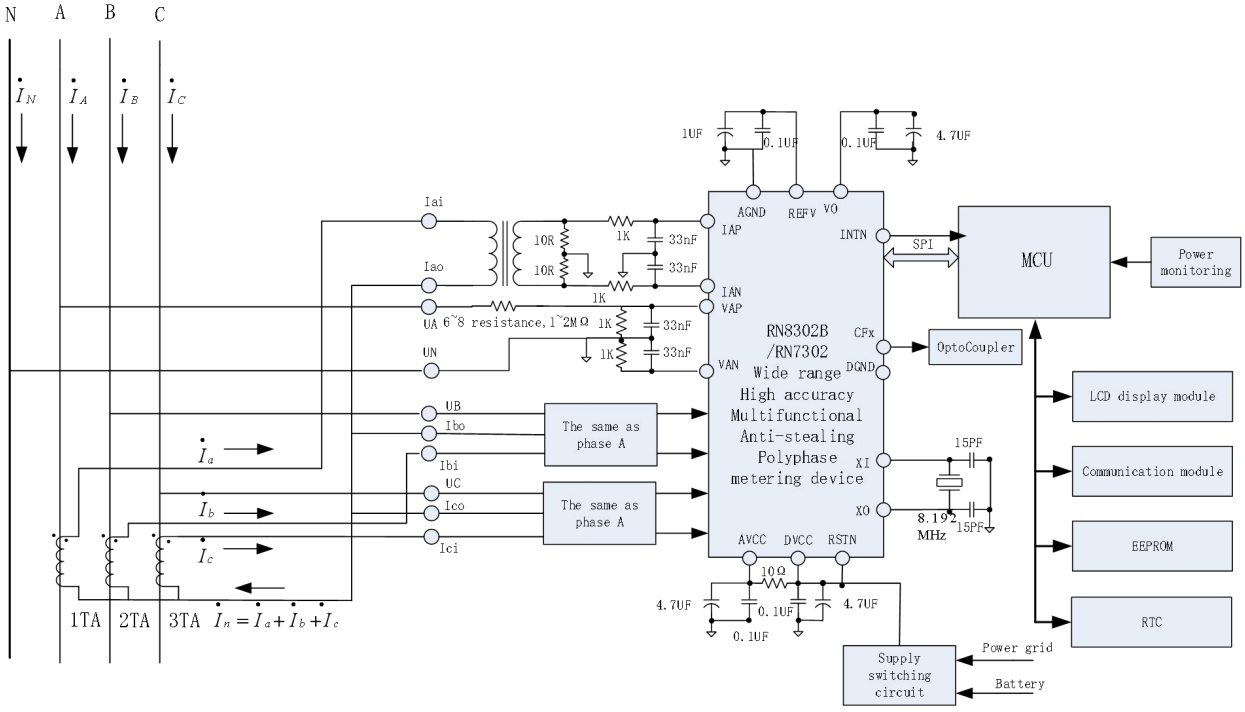


Figure4-1 Diagram of a typical application circuit when the RN8302B/RN7302 is applied to a three-phase four-wire meter

4.2 RN8302B/RN7302 applied to a three-phase three-wire meter

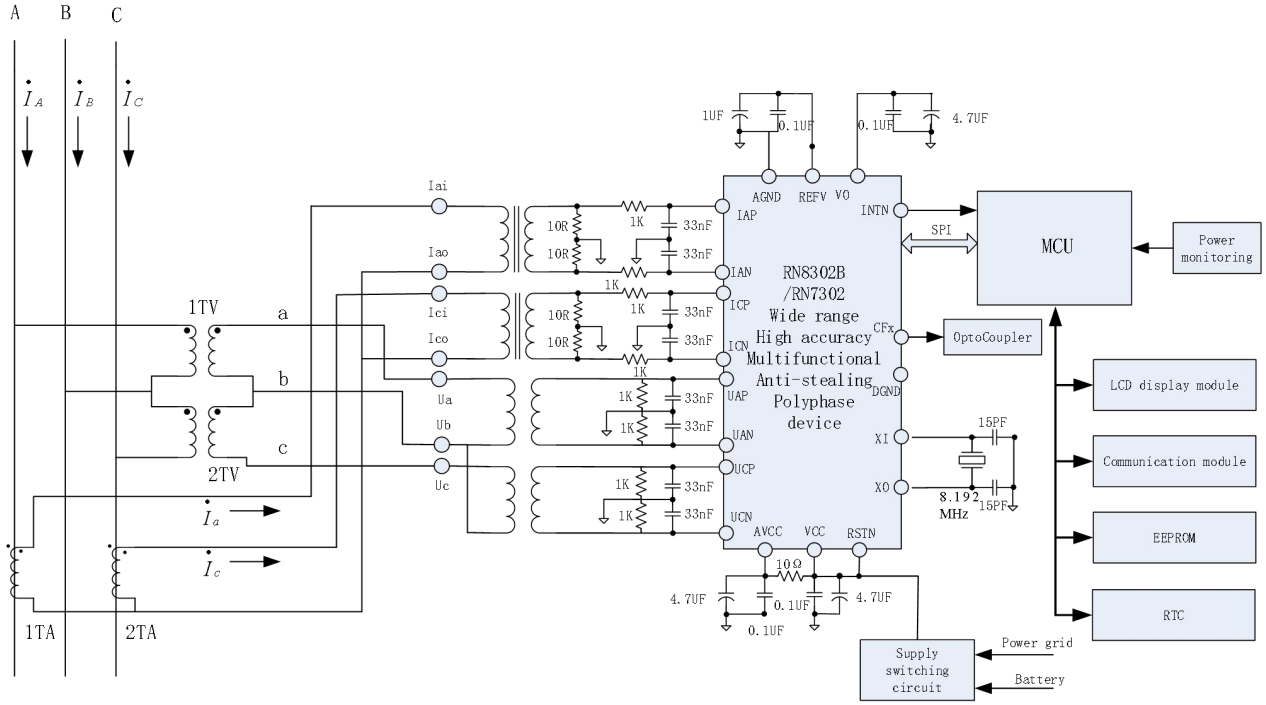


Figure 4-2 Diagram of a typical application circuit when the RN8302B/RN7302 is applied to a three-phase three-wire meter

4.3 RN8306 applied to a three-phase four-wire meter

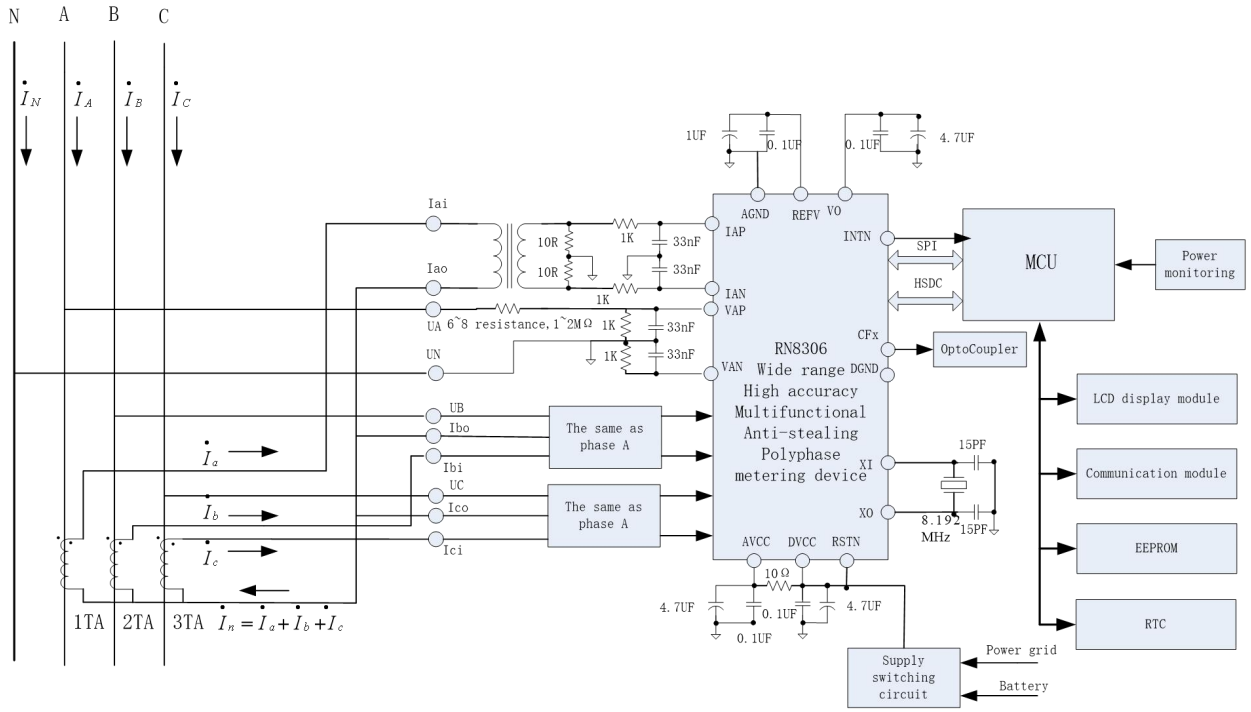


Figure 4-3 Diagram of a typical application circuit when RN8306 is applied to a three-phase four-wire meter

4.4 RN8306 applied to a three-phase three-wire meter

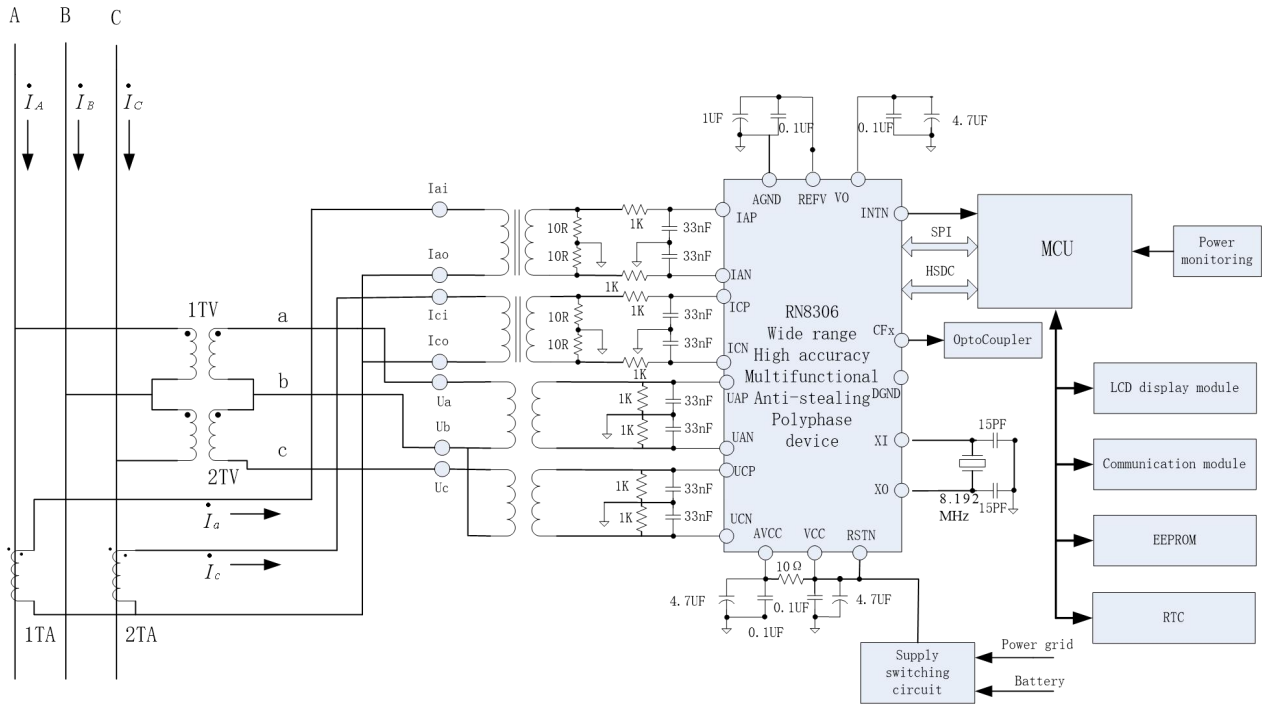


Figure 4-4 Diagram of a typical application circuit when RN8306 is applied to a three-phase three-wire meter

4.5 RN7306 applied to a three-phase four-wire meter

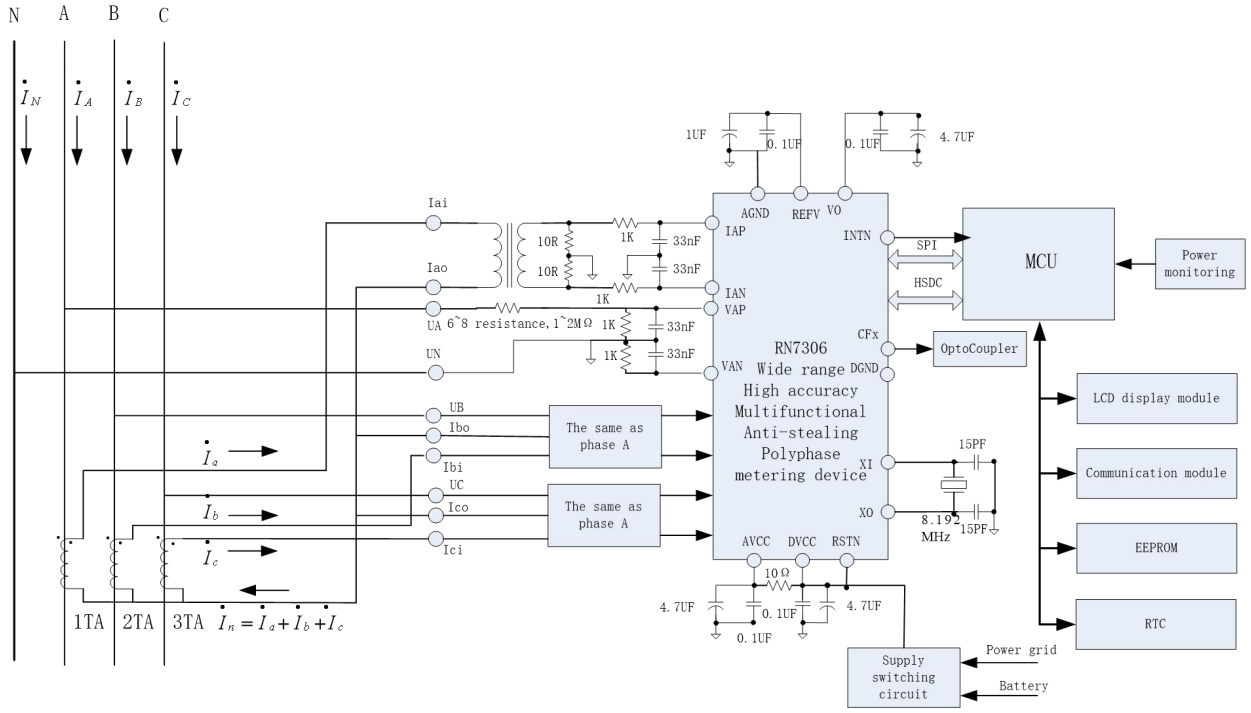


Figure4-5 Diagram of a typical application circuit when RN7306 is applied to a three-phase four-wire meter

4.6 RN7306 applied to a three-phase three-wire meter

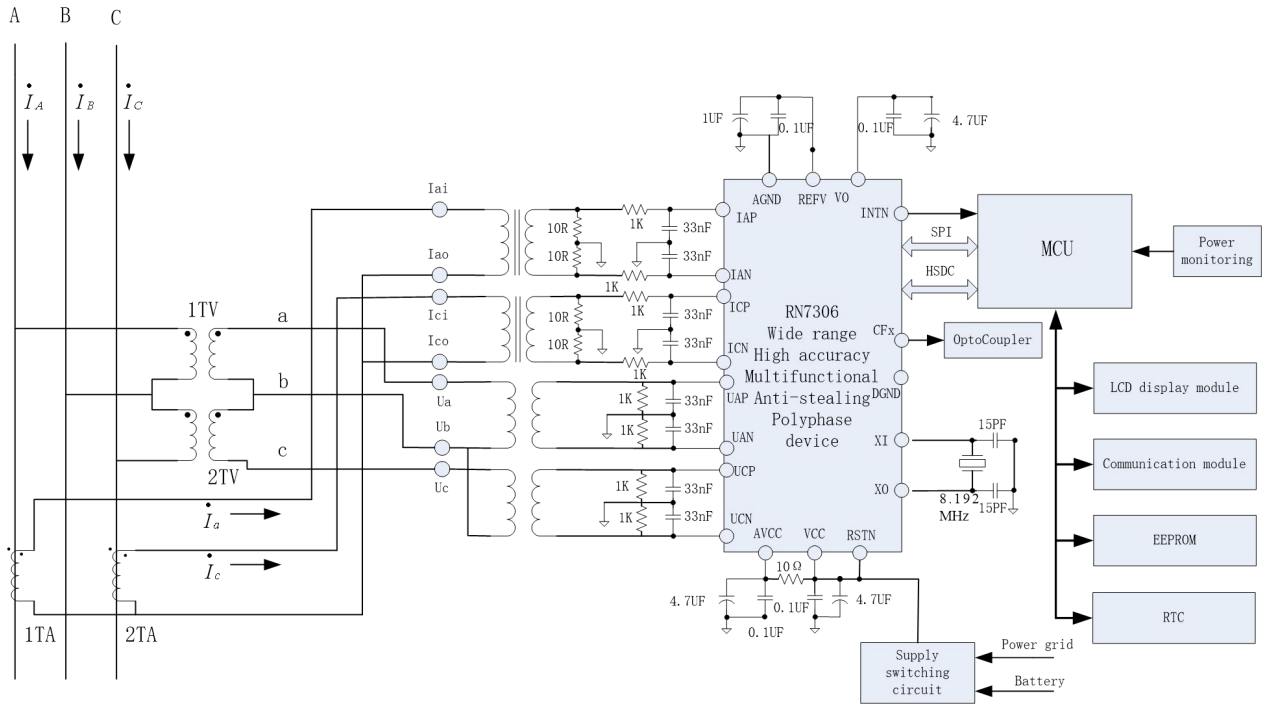


Figure 4-6 Diagram of a typical application circuit when RN7306 is applied to a three-phase three-wire meter

4.7 RN8302C applied to three-phase shunt meter -case 1

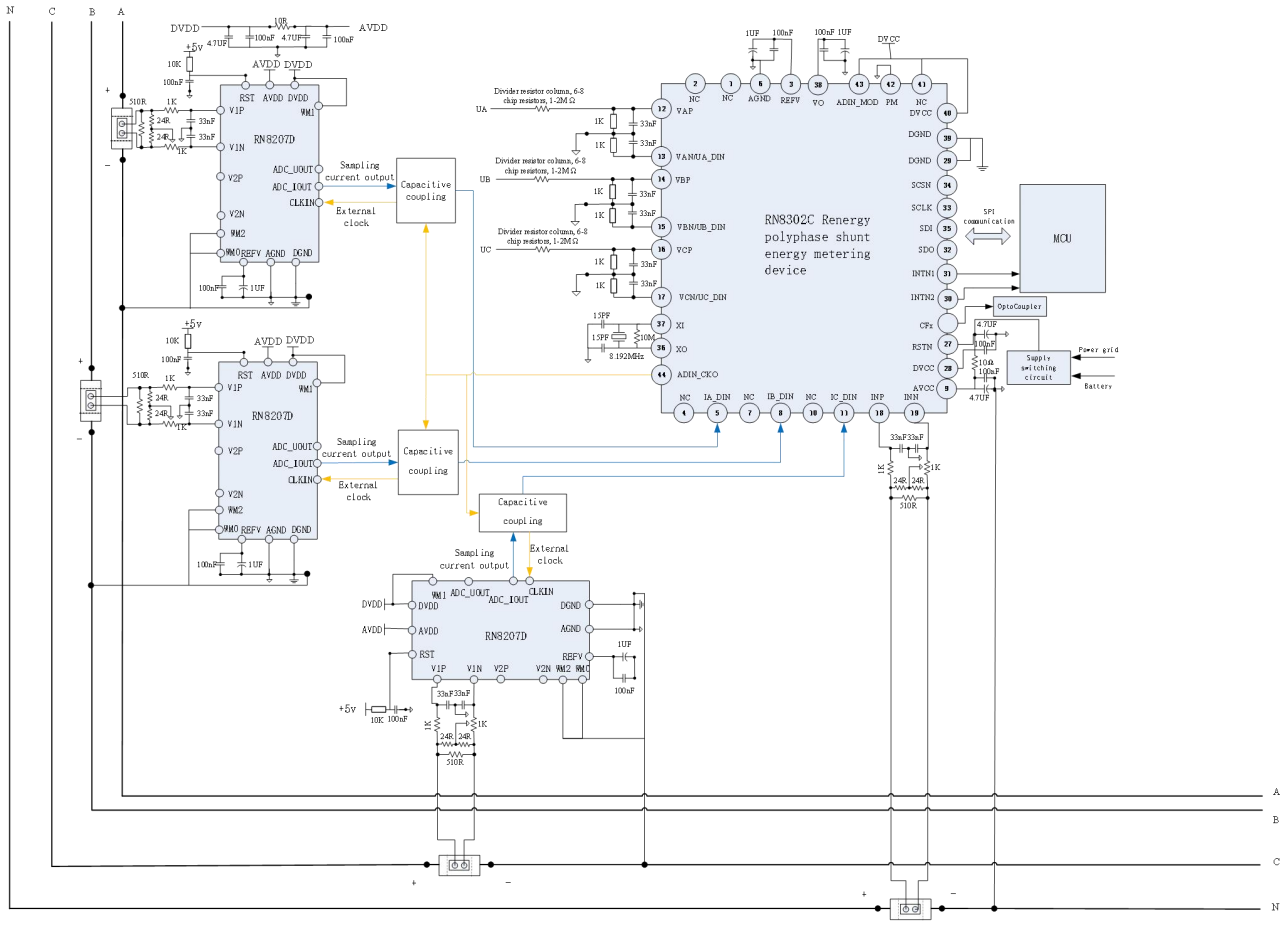


Figure 4-7 Diagram of RN8302C applied to three-phase shunt meter -case 1

The scheme uses three external current ADC sampling inputs, one built-in neutral current, and three built-in voltage channel ADCs.

Among them, 3 external current ADC sampling inputs are realized by 3 Renergy chips RN8207D; The ADC chip RN8207D required external clock, which is output from the ADIN_CKO pin of the RN8302C to ensure that the clocks of each chip are of the same origin; The ADC chip RN8207D sampling outputs, which are input from the IA_DIN, IB_DIN, and IC_DIN pins of the RN8302C.

One built-in neutral current channel ADC for neutral current sampling is fully differential input, and the maximum differential signal input amplitude of the neutral current channel is 830mVp peak.

Three built-in voltage-channel ADCs are used for voltage sampling and are fully differential inputs with a maximum differential signal input amplitude of 830mVp peak.

This case requires to configure the RN8302C metering mode at ADCIN mode by hardware; This is realized by configuring the ADIN_MOD pin to 1 and the PM pin to 0;

Software configuration of case 1: The phase A\B\C sampling channels current of RN8302C are configured as external ADC sampling inputs, one neutral current and three sampling channel voltages are configured as built-in ADC sampling inputs. The register of RN8302C to configure the external ADC is the ADCIN mode configuration register (ADCIN_CFG), which is located in the Bank1 area at address 0xA1. ADCIN mode configuration register operation is WREN(0x180) and ADCIN_WREN(0x1A0) write-protected, and write-protected needs to be turned on before operation. The specific configuration method is that the host computer sends configuration commands

to the RN8302C through SPI in turn.

1.Write 0xE5 to Bank1 register address 0x80H

2.Write 0xEA to Bank1 register address 0XA1H

3.Write 0x40 to Bank1 register address 0xA0H

After the software configuration is completed, the host computer is required to read the two-byte value of the Bank1 register address 0xA0H as 0x0040 through SPI to confirm that the software configuration is successful.

In this case, RN8302C use the built-in ADC to do three-phase voltage and neutral current sampling, with the neutral line as the ground, so the RN8302C and RN8207D which uses three-phase current sampling need to be isolated with capacitive coupling, and the isolation voltage of capacitive coupling is recommended to be 2000V~3000V. The design here needs to pay attention to the fact that in the scenario where the RN8207D power-down ratio is faster than RN8302C, the 1-bit stream output by the ADC in the RN8207D will be a fixed value at the output of the capacitive coupling back-end to the RN8302C, and this fixed value, whether it is 1 or 0, represents the maximum value for the RN8302C, which may cause the phenomenon of pulsing without adding current when powering down. In practice, customers are required to circumvent this situation, and can control the power up and down sequence of hardware, or judge the power off and shutdown RN8302C in advance according to SAG on software, or handle it at the same time on software and hardware.

4.8 RN8302C applied to three-phase shunt meter -case 2

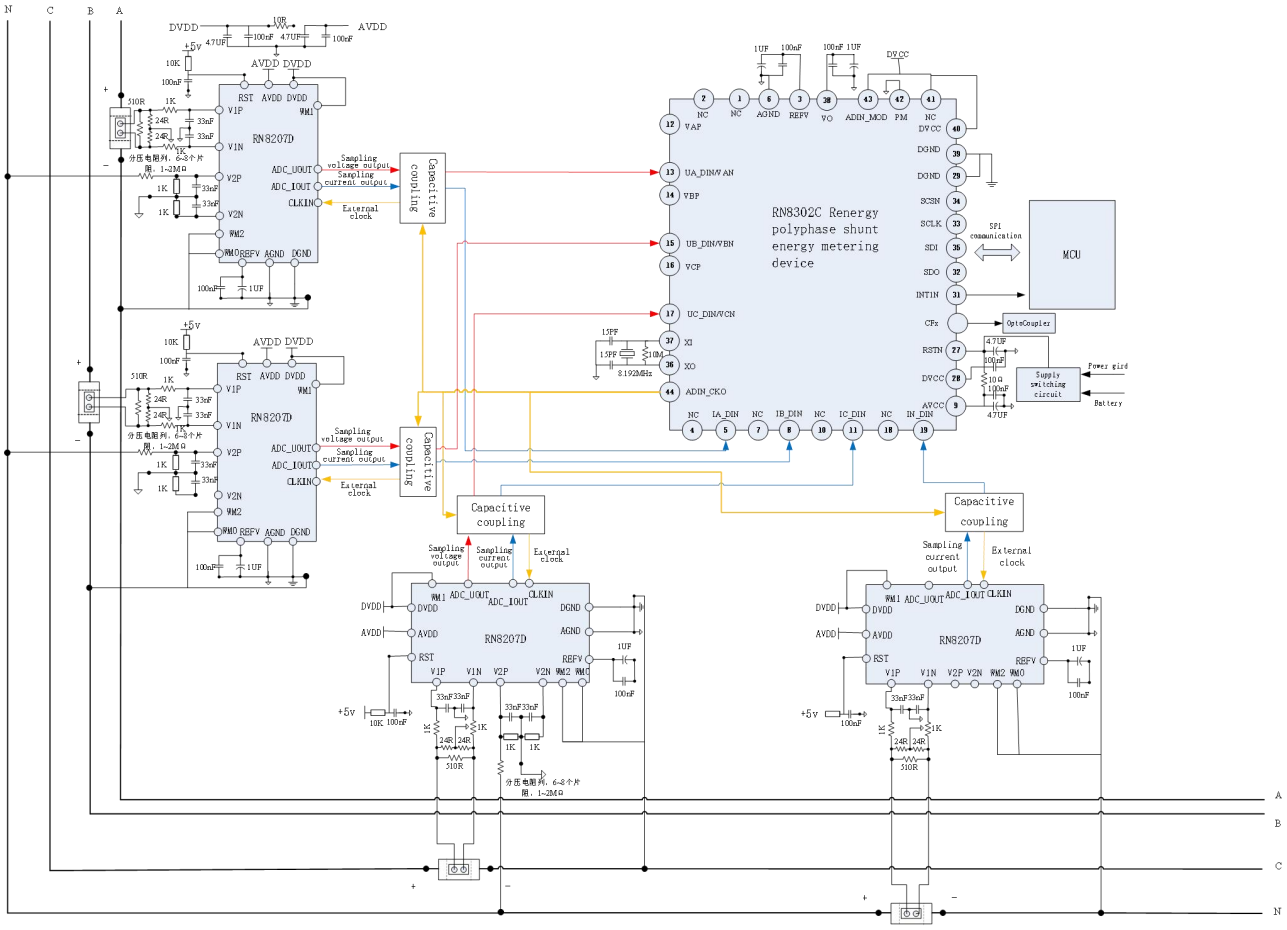


Figure 4-8 Diagram of RN8302C applied to three-phase shunt meter –case 2

In this case, current and voltage channels of RN8302C is total 7 sampling channels, and all of them use external ADC as inputs and sampling data processing circuits. Therefore, need to use four Renergy three-phase shunt meter ADC chips RN8207D, three of which are used for both voltage sampling and current sampling, and the other is used for neutral line current sampling. The ADC chip RN8207D required external clock, which from the RN8302C's ADIN_CKO to ensure that the clocks of the two chips are of the same source. The ADC chip RN8207D samples output, which is input from the RN8302C's IA_DIN, UA_DIN, IB_DIN, UB_DIN, IC_DIN, UC_DIN, and IN_DIN pins.

The hardware pin configuration of this case is the same as that of case 1: Require to configure the RN8302C metering mode at ADCIN mode by hardware. This is realized by configuring the ADIN_MOD pin to 1 and the PM pin to 0;

Software configuration: All 7 sampling channels of RN8302C are configured as external ADC sampling inputs, The register of RN8302C to configure the external ADC is the ADCIN mode configuration register (ADCIN_CFG), which is located in the Bank1 area at address 0xA1. ADCIN mode configuration register operation is WREN(0x180) and ADCIN_WREN(0x1A0) write-protected, and write-protected needs to be turned on before operation. The specific configuration method is that the host computer sends configuration commands to the RN8302C through SPI in turn.

1.Write 0xE5 to Bank1 register address 0x80H

2.Write 0xEA to Bank1 register address 0XA1H

3.Write 0x40 to Bank1 register address 0xA0H

After the software configuration is completed, the host computer is required to read the two-byte value of the Bank1 register address 0xA0H as 0x0040 through SPI to confirm that the software configuration is successful.

RN8207D need to be both voltage sampling output and current sampling output, each chip needs to be isolated, at this time the RN8302C to weak current as the ground, so customers can appropriately increase the isolation voltage of the capacitive couple to 5000V according to actual needs. The design here needs to pay attention to the fact that in the scenario where the RN8207D power-down ratio is faster than RN8302C, the 1-bit stream output by the ADC in the RN8207D will be a fixed value at the output of the capacitive coupling back-end to the RN8302C, and this fixed value, whether it is 1 or 0, represents the maximum value for the RN8302C, which may cause the phenomenon of pulsing without adding current when powering down. In practice, customers are required to circumvent this situation, and can control the power up and down sequence of hardware, or judge the power off and shutdown RN8302C in advance according to SAG on software, or handle it at the same time on software and hardware.

5 Electrical characteristics

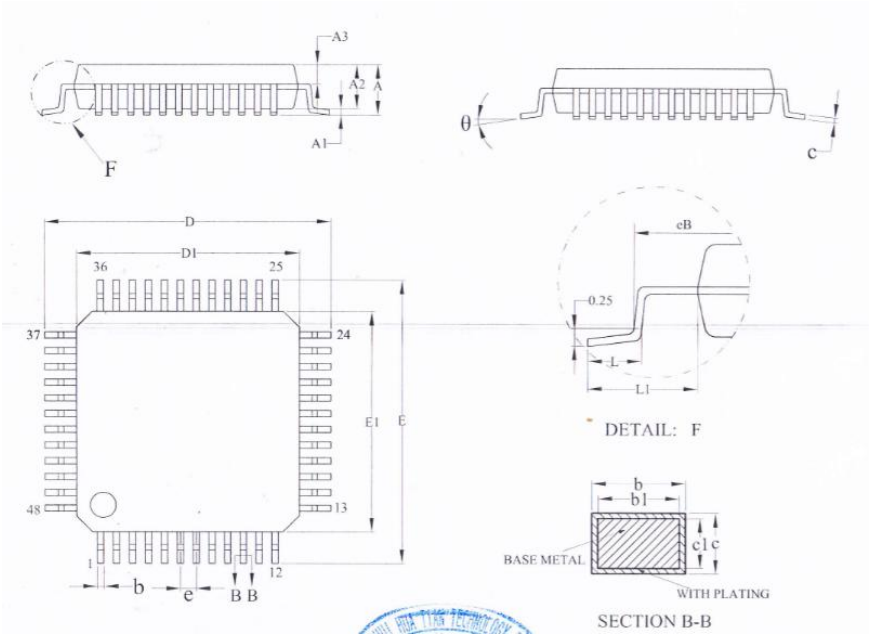
Parameter	Name	Min	Typ	Max	Unit	Test Conditions/Comments
Accuracy (DV_{CC}=AV_{CC}=3.3V±10%, room temperature)						
Active energy accuracy	Err	-0.1%		+0.1%		Dynamic range: 10000:1
Reactive energy accuracy	Err	-0.1%		+0.1%		Dynamic range: 10000:1
Apparent energy accuracy	Err	-0.1%		+0.1%		Dynamic range: 10000:1
Energy measurement bandwidth	BW		4		kHz	fosc=8.192MHz
RMS accuracy	RErr	-0.2%		+0.2%		Dynamic range: 1000:1
NVM1 RMS accuracy	NRErr	-0.5%		+0.5%		Dynamic range: 400:1
RMS measurement bandwidth	BW		4		kHz	fosc=8.192MHz
Phase angle accuracy	YErr	-0.02		+0.02	°	Current channel 50mV input, Phase angle 60°/120°/240°/300°
Frequency measurement resolution ratio			0.0001		Hz	40Hz~70Hz
Frequency accuracy	FErr	-0.02%		+0.02%		40Hz~70Hz
Calibration range						
Channel gain calibration factor	GS	0		2		
Channel phase calibration	PHS	-4.5		4.5	°	fosc=8.192MHz
Analog input						
Max Differential input signal level	V_{xpn}			830	mVp	Peak, PGA=1
-3dB bandwidth	B_{-3dB}		4		kHz	fosc=8.192MHz
SNR			88		dB	
THD			-80		dB	
CrossTalk			-110		dB	$U_{A/B/C}$=830mVpp
Offset voltage				500	μV	
Input impedance			270		kΩ	When PGA=1
Reference (DV_{CC}=AV_{CC}=3.3V±10%, temperature range: -40℃～+85℃)						
Output voltage	V_{ref}		1.25		V	1.25±1%
Temperature factor	T_c		5	15	ppm/℃	
Clock input						

Input clock frequency range	fxi		8.192		MHz	
XI input capacitor	Cxi		15		pf	
XO input capacitor	Cxo		15		pf	
Crystal oscillator ESR	ESR		100		Ω	10 times the starting vibration margin
Digital interface						
SPI interface rate				3.5M	bps	
HSDC interface rate				4.096M	bps	
SCLK/SCSN/SDI logic low level input	Vil			0.3Vcc	V	
SCLK/SCSN/SDI logic high level input	Vih	0.7Vcc			V	
CF1-CF5/INTN logic high level output	Voh	0.9Vcc			V	Isource=4.5mA(3.3V)
CF1-CF5/INTN logic low level output	Vol			0.1Vcc	V	Isink=7.4mA(3.3V)
Power Supply						
Analog	AVCC	3.0	3.3	3.6	V	
Digital	DVCC	3.0	3.3	3.6	V	
Reset						
POR	Vil			2.45	V	
	Vih	2.55			V	
	Time		20		ms	
BOR	Vil			2.7	V	
	Vih	2.8			V	
	Time		780		μs	
VDET	Vil			1.25	V	
	Vih	1.35			V	
SLM→NVM1	Wake-up reset time		1.5		ms	
SLM→EMM			1.5		ms	
NVM2→NVM1			1.5		ms	
NVM2→EMM			1.5		ms	
Consumption(DV_{CC}=AV_{CC}=3.3V±5%, room temperature)						
EMM current	Idd1	4.0	4.4	4.7	mA	fosc=8.192MHz Idd1=AIdd1+DIdd1, the same below
ADCIN current	Idd1	3.8	4.1	4.4	mA	fosc=8.192MHz Idd1=AIdd1+DIdd1, the same below
NVM1 current	Idd2		2.3		mA	OSCI=8.192MHz
NVM2 current	Idd3		150		μA	
SLM current	Idd4		1.4		μA	

No-voltage measurement typical operating current	Idd5		7		μA	60 seconds automatic wake-up measurement of three RMS currents
Limit parameters						
Digital supply	DVCC	-0.3	--	＋6	V	
Analog supply	AVCC	-0.3	--	＋6	V	
DV_{cc} to DGND		-0.3	--	＋3.7	V	
VO to DGND		-0.3		＋3	V	
DVCC to AVCC		-0.3		+0.3	V	
Analog differential input		-2		+2	V	
REFV input		-0.3		AVCC +0.3	V	
Digital input voltage relative to GND	V_{IND}	-0.3	--	DVCC +0.3	V	
Digital output voltage relative to GND	V_{outD}	-0.3	--	DVCC +0.3	V	
Operating temperature range	T_A	-40	--	85	℃	
Junction temperature	TJ		--	175	℃	
Storage Temperature Range	T_{stg}	-65	--	150	℃	
Reliability						
Electrostatic Discharge (ESD)	HBM		±8000		V	Perform on all pins according to standard JEDEC EIA/JESD22-A114
	MM		±2000		V	Perform on all pins according to standard JEDEC EIA/JESD22-A115C
Moisture sensitivity	MSD		3 level		/	Evaluate according to standard IPC/JEDEC J-STD-020D.1

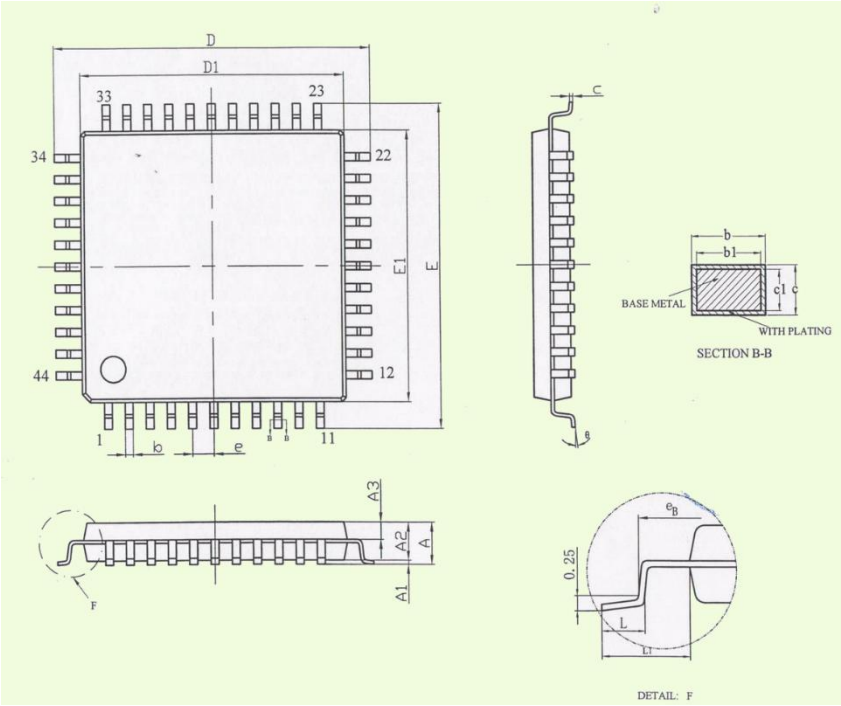
6 Packaging

6.1 LQFP48 outline demensions



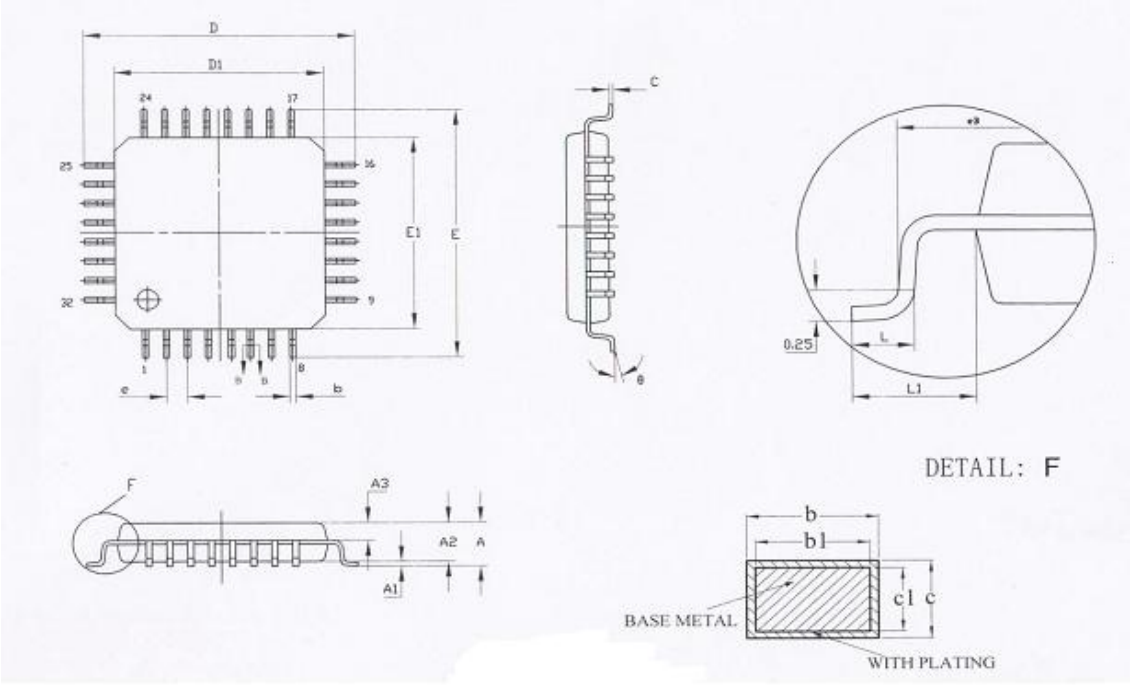
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

6.2 LQFP44 outline demensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.29	—	0.37
b1	0.28	0.30	0.33
c	0.13	—	0.18
c1	0.12	0.127	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
e_B	11.25	—	11.45
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	7°
L/F载体尺寸 (mil)	122*122		160*110
	180*180		205*205

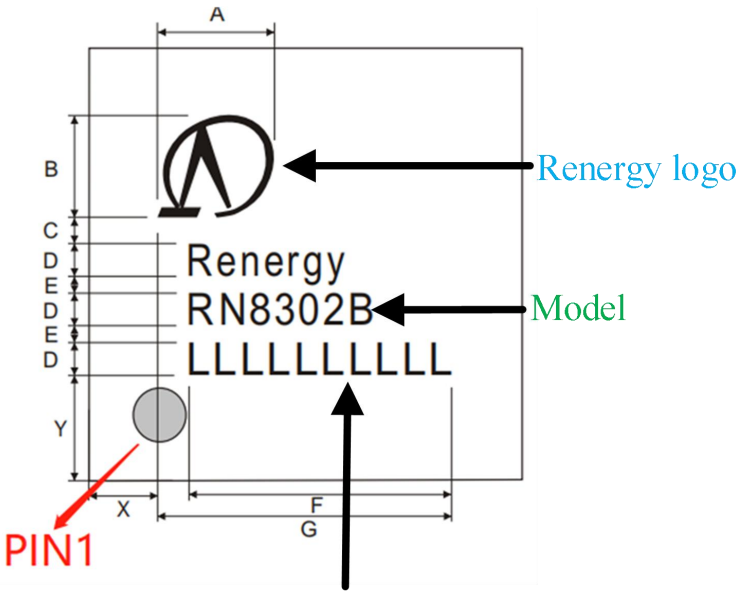
6.3 LQFP32 outline demensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	—	0.43
b1	0.31	0.35	0.39
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.40	—	0.65
L1	1.00BSC		
θ	0°	—	7°
L/F载体尺寸 (mil)	150*150		
	205*205		

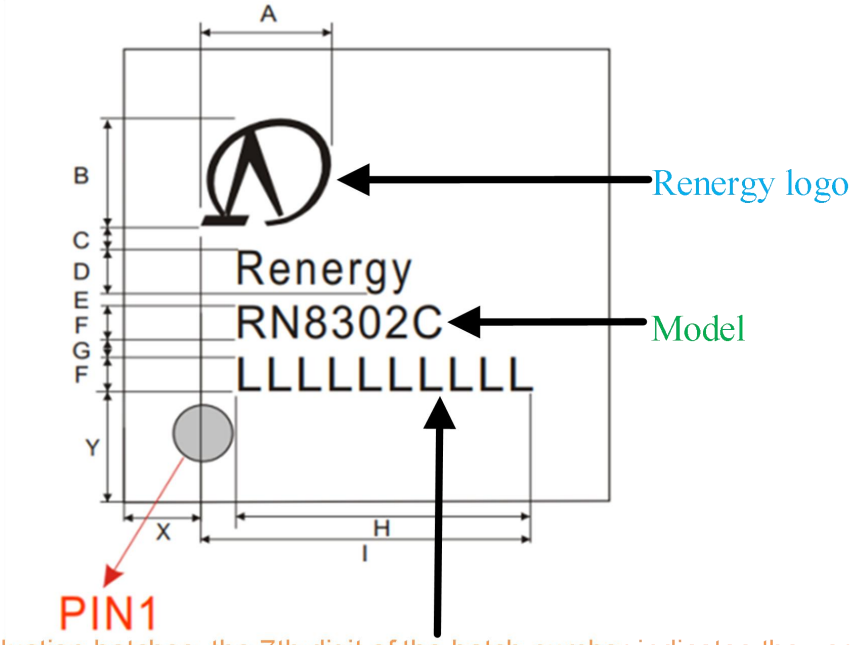
7 Appearance

7.1 RN8302B



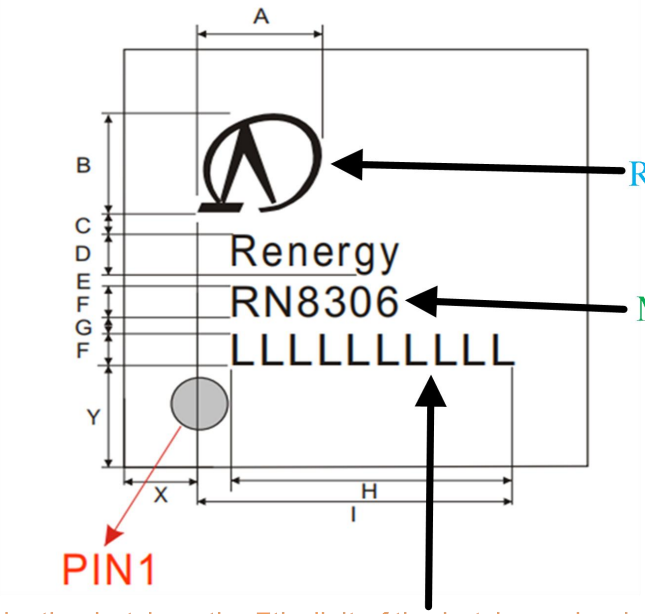
Production batches, the 7th digit of the batch number indicates the version number, and the 7th digit of C indicates the V3 version.

7.2 RN8302C



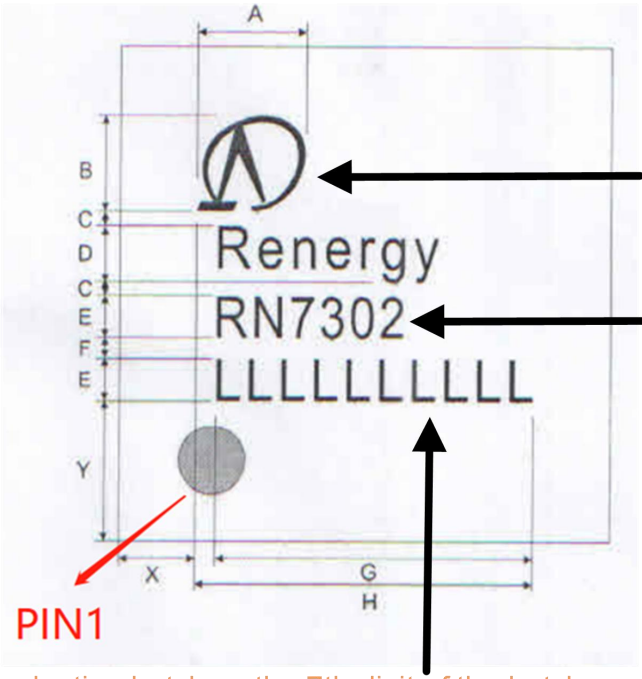
Production batches, the 7th digit of the batch number indicates the version number, and the 7th digit of C indicates the V3 version.

7.3 RN8306



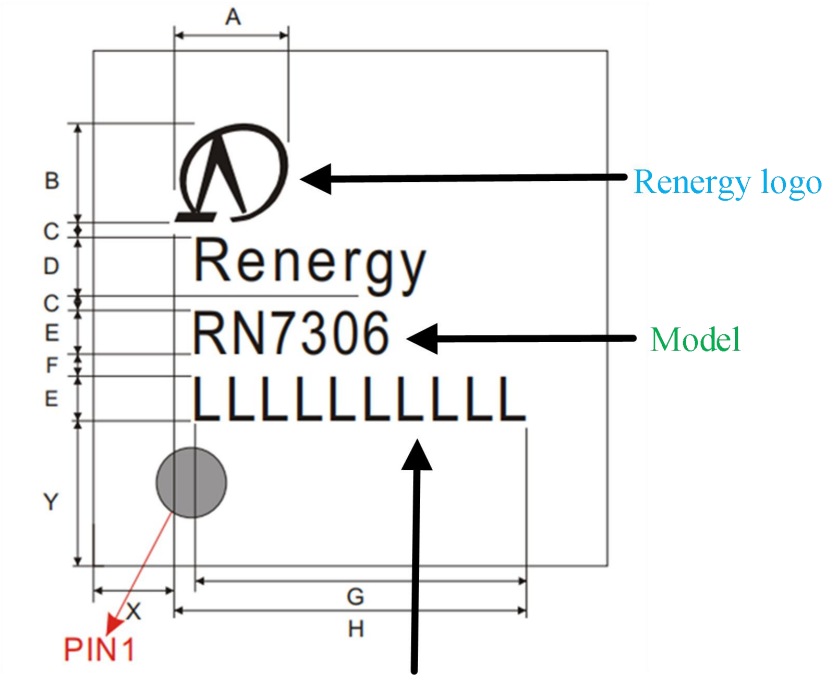
Production batches, the 7th digit of the batch number indicates the version number, and the 7th digit of C indicates the V3 version.

7.4 RN7302



Production batches, the 7th digit of the batch number indicates the version number, and the 7th digit of C indicates the V3 version.

7.5 RN7306



Production batches, the 7th digit of the batch number indicates the version number, and the 7th digit of C indicates the V3 version.