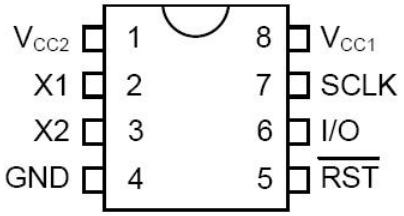
RoHS , Green Package, Lead Free
Package: SOIC8/SOP8/DIP8

■ Features

1、Real time clock counts seconds, minutes, hours, date of the month, day of the week, and year with leap year compensation valid up to 2100
2、31X8 RAM；
3、Serial I/O for minimum pin count；
4、2~5.5V full operation;
5、Consumes less than 300nA at 2.5V or below;
6、Single byte or multiple byte data transfer;
7、SOIC8, SOP8, or DIP8
8、Simple 3-wire interface；
9、TTL compatible；
10、Optional industrial temperature range：-40℃～85℃

■ Pin Descriptions



Pin Number	Pin Name	Function	I/O
1	VCC2	Power supply pin	P
2	X1	32.768kHZ crystal input	I
3	X2	32.768kHZ crystal output	O
4	GND	GND	P
5	RST	Reset pin	I
6	I/O	I/O pin	I/O
7	SCLK	Clock pin	I
8	VCC1	Power supply pin	P

■ Characteristics

Absolute Maximum Ratings:

＃Voltage on any pin realtive to GND：-0.5V~7.0V；

＃Operating temperature：-40℃～85℃

＃Storage temperature：-55℃~125℃；

Recommended DC Operating Conditions：(-40℃~85℃)

Parameters	Condition	Min	Typ	Max	Unit
VCC1，VCC2		2		5.5	V
Logic 1 Input		2.0		VCC+0.3	V
Logic 0 Input	VCC=2V	-0.2		+0.3	V
	VCC=5V	-0.3		+0.8	V

DC Electrical Characteristics：(-40℃~85℃)（VCC=2~5.5V）

Parameters	Symbol		Min	Tpy	Max	Unit
Input Leakage	ILI				500	uA
I/O Leakage	ILO				500	uA
Logic 1 Output	VOH	VCC=2V	1.6			V
		VCC=5V	2.4			V
Logic 0 Output	VOL	VCC=2V			0.4	V
		VCC=5V			0.4	V
Active Supply Current	ICC1A	VCC=2V			0.3	mA
		VCC=5V			1.2	mA
Timekeeping current	ICC1T	VCC=2V			0.3	uA
		VCC=5V			1	uA
Standby Current	ICC1S	VCC=2V		100		nA
		VCC=5V		100		nA
Active Supply Current	ICC2A	VCC=2V			0.4	mA
		VCC=5V			1.28	mA
Timekeeping current	ICC2T	VCC=2V			25	uA
		VCC=5V			81	uA
Standby Current	ICC2S	VCC=2V			25	uA
		VCC=5V			80	uA

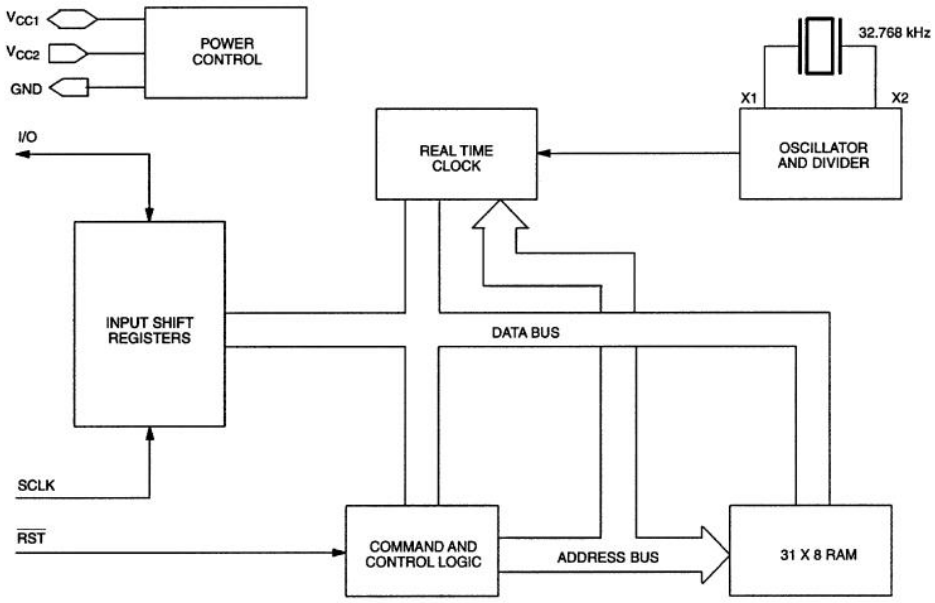
AC Electrical Characteristics：(-40℃~85℃)（VCC=2~5.5V）

Parameters	Symbol		Min	Tpy	Max	Unit
Clock Frequency	FCLK	VCC=2V			0.5	MHZ
		VCC=5V			2	

■ Descriptions

The SLM1302 Trickle Charge Timekeeping Chip contains a real time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator.
Interfacing the SLM1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) RST (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock).

■ Block Diagram



■ Operation

1. Command Byte:

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A4	A3	A2	A1	A0	RD / $\overline{W}$

Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is 0, writes to the SLM1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic. The command byte is always input starting with the LSB (bit 0).

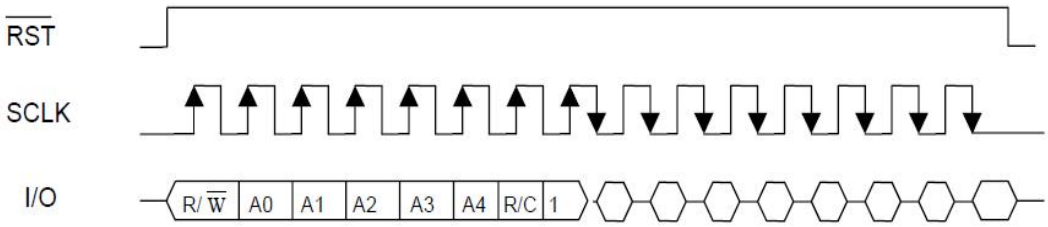
2. Reset and Clock Control:

All data transfers are initiated by driving the RST input high. The RST input serves two functions. First, RST turns on the control logic which allows access to the shift register for the address/command sequence. Second, the RST signal provides a method of terminating either single byte or multiple byte data transfer.

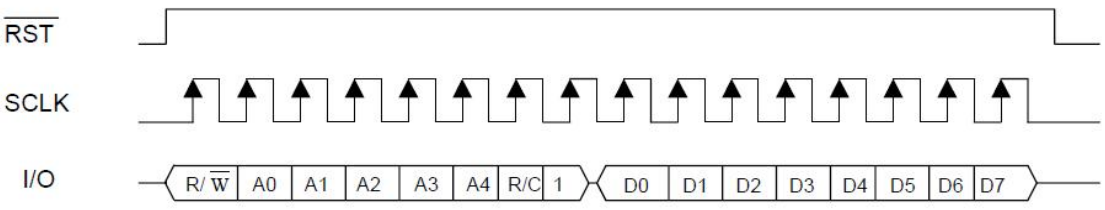
A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the RST input is low all data transfer terminates and the I/O pin goes to a high impedance state. At power–up, RST must be a logic 0 until VCC > 2.0 volts. Also SCLK must be at a logic 0 when RST is driven to a logic 1 state.

3. Data Transfer Summary:

Single Byte Read



Single Byte Write



4. Register Address/Definition:

All the time information is included in the following 7 registers

Register Address：

SEC	1	0	0	0	0	0	0	RD / $\overline{W}$

Register Definition：

00－59	CH	10 SEC	SEC

Register Address：

MIN	1	0	0	0	0	0	1	RD / $\overline{W}$

Register Definition：

00－59	0	10 MIN	MIN

Register Address：

HR	1	0	0	0	0	1	0	RD / $\overline{W}$

Register Definition：

01－12 00－23	12/24	0	10 A/P	HR	HR

Register Address：

DATE	1	0	0	0	0	1	1	RD / $\overline{W}$

Register Definition：

01-28/29 01- 30 01-31	0	0	10 DATE	DATE

Register Address：

MONTH	1	0	0	0	1	0	0	RD / $\overline{W}$

Register Definition：

01-12	0	0	0	10 M	MONTH

Register Address：

DAY	1	0	0	0	1	0	1	RD / $\overline{W}$

Register Definition：

01-07	0	0	0	0	0	DAY

Register Address：

YEAR	1	0	0	0	1	1	0	RD / $\overline{W}$

Register Definition：

00-99	10 YEAR	YEAR

5. Clock Halt Flag

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock

oscillator is stopped and the SLM1302 is placed into a low–power standby mode with a current drain of less than 100nA. When this bit is written to logic 0, the clock will start. The initial power on state is not defined.

6. AM-PM/12-24 Mode:

Bit 7 of the hours register is defined as the 12 or 24 hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10-hour bit (20 – 23 hours).

7. Write Protection:

Write Protection Register Address：

1	0	0	0	1	1	1	RD / $\overline{W}$

Register Definition：

WP	0	0	0	0	0	0	0

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0 – 6) are forced to 0 and will always read a 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write protect bit prevents a write operation to any other register. The initial power on state is not defined. Therefore the WP bit should be cleared before attempting to write to the device.

8. Trickle Charge Register

Trickle Charge Register Address：

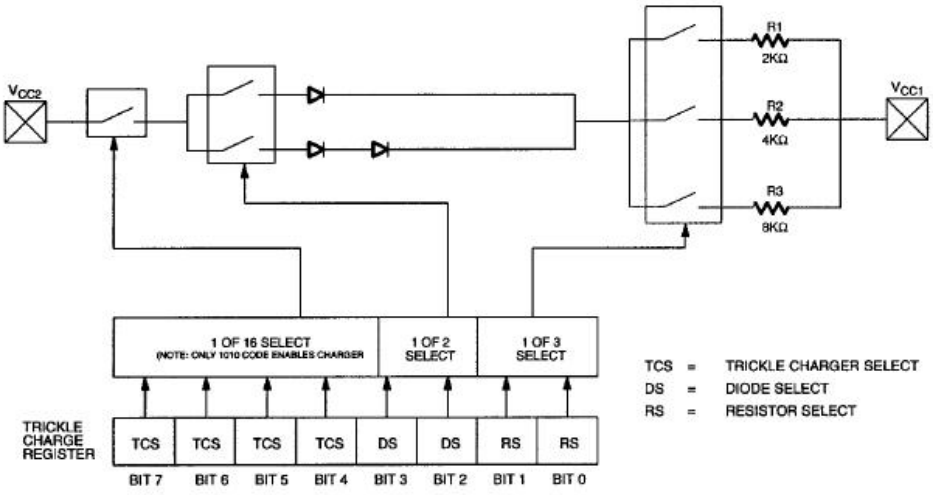
1	0	0	1	0	0	0	RD / $\overline{W}$

Register Definition：

TCS	TCS	TCS	TCS	DS	DS	RS	RS

This register controls the trickle charge characteristics of the SLM1302. The trickle charge select (TCS) bits (bits4 -7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The SLM1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 – 3) select

whether one diode or two diodes are connected between VCC2 and VCC1. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0 -1) select the resistor that is connected between VCC2 and VCC1. No resistor is connected if RS is 00. If RS is 01, 2k resistor is selected; 10 means 4k resistor is selected; 11 means 8k resistor is selected.



8. Clock/Calendar Burst Mode

Clock Burst Register Address：

1	0	1	1	1	1	1	RD / $\overline{W}$

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written starting with bit 0 of address 0.

9. RAM Burst Mode

Register Address：

RAM0	1	0	1	1	1	1	1	RD / $\overline{W}$

RAM30	1	0	1	1	1	1	1	RD / $\overline{W}$

Register Definition：

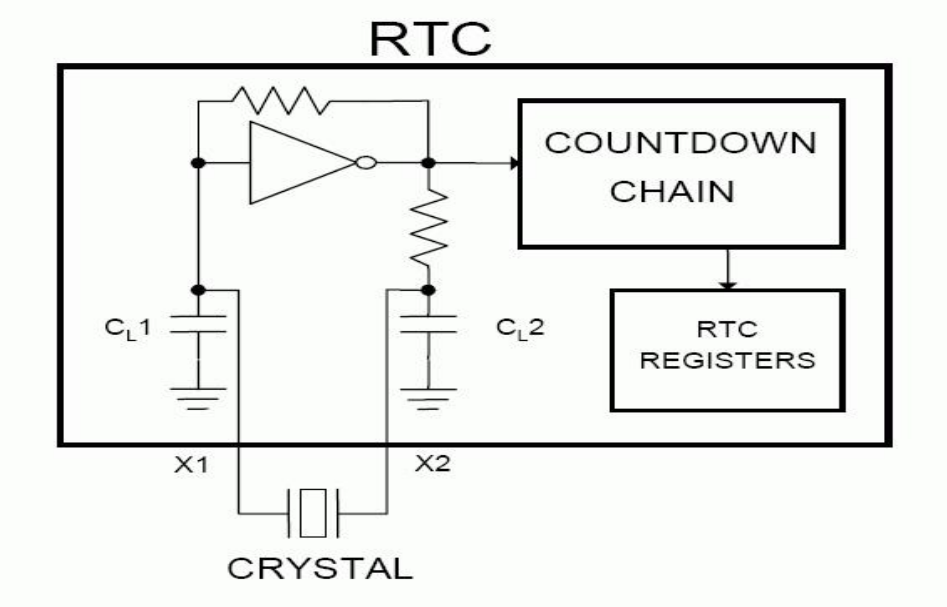
RAM DATA0								
⋮								
RAM DATA30								

RAM Burst Register Address：

1	1	1	1	1	1	1	RD / $\overline{W}$

10. Crystal Selection

Crystal with a oscillator frequency of 32.768kHZ is required for the SLM1302, and the load capacitance (CL) of the crystal should be 6pF.



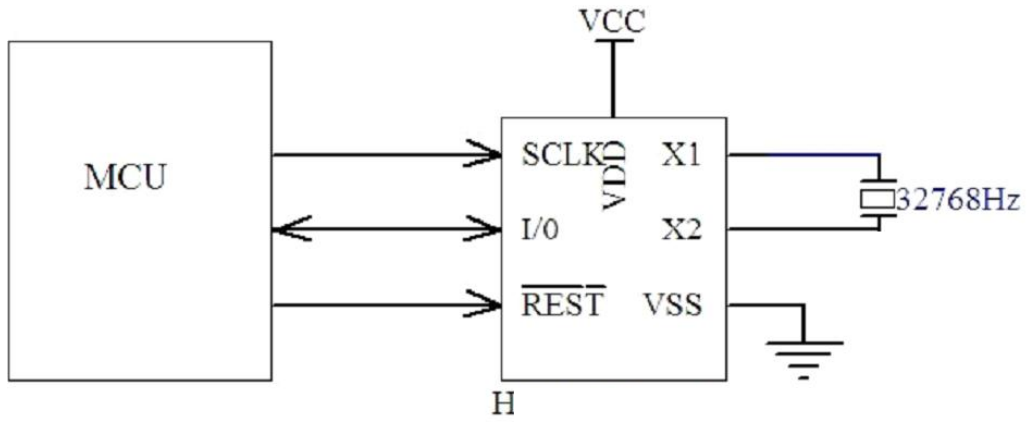
11. Power Supply (VCC1 and VCC2)

VCC1 provides low power operation in single supply and battery operated systems as well as low power battery backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

Vcc2 is the primary power supply pin in a dual supply configuration. VCC1 is connected to a backup source to maintain the time and date in the absence of primary power.

The SLM1302 will operate from the larger of VCC1 or VCC2. When VCC2 is greater than VCC1 + 0.2V, VCC2 will power the SLM1302. When VCC2 is less than VCC1, VCC1 will power the SLM1302.

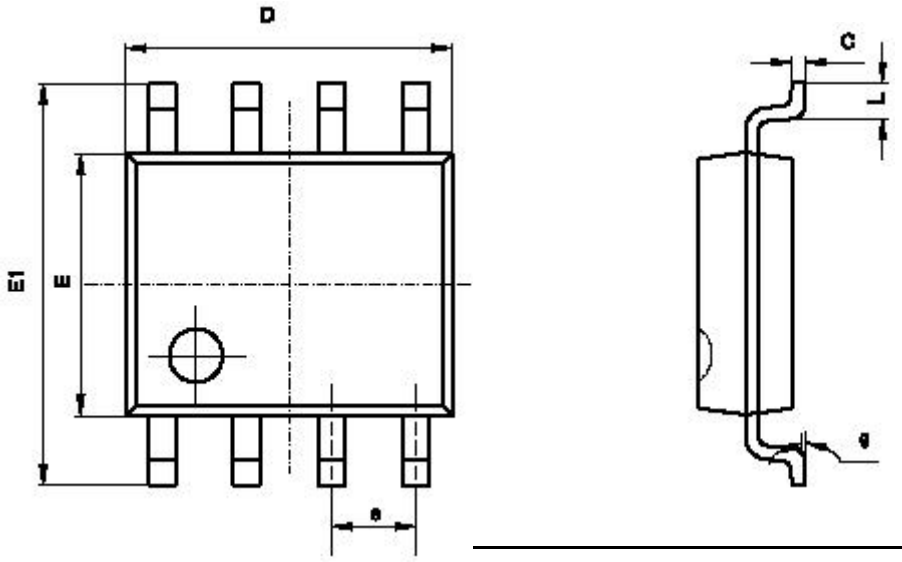
■ Typical Application

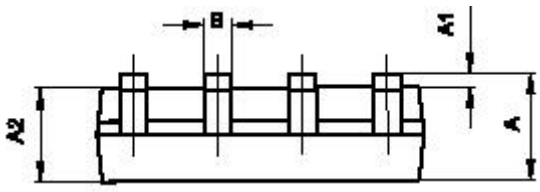


SLM1302

■ Package

SOIC8 150MIL





Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	4.780	5.000
E	3.800	4.000
E1	5.800	6.300
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°