36 V, Latch-Up Immune, 4-/8-Channel, Precision Analog Multiplexers

Features

- Latch-Up Immune for all pins
- Break-Before-Make Construction
- Fast Switching Time: t_{ON} 166 nS; t_{OFF} 135 nS
- Low On Resistance: 270 Ω
- Off Leakage Current: 10 pA
- Charge Injection: 14.8 pC
- TTL and CMOS-Compatible Inputs
- Supply Voltage: ±5 V to ±18 V
- Specified Temperature Range: -40 °C to 125 °C
- ESD: 8 kV HBM

Applications

- Analog Input/Output Module
- Industrial and Process Control Systems
- Instruments
- ATE
- Communication Systems
- Relay Replacement

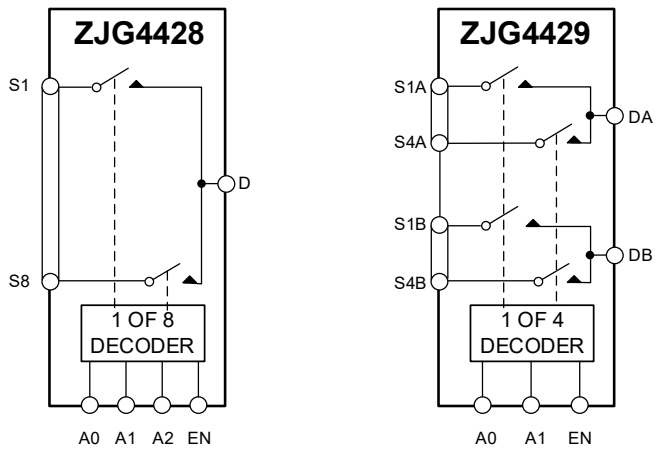
General Description

The ZJG4428 and ZJG4429 are analog multiplexers, with the ZJG4428 comprising eight single channels and the ZJG4429 comprising four differential channels. The ZJG4428 switches one of eight inputs to a common output as determined by the 3-bit binary address lines, A0, A1, and A2. The ZJG4429 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines, A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched off. They support bidirectional analog and digital signals on the source (Sx) and drain(D) pins.

The ZJG4428 and ZJG4429 provide latch-up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows the ZJG4428 and ZJG4429 to be used in harsh environments.

The ZJG4428 and ZJG4429 are available in SOIC-16 and TSSOP-16 packages and are pin compatible with industry standards.

Functional Block Diagram



Typical Application

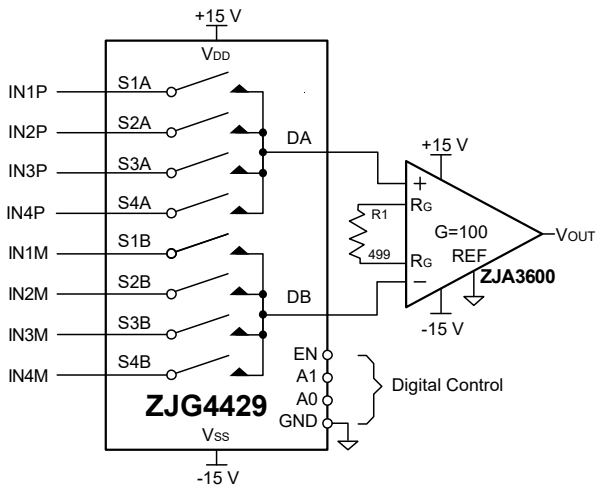


Table of Contents

Revision History (Release B) [1]

Jan. 2025 — Release B

English Version

Added TSSOP-16 Pin Configuration, Terminology and Test Circuits

Updated Specifications, Ordering Guide, Product Order Model and Related Parts

Sep. 2024

Updated Specifications, Ordering Guide, Product Order Model and Related Parts

Apr. 2024 — Release A

Mar. 2023 — Initial

[1] Information furnished by ZJW Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by ZJW Microelectronics for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of ZJW Microelectronics. Trademarks and registered trademarks are the property of their respective owners.

Pin Configuration and Function Description

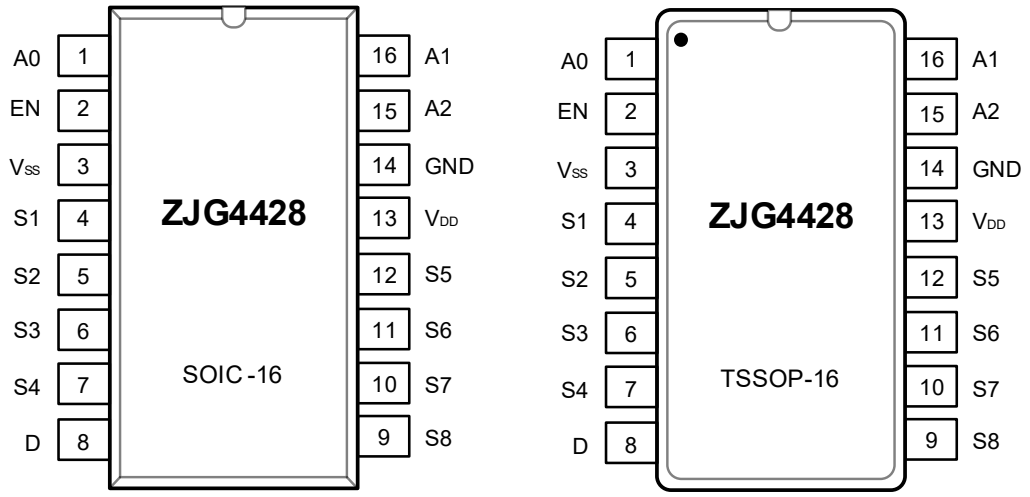


Figure 1. ZJG4428 Pin Configuration (SOIC-16 & TSSOP-16)

Mnemonic	Pin No.	Description
A0	1	Logic Control Input LSB.
EN	2	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
V_{SS}	3	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
S1	4	Source Terminal 1. This pin can be an input or an output.
S2	5	Source Terminal 2. This pin can be an input or an output.
S3	6	Source Terminal 3. This pin can be an input or an output.
S4	7	Source Terminal 4. This pin can be an input or an output.
D	8	Drain Terminal. This pin can be an input or an output.
S8	9	Source Terminal 8. This pin can be an input or an output.
S7	10	Source Terminal 7. This pin can be an input or an output.
S6	11	Source Terminal 6. This pin can be an input or an output.
S5	12	Source Terminal 5. This pin can be an input or an output.
V_{DD}	13	Most Positive Power Supply Potential.
GND	14	Ground (0 V) Reference.
A2	15	Logic Control Input MSB.
A1	16	Logic Control Input.

ZJG4428 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

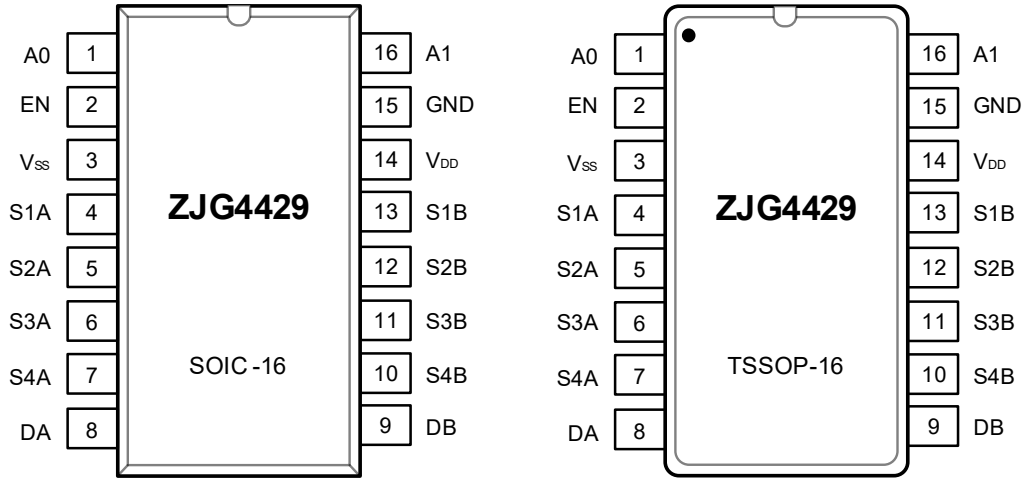


Figure 2. ZJG4429 Pin Configuration (SOIC-16 & TSSOP-16)

Mnemonic	Pin No.	Description
A0	1	Logic Control Input LSB.
EN	2	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
V_{SS}	3	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
S1A	4	Source Terminal 1A. This pin can be an input or an output.
S2A	5	Source Terminal 2A. This pin can be an input or an output.
S3A	6	Source Terminal 3A. This pin can be an input or an output.
S4A	7	Source Terminal 4A. This pin can be an input or an output.
DA	8	Drain Terminal A. This pin can be an input or an output.
DB	9	Drain Terminal B. This pin can be an input or an output.
S4B	10	Source Terminal 4B. This pin can be an input or an output.
S3B	11	Source Terminal 3B. This pin can be an input or an output.
S2B	12	Source Terminal 2B. This pin can be an input or an output.
S1B	13	Source Terminal 1B. This pin can be an input or an output.
V_{DD}	14	Most Positive Power Supply Potential.
GND	15	Ground (0 V) Reference.
A1	16	Logic Control Input MSB.

ZJG4429 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Input Voltage	V_{SS} - 0.5 V ~ V_{DD} + 0.5 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature	-65 °C to 150 °C
Maximum Reflow Temperature [2]	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	8 kV
Charged Device Model (CDM) [5]	2 kV

Thermal Resistance [6]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-16	94	23.5	°C/W
TSSOP-16	104	60	°C/W

1 These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2 IPC/JEDEC J-STD-020 Compliant.

3 Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

4 ANSI/ESDA/JEDEC JS-001 Compliant.

5 ANSI/ESDA/JEDEC JS-002 Compliant.

6 θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at V_{DD} = 15 V ± 10%, V_{SS} = -15 V ± 10%, GND = 0 V, T_A = 25 °C.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ANALOG SWITCH							
Analog Signal High		Output open circuit			V_{DD} - 1.4		V
Analog Signal Low					V_{SS} + 1.4		V
Analog Signal High		Output loaded, 1 mA			V_{DD} - 2.2		V
Analog Signal Low					V_{SS} + 2.2		V
On Resistance	R_{ON}	-10 V ≤ V_S ≤ +10 V, I_S = 1 mA, V_{DD} = 15 V, V_{SS} = -15 V	●		270	530	Ω
		-40 °C < T_A < 85 °C				430	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	-10 V ≤ V_S ≤ +10 V, I_S = 1 mA, V_{DD} = 15 V, V_{SS} = -15 V			5	7	%
			●			10	%
		-40 °C < T_A < 85 °C				10	%
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±10 V, I_S = 1 mA	●		0.5	3	%
LEAKAGE CURRENTS							
Source Off Leakage	I_S (Off)	V_S = ±10 V, V_D = ∓10 V		-0.5	±0.01	+0.5	nA
			●	-4		+4	nA
		-40 °C < T_A < 85 °C		-1		1	nA
Drain Off Leakage	I_D (Off)	V_S = ±10 V, V_D = ∓10 V		-0.5	±0.01	+0.5	nA
			●	-0.2		+0.2	μA
		-40 °C < T_A < 85 °C		-4		4	nA
Channel On Leakage	I_D,I_S(ON)	V_S = V_D = ±10 V		-0.5	±0.01	+0.5	nA
			●	-0.2		+0.2	μA
		-40 °C < T_A < 85 °C		-4		4	nA
DIGITAL INPUTS							
Input High Voltage	V_{INH}		●	2.4			V
Input Low Voltage	V_{INL}		●			0.8	V
Input Current	I_{INL}/I_{INH}	V_{EN} = 0 V or V_{DD}	●			1	μA
DYNAMIC CHARACTERISTICS [1]							
$t_{TRANSITION}$		R_L = 1 MΩ, C_L = 35 pF, V_{S1} = ±10 V, V_{S8} = ±10 V	●		168	320	ns
t_{OPEN}		R_L = 1 KΩ, C_L = 35 pF, V_S = 5 V	●	50	139		ns
t_{ON}		R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V	●		166	330	ns
t_{OFF}		R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V	●		135	170	ns
Settling Time		t_{SETT} 0.1%, R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V			0.25		μs

[1] Guaranteed by design, not subject to production test.

Charge Injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF			14.8		pC
Off Isolation		R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz, V_S = 7 Vrms			-93		dB
Channel-to-Channel Crosstalk		R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz, V_S = 7 Vrms			-104		dB
C_S (Off)					2.6		pF
C_D (Off)		ZJG4428			5.8		pF
		ZJG4429			3.2		pF
POWER SUPPLY							
I_{DD_ON}, I_{SS_ON}		V_{DD} = 15 V, V_{SS} = -15 V, V_{EN} = 2.4 V			0.07	0.15 0.2	mA mA
			•				
I_{DD_OFF}, I_{SS_OFF}		V_{DD} = 15 V, V_{SS} = -15 V, V_{EN} = 0.8 V			0.05	0.15 0.2	mA mA
			•				
Power Supply Range				±5		±18	V
TEMPERATURE RANGE							
Specified				-40		125	ºC

Typical Performance Characteristics

Unless otherwise stated, V_{DD} = 15 V, V_{SS} = -15 V, GND = 0 V, T_A = 25 °C.

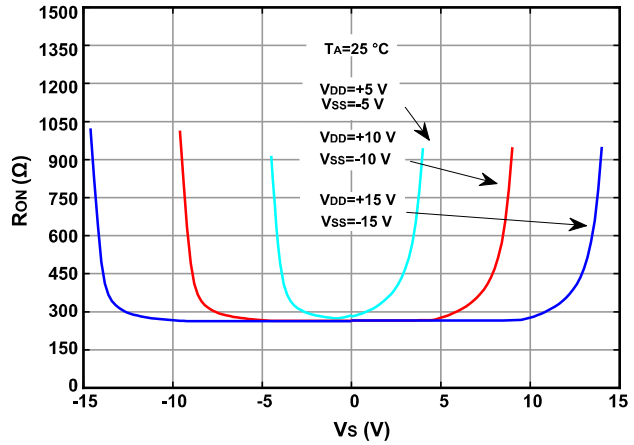


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures

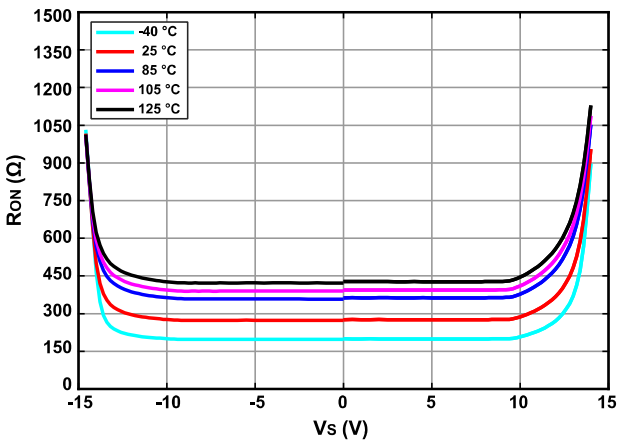


Figure 4. On Resistance as a Function of V_D (V_S)

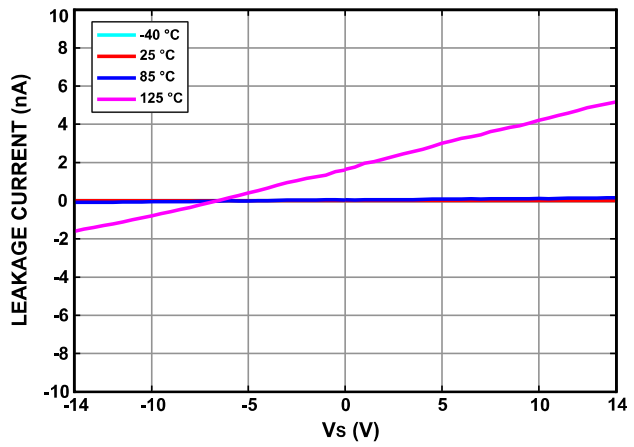


Figure 5. Source Input Leakage Current as a Function of V_S for Different Temperatures (Power Supplies On)

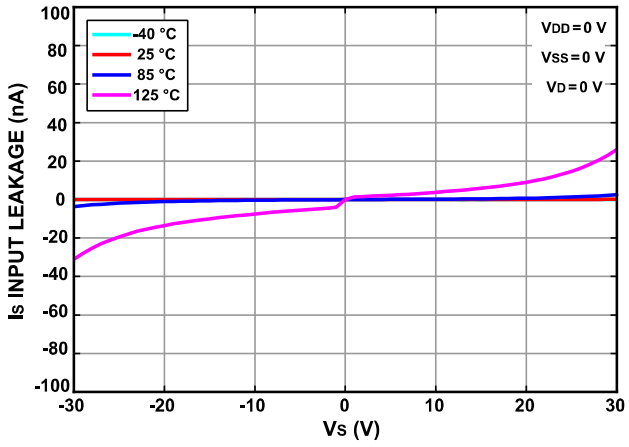


Figure 6. Source Input Leakage Current as a Function of VS for Different Temperatures (Power Supplies Off)

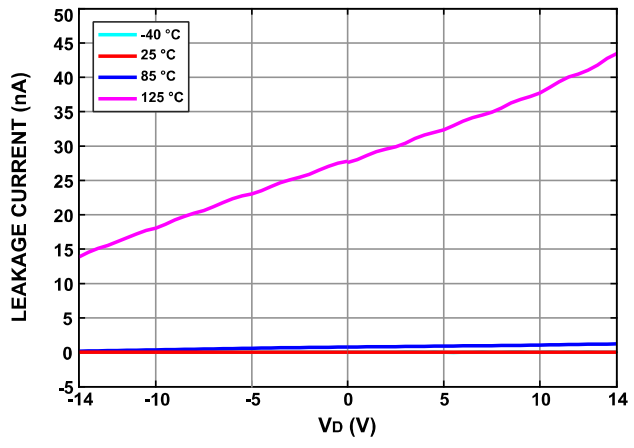


Figure 7. Leakage Current I_D (on) as a Function of V_D for Different Temperatures

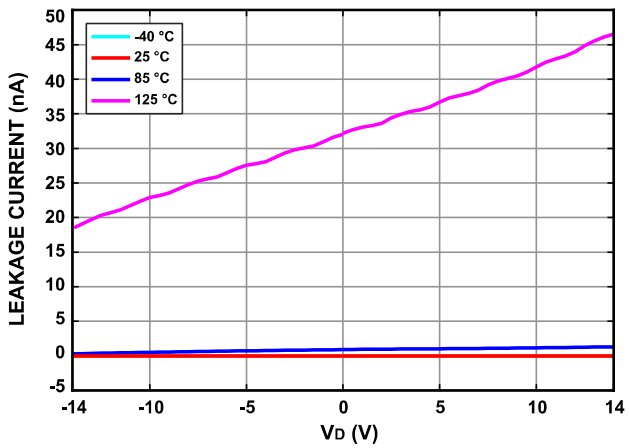


Figure 8. Leakage Current I_D (off) as a Function of V_D for Different Temperatures

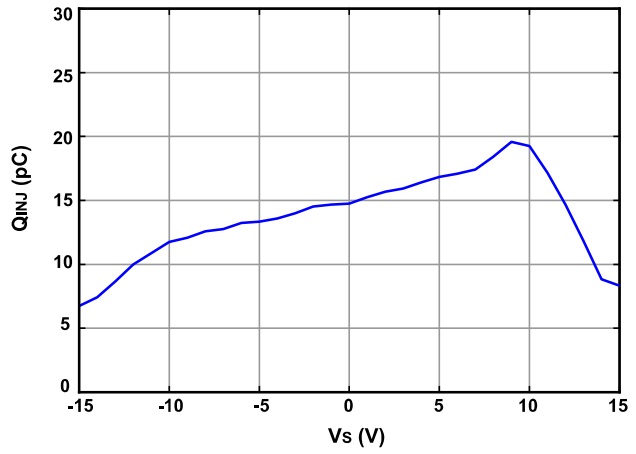


Figure 9. Charge Injection vs. Source Voltage

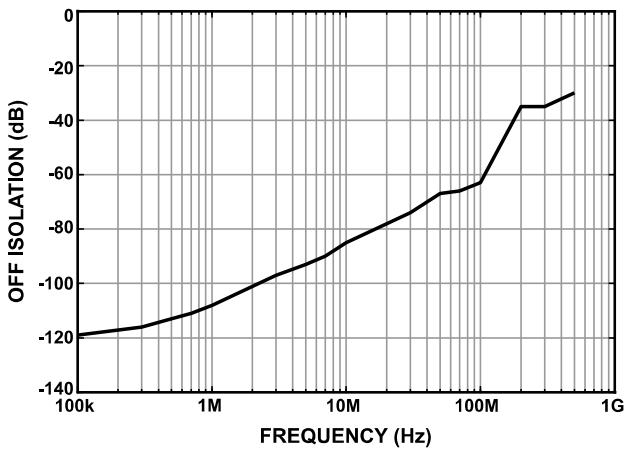


Figure 10. Off Isolation vs. Frequency

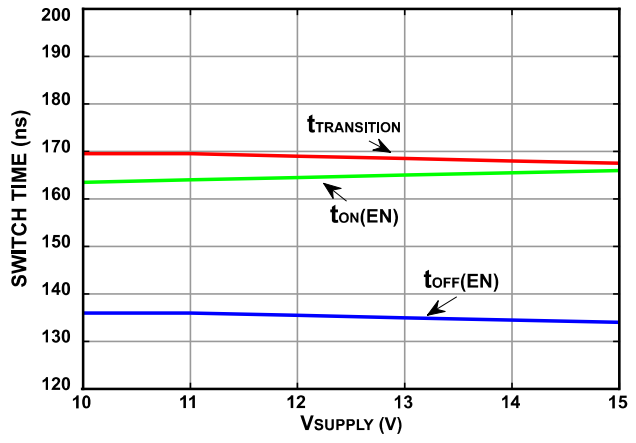


Figure 11. Switching Time vs. Dual Power Supply

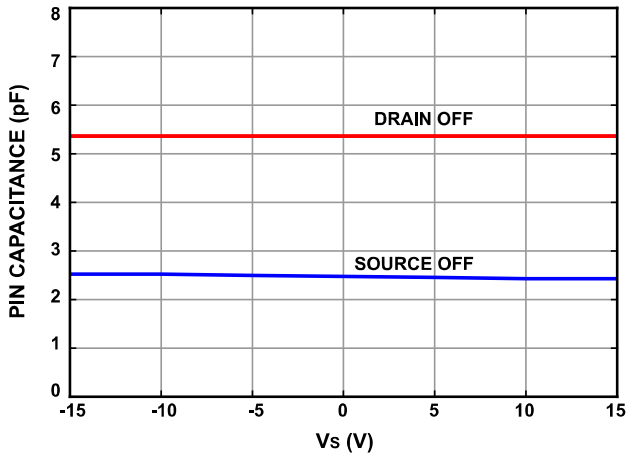


Figure 12. Capacitance vs. Source Voltage

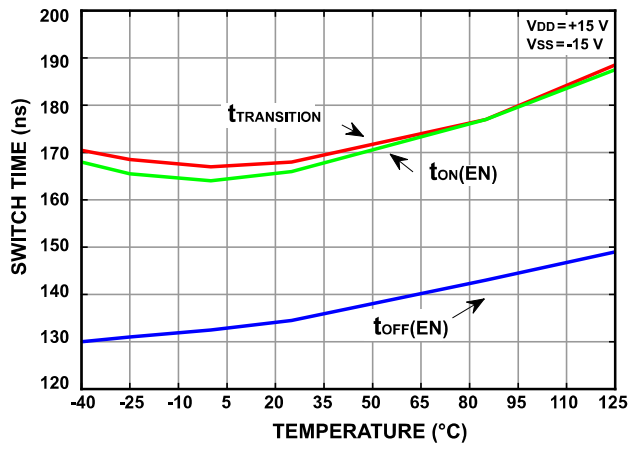


Figure 13. Switching Time vs. Temperature

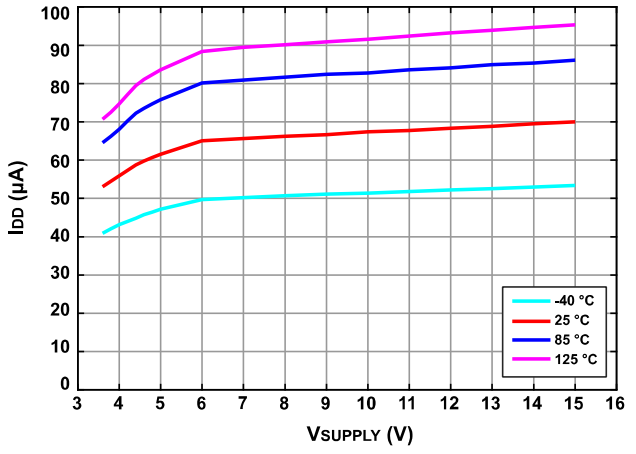


Figure 14. Supply Current vs Supply Voltage for Different Temperatures (EN = 1)

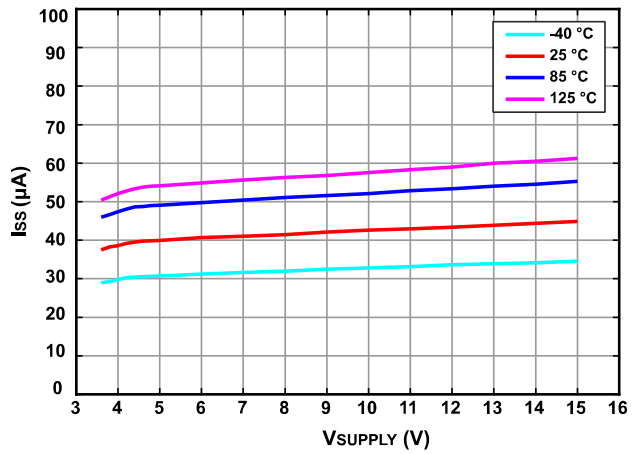


Figure 15. Supply Current vs Supply Voltage for Different Temperatures (EN = 0)

Terminology

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels as a percentage of the maximum R_{ON} of those two channels.

$R_{FLAT\ (ON)}$
Flatness is defined as the difference between the maximum and minimum value of the on resistance measured over the specified analog signal range and is represented by $R_{FLAT\ (ON)}$.

Flatness is calculated by

$$\left((R_{MAX} - R_{MIN})/R_{MAX} \times 100\right)$$

R_{ON} Drift
Change in R_{ON} when temperature changes by one degree Celsius.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

I_S (Fault—Power Supplies On)
Source leakage current when exposed to an overvoltage condition.

I_D (Fault—Power Supplies On)
Drain leakage current when exposed to an overvoltage condition.

I_S (Fault—Power Supplies Off)
Source leakage current with power supplies off.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 80% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Test Circuits

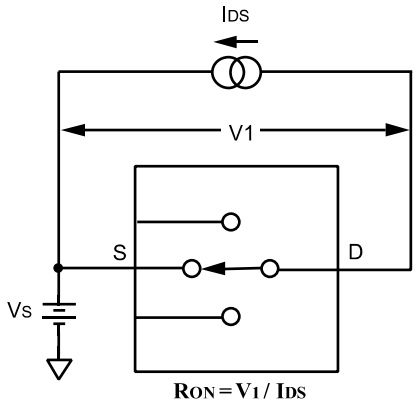


Figure 16. On Resistance

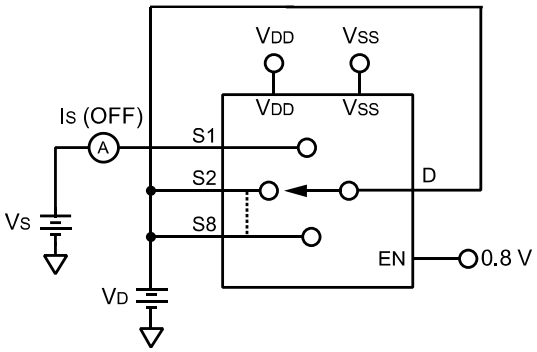


Figure 17. I_S (Off)

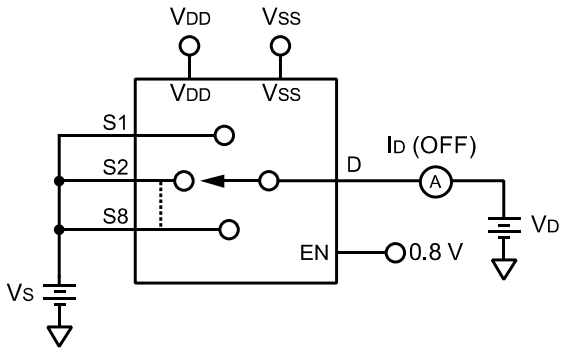


Figure 18. I_D (Off)

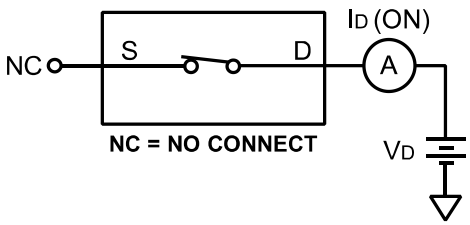


Figure 19. I_D (On)

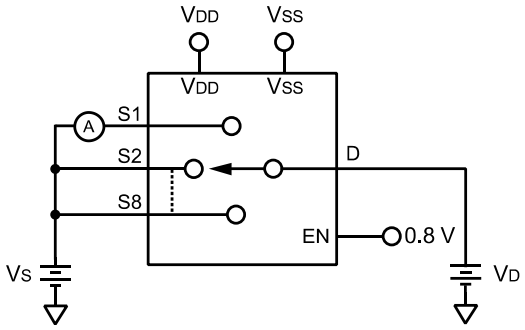


Figure 20. Input Leakage Current (with Overvoltage)

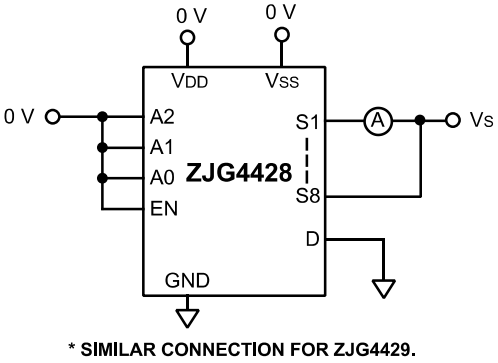


Figure 21. Input Leakage Current (with Power Supplies Off)

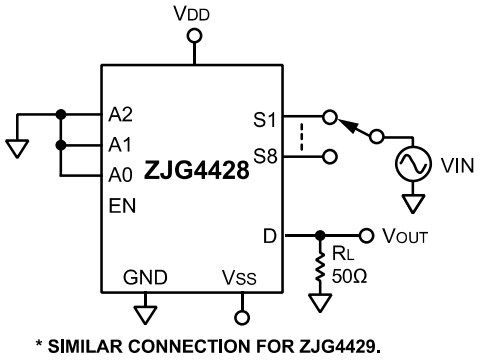


Figure 22. Off Isolation

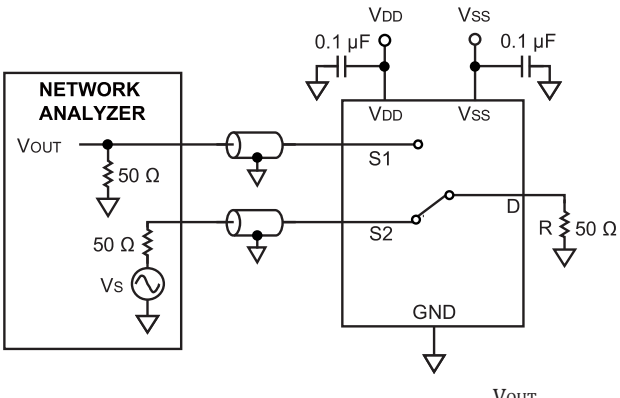
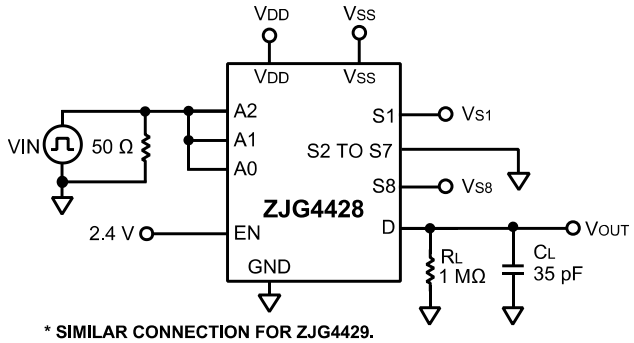


Figure 23. Channel-to-Channel Crosstalk



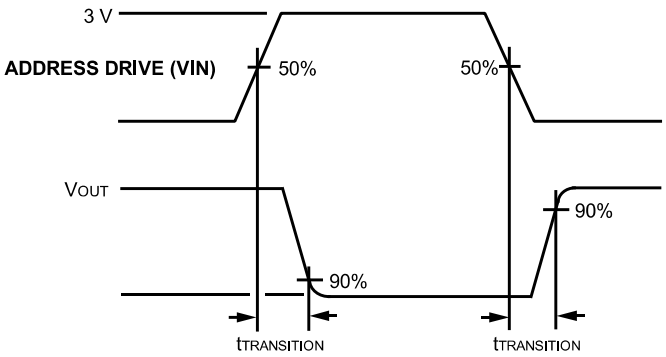
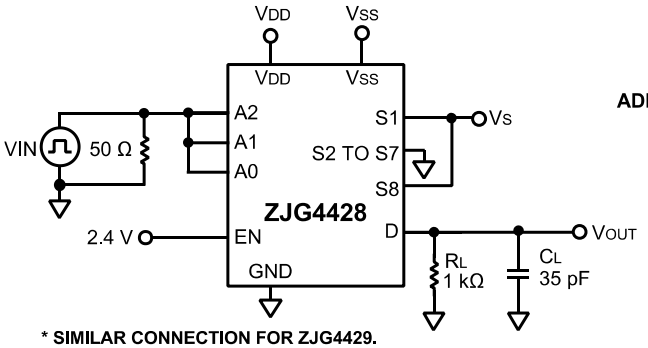


Figure 24. Switching Time of Multiplexer, $t_{TRANSITION}$



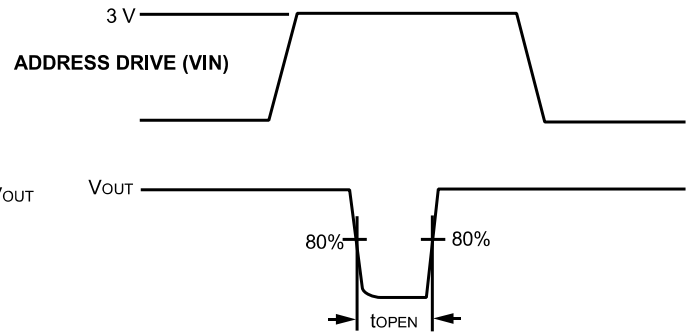
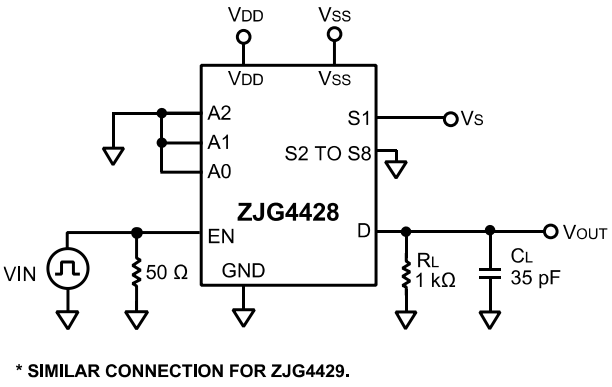


Figure 25. Break-Before-Make Delay, t_{OPEN}



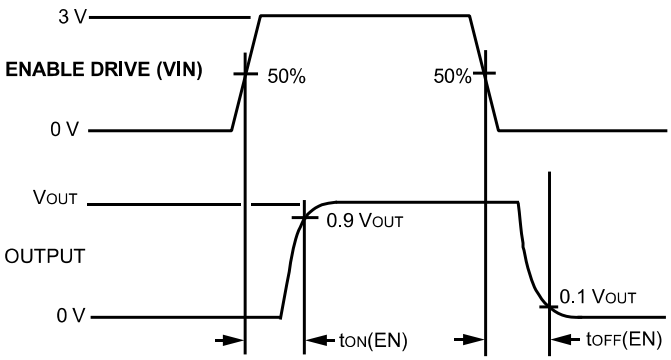
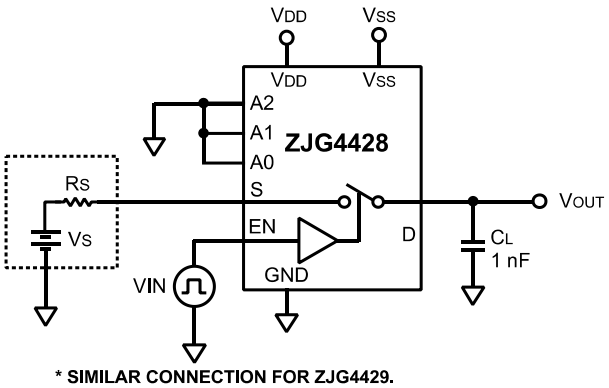


Figure 26. Enable Delay, t_{ON} (EN), t_{OFF} (EN)



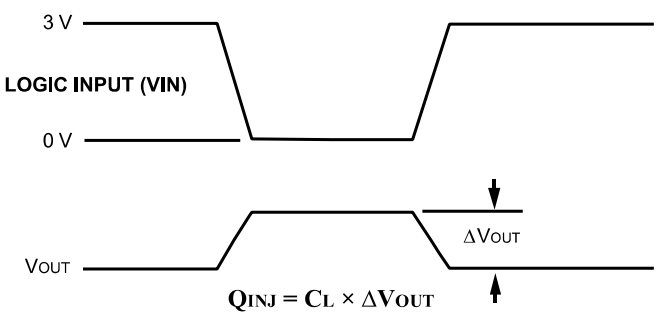


Figure 27. Charge Injection

Applications Information

The ZJG4428 and ZJG4429 are 36 V precision high-voltage multiplexers designed to switch among multiple high-voltage signals. A latch-up happens at the system's front end can lead to severe consequences, often requires a full system reset or causes hardware damage. ZJG4428 and ZJG4429 mitigate this risk by ensuring that all pins—including input, output, and logic control pins—are inherently latch-up free. This key feature simplifies system design and maintenance while enhancing overall system reliability.

On-resistance (Ron) is a key parameter for analog switches and multiplexers. ZJG4428 offers a typical Ron of 270 Ω. Unlike many high-voltage analog switches and multiplexers, where Ron can significantly increase as the signal approaches the power rails, ZJG4428 exhibits superior Ron flatness over a wider voltage range, as shown in Figure 28. Powered by ±15 V with a ±10 V input voltage, the ZJG4428 exhibits a typical flatness of 5% and a maximum flatness of 7% at room temperature. In the extended industrial temperature range (-40 °C to 125 °C), the maximum flatness remains within 10%. This characteristic makes them ideal for high-precision data acquisition systems requiring 16-bit or greater accuracy.

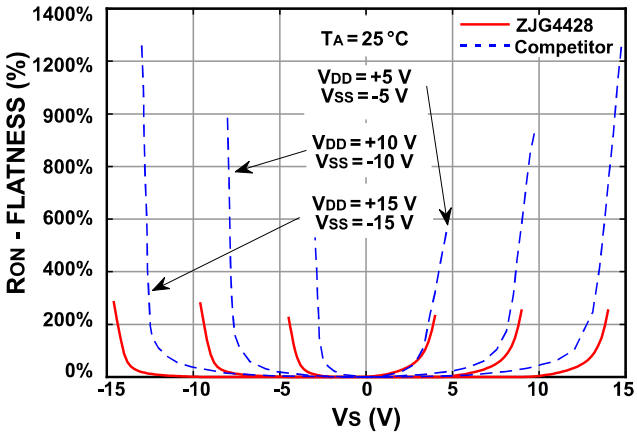


Figure 28. ZJG4428 On Resistance vs. Input Voltage

Leakage current when the switch is on is a critical DC specification for analog switches and multiplexers, as it decides system accuracy. Higher leakage current leads to increased measurement error, making the device less suitable for precision data acquisition systems. ZJG4428 exhibits excellent leakage current characteristics, as illustrated in Figure 29. When powered by ±15 V with a ±10 V input, they achieve a leakage current of 10 pA at room temperature. Over the temperature range of -40 °C to 85 °C, the leakage current remains below 4 nA, and even at -40 °C to 125 °C, it stays within 200 nA. These low leakage currents make them ideal for 14-bit or greater data acquisition systems.

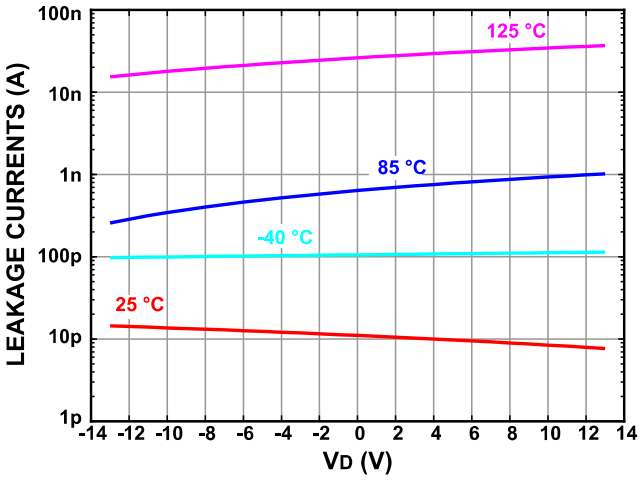


Figure 29. ZJG4428 Leakage Current when Turned On

Charge injection, which occurs during switching, can interfere with input signals and degrade system linearity. As shown in Figure 30, ZJG4428 exhibits a lower charge injection of 14.8 pC and maintains superior flatness across the entire input range compared to competing parts.

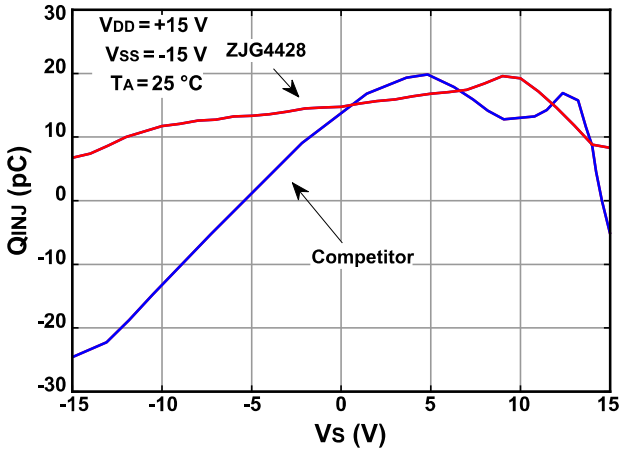


Figure 30. ZJG4428 Charge Injection vs. Source Voltage V_S

ZJG4428 and ZJG4429 offer fast switching times of 166 ns t_{ON} and 135 ns t_{OFF}. They are in break-before-make construction and the crosstalk between channels is just 104 dB. In the off state, they exhibit low input capacitance C_S of 2.6 pF and output capacitance C_D of 5.8 pF for ZJG4438 and 3.2 pF for ZJG4439. Their CMOS and TTL-compatible parallel interfaces simplify integration and ease of use.

Outline Dimensions

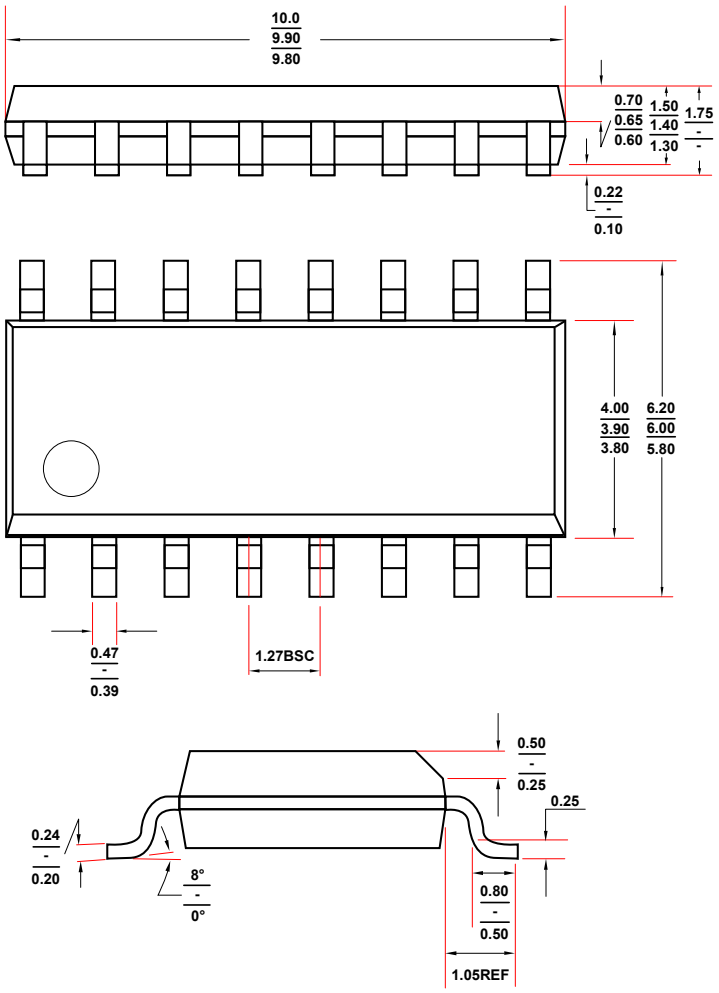


Figure 31. 16-Lead SOIC Package Dimensions Shown in Millimeters

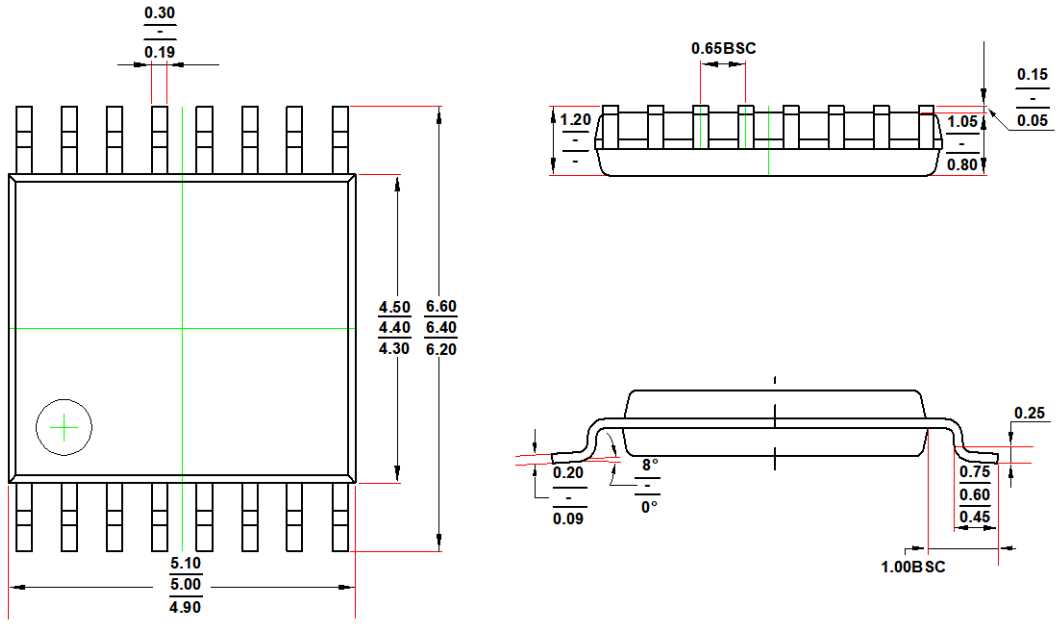
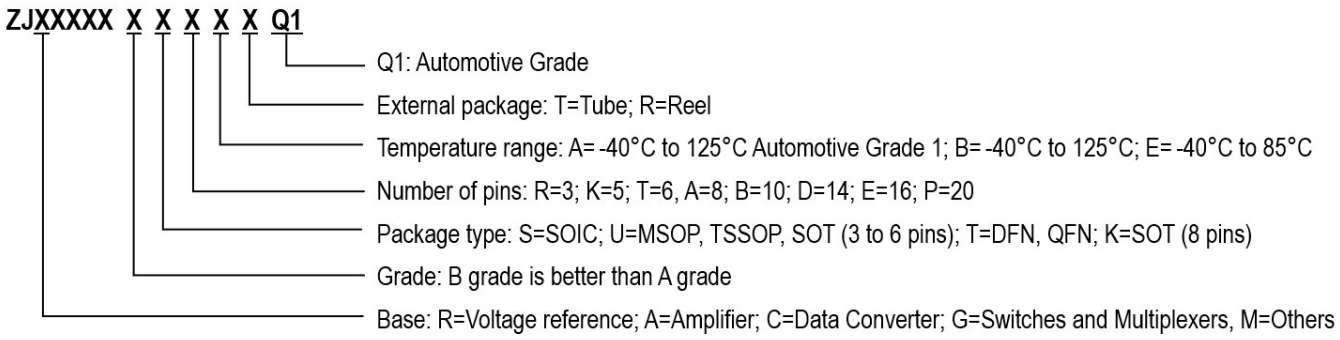


Figure 32. 16-Lead TSSOP Package Dimensions Shown in Millimeters

Ordering Guide

Model	Orderable Device	Function	Temperature Range (°C)	Package	External Package
ZJG4428	ZJG4428ASEBT	8:1 Multiplexer	-40 to +125	SOIC-16	Tube
	ZJG4428ASEBR			SOIC-16	13” Reel
	ZJG4428AUEBT			TSSOP-16	Tube
	ZJG4428AUEBR			TSSOP-16	13” Reel
ZJG4429	ZJG4429ASEBT	4:1 Differential Multiplexer	-40 to +125	SOIC-16	Tube
	ZJG4429ASEBR			SOIC-16	13” Reel
	ZJG4429AUEBT			TSSOP-16	Tube
	ZJG4429AUEBR			TSSOP-16	13” Reel

Product Order Model



Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV