2.7 V~5.5 V Supply, Voltage Output Precision DAC

Features

- 18/16/14-bit resolution
- 2.7 V to 5.5 V single supply
- 1 μs settling time
- Power-on output:
  - ZJC2542-18/16/14: 0 V
  - ZJC2544-18/16/14: $V_{REF}/2$
- Low glitch: 1 nV-s
- Low noise spectral density: 11 $nV/\sqrt{Hz}$
- Low gain temperature drift: 0.05 ppm/°C
- Low power dissipation: 120 μA supply current
- Package: SOIC-14/TSSOP-16/QFN-16
- Operating temperature range: -40 °C to +125 °C

Application

- Precision Control Equipment
- Automated Testing
- Precision Instrument
- Medical Instrument

General Description

ZJC2542/4-18/16/14 (hereinafter referred to as ZJC2542/4) it is a single, serial data input, voltage output 18/16/14-bit resolution precision digital-to-analog converter (DAC). Its supply voltage is 2.7 V to 5.5 V, the output range is 0 V to V_{REF}, and monotonicity is guaranteed and can guarantee DNL/INL accuracy over temperature range of -40 °C to +125 °C.

The ZJC2542/4 can operate in bipolar mode with precision amplifiers to generate a $\pm V_{REF}$ output swing. It also includes Kelvin sense connections for the reference and analog ground pins.

The output of ZJC2542/4 is un-buffered. The settling time is within 1 μs, and it has the characteristics of low power consumption and low offset error. Low noise performance and low glitches make it suitable for use in a variety of end systems.

ZJC2542/4 adopts multifunctional three-wire interface, and is compatible with SPI, QSPI, MCU and DSP interface standards.

The default output voltage of ZJC2542 is 0 V; While it is $V_{REF}/2$ for ZJC2544. Other functions and performance indicators are exactly the same.

Application Example

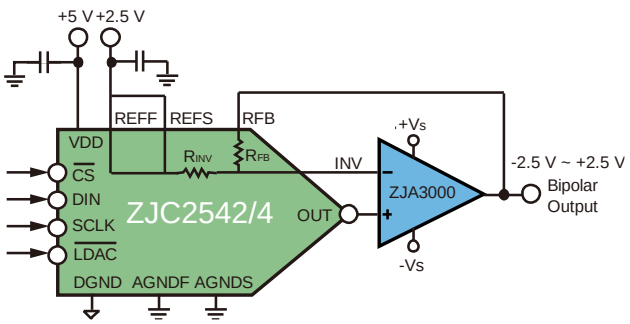

Figure 1. Applications

Typical Performance Characteristics

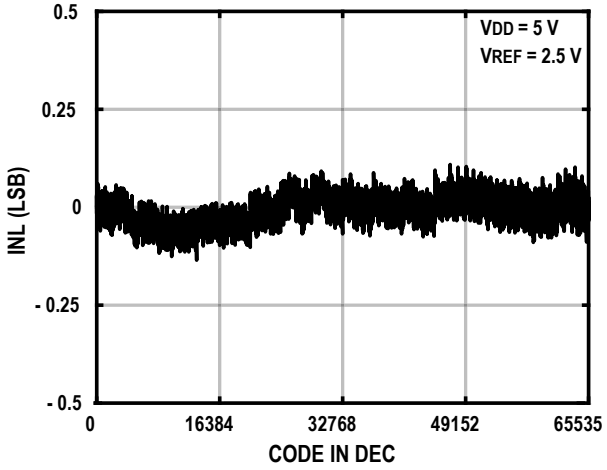

Figure 2. ZJC2542/4-16 INL

18/16/14 -bit bipolar DAC series models are as follows:

DAC Resolution (bit)	DAC Model	Power-on Output Voltage	Package
18	ZJC2542-18	0	SOIC-14/TSSOP-16/QFN-16
18	ZJC2544-18	$V_{REF}/2$	
16	ZJC2542-16	0	
16	ZJC2544-16	$V_{REF}/2$	
14	ZJC2542-14	0	
14	ZJC2544-14	$V_{REF}/2$	

Table Of Contents

Version (Release C)[1]

July 2024——Release C

English Version

Update Bipolar Output Part

Updated Ordering Guide, Product Order Model and Related Parts

August 2023——Release B

Update Full Text Formatting

Add MSOP-16, DFN-16 pin configuration and function

Timing diagram changes

Add MSOP-16, DFN-16 package dimensions

June 2023——Release A

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Pin Configuration And Function

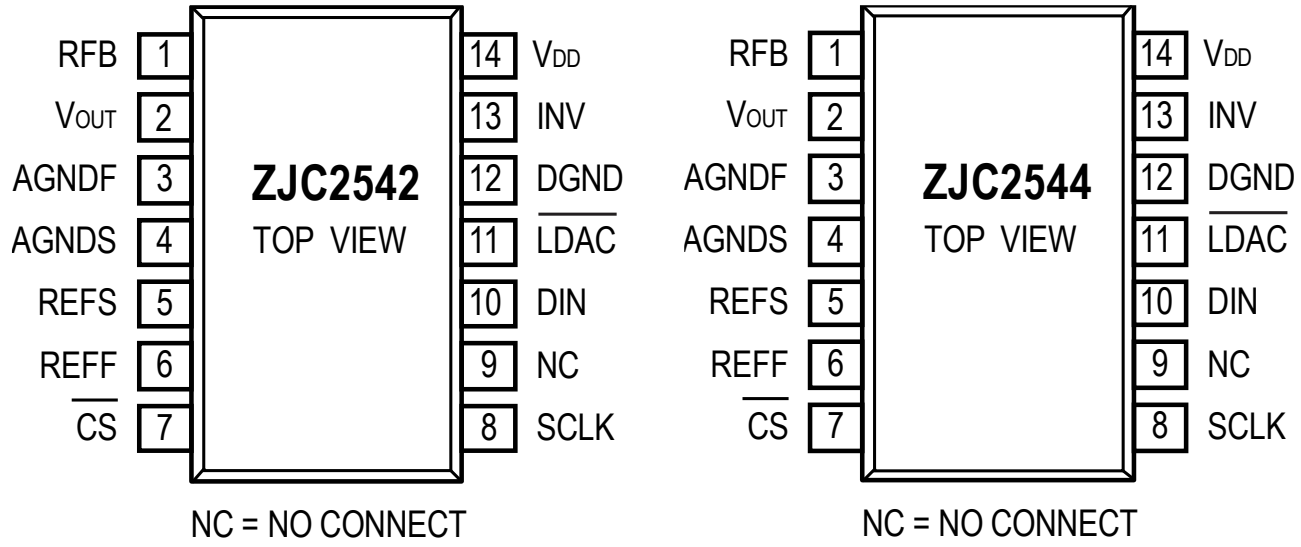

Figure 3. ZJC2542 and ZJC2544 with the Same 14-Pin SOIC Pinout Diagram

Mnemonic	Pin No.	Pin Type	Description
R_{FB}	1	Analog Input	Feedback resistor input pin. Connect it to external amplifier output for bipolar mode.
V_{OUT}	2	Analog Output	DAC un-buffered voltage output. The output resistance is typically 6.25 kΩ.
AGNDF	3	Analog Ground Force	Analog ground force pin.
AGNDS	4	Analog Ground Sense	Analog ground sense pin.
REFS	5	Analog Output	Voltage reference sense output.
REFF	6	Analog Input	Voltage reference force input.
$\overline{CS}$	7	Digital Input	Serial digital chip select input, active at low.
SCLK	8	Digital Input	Serial data clock input.
NC	9	NC Pin	No Connection.
DIN	10	Digital Input	Serial digital signal input.
$\overline{LDAC}$	11	Digital Input	$\overline{LDAC}$ input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
DGND	12	Digital Ground	Digital ground.
INV	13	Analog Output	Connected to the middle point of the internal scaling resistors. Connect the INV pin to external op amps inverting input in bipolar mode.
V_{DD}	14	Power Supply	Supply voltage input.

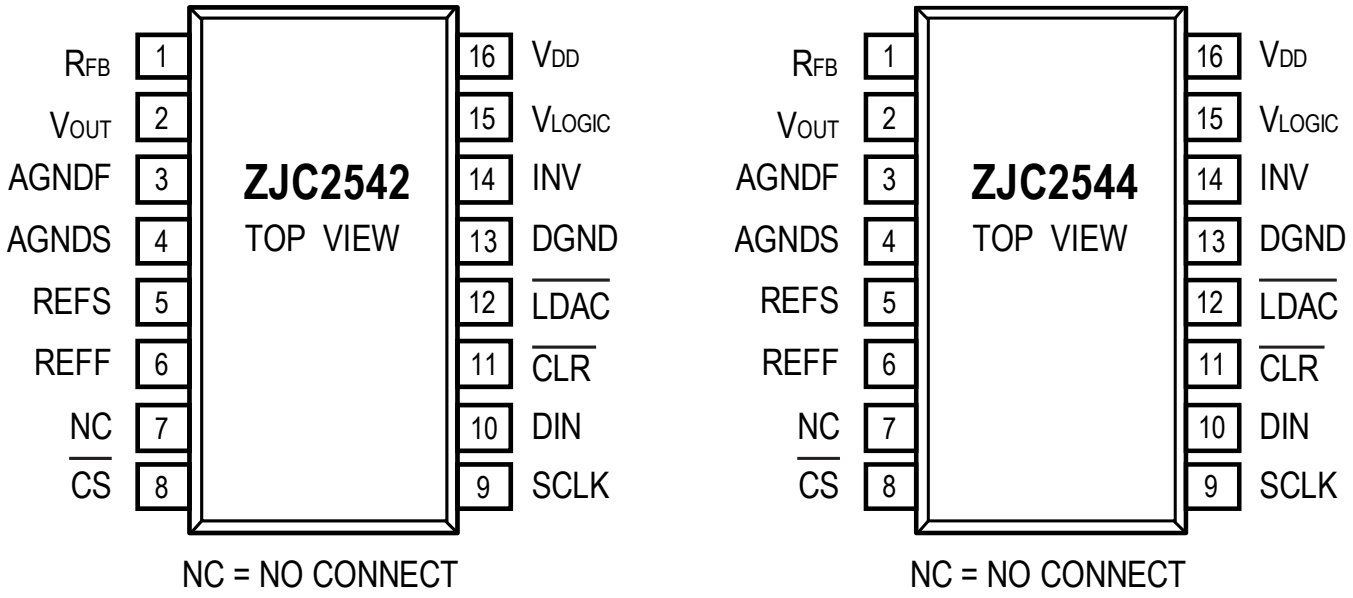

Figure 4. ZJC2542 and ZJC2544 with the Same 16-Pin TSSOP Pinout diagram

Mnemonic	Pin No.	Pin Type	Description
R_{FB}	1	Analog Input	Feedback resistor input pin. Connect it to external amplifier output for bipolar mode.
V_{OUT}	2	Analog Output	DAC un-buffered voltage output. The output resistance is typically 6.25 kΩ.
AGNDF	3	Analog Ground Force	Analog ground force pin.
AGNDS	4	Analog Ground Sense	Analog ground sense pin.
REFS	5	Analog Output	Voltage reference sense output.
REFF	6	Analog Input	Voltage reference force input.
NC	7	NC pin	No Connection.
$\overline{CS}$	8	Digital Input	Serial digital chip select input, active at low.
SCLK	9	Digital Input	Serial data clock input.
DIN	10	Digital Input	Serial digital signal input.
$\overline{CLR}$	11	Digital Input	The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the DAC register is cleared to the model selectable midscale.
$\overline{LDAC}$	12	Digital Input	Digital input. Loads the data latch register code value to the output voltage.
DGND	13	Digital Ground	Digital ground.
INV	14	Analog Output	Connected to the middle point of the internal scaling resistors. Connect the INV pin to an external op amp inverting input in bipolar mode.
V_{LOGIC}	15	Digital Power Supply	Digital interface supply voltage input.
V_{DD}	16	Power Supply	Supply voltage input.

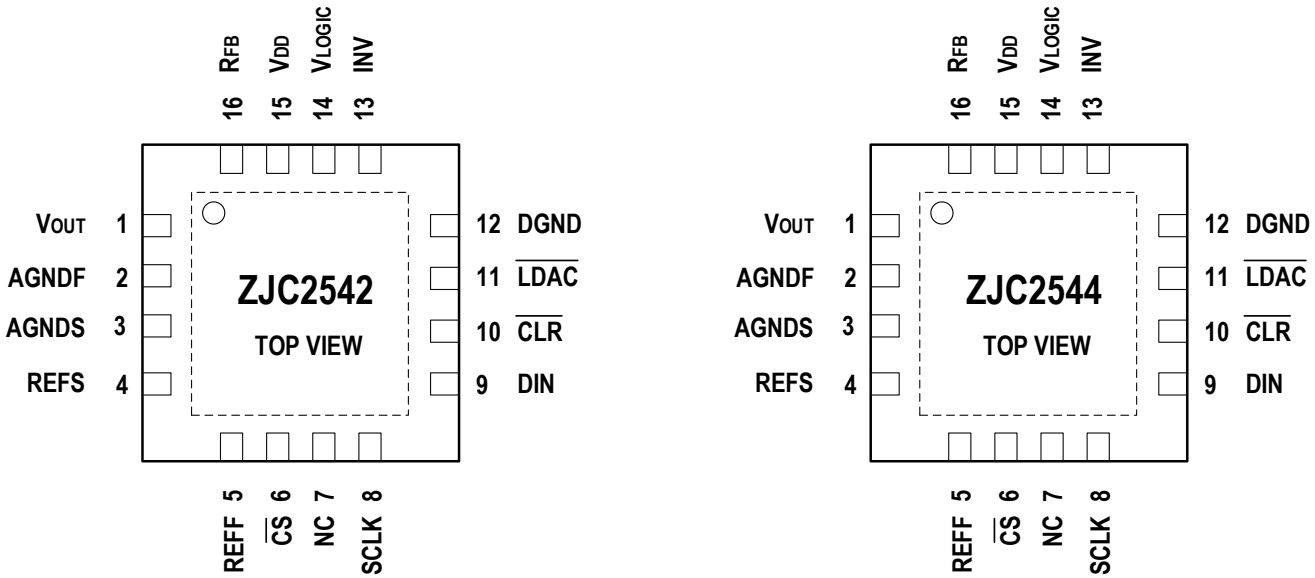

Figure 5. ZJC2542 and ZJC2544 with the same 16-Pin QFN Pinout Diagram

Mnemonic	Pin No.	Pin Type	Description
V_{OUT}	1	Analog Output	DAC un-buffered voltage output. The output resistance is typically 6.25 kΩ.
AGNDF	2	Analog Ground Force	Analog ground force pin.
AGNDS	3	Analog Ground Sense	Analog ground sense pin.
REFS	4	Analog Output	Voltage reference sense output.
REFF	5	Analog Input	Voltage reference force input.
$\overline{CS}$	6	Digital Input	Serial digital chip select input, active at low.
NC	7	NC pin	No Connection.
SCLK	8	Digital Input	Serial data clock input.
DIN	9	Digital Input	Serial digital signal input.
$\overline{CLR}$	10	Digital Input	The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the DAC register is cleared to the model selectable midscale.
$\overline{LDAC}$	11	Digital Input	Digital input. Loads the data latch register code value to the output voltage.
DGND	12	Digital Ground	Digital ground.
INV	13	Analog Output	Connected to the middle point of the internal scaling resistors. Connect the INV pin to an external op amp inverting input in bipolar mode.
V_{LOGIC}	14	Digital Power Supply	Digital interface supply voltage input.
V_{DD}	15	Power Supply	Supply voltage input.
R_{FB}	16	Analog Input	Feedback resistor input pin. Connect it to external amplifier output for bipolar mode.
EP	EP	Exposed PAD	The exposed pad should be tied to GND.

Absolute Maximum Ratings[1]

Parameter	Rating
V_{DD} to AGND	-0.3 V~+6 V
REF to AGND	-0.3 V~V_{DD}+0.3 V
Digital Input to DGND	-0.3 V~V_{DD}+0.3 V
Input current to pins except V_{DD}	±10 mA
Storage Temperature Range	-65 °C~+150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature[2]	260 °C
Electrostatic Discharge (ESD)[3]	
Human Body Model (HBM)[4]	3.5 kV
Charged Device Model (CDM)[5]	2 kV

Thermal Resistance[6]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-14	106.7	54.2	°C/W
TSSOP-16	104	29	°C/W
QFN-16	51	27	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDECJ–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise noted. V_{DD}=2.7 V~5.5 V, V_{REF}=2.5 V~V_{DD}, AGND=DGND=0 V, T_A=25 °C.

Parameter	Symbol	Conditions			Min	Typ	Max	Unit
Resolution								
ZJC2542/4-18		18-bits					18	bits
ZJC2542/4-16		16-bits					16	
ZJC2542/4-14		14-bits					14	
Accuracy								
Integral Nonlinear Error	INL	18 bits	-40 °C≤T_A≤+85 °C		-2.5	±1	+2.5	LSB
			-40 °C≤T_A≤+125 °C	●	-4	±1	+4	
		16 bits		●	-1	±0.5	+1	
		14 bits		●	-0.5	±0.2	+0.5	
Differential Nonlinear Error	DNL	18 bits	-40 °C≤T_A≤+85 °C		-0.85	±0.5	+0.85	LSB
			-40 °C≤T_A≤+125 °C	●	-1	±0.5	+1	
		16 bits		●	-0.75	±0.25	+0.75	
		14 bits		●	-0.25	±0.1	+0.25	
Gain Error	GE	18 bits	T_A=25 °C		-1.5	±0.5	+1.5	LSB
			-40 °C≤T_A≤+85 °C		-2.5	0.5	+2.5	
			-40 °C≤T_A≤+125 °C	●	-4	±0.5	+4	
		16 bits	T_A=25 °C		-0.75	± 0.3	+0.75	
			-40 °C≤T_A≤+85 °C		-1	±0.5	+1	
			-40 °C≤T_A≤+125 °C	●	-1.5	±0.5	+1.5	
		14 bits	T_A=25 °C		-0.3	±0.1	+0.3	
			-40 °C≤T_A≤+85 °C		-0.5	±0.15	+0.5	
			-40 °C≤T_A≤+125 °C	●	-0.75	±0.25	+0.75	
Gain Error Temperature Drift						±0.05		ppm/°C
Zero Code Error	ZCE	18 bits		●	-2	±0.5	+2	LSB
		16 bits		●	-1	±0.25	+1	
		14 bits		●	-0.5	±0.15	+0.5	
Zero Code Error Temperature Coefficient						±0.1		ppm/°C
Bipolar Resistor Matching		R_{FB}/R_{INV}, typically $R_{FB}=R_{INV}$=28 kΩ				±20	±80	ppm
Bipolar Zero Code Error		18-bit		●	-16	±4	+16	LSB
		16-bit		●	-4	±1	+4	
		14-bit		●	-1	±0.25	+1	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Bipolar Zero Code Error Drift					±0.1		ppm/°C
Output Characteristics							
Output Voltage Range		Unipolar	●	0		V_{REF}-1 LSB	V
		Bipolar	●	-V_{REF}		V_{REF}-1 LSB	V
Output Voltage Settling Time		to 1/2 LSB of full scale, C_L=10 pF					
		18 bits			1		µs
		16 bits			1		
		14 bits			1		
Slew rate		C_L=10 pF, measured from 0% to 63%			16		V/µs
Digital-to-Analog Conversion Glitch	Glitch	Major carry changes 1 LSB (16-bit resolution)			1		nV-s
Digital Feedthrough		All 1s sent to DAC, V_{REF}=2.5 V			0.2		nV-s
DAC Output Impedance		General tolerance 20%			6.25		kΩ
Output Noise Density		Frequency=1 kHz			11		nV/$\sqrt{Hz}$
Output Noise		0.1 Hz to 10 Hz			0.18		μV_{P-P}
Spurious Free Dynamic Range	SFDR	f_{IN}=1 kHz, V_{REF}=5 V			87		dB
Total Harmonic Distortion	THD	DAC code=0xFFFF, Frequency=10 kHz, V_{REF}=2.5 V±1 V_{P-P}			-87		dB
Power Supply Rejection Ratio		Δ V_{DD}±10%			±0.5		LSB
DAC reference input							
Voltage Range			●	2		V_{DD}	V
Input Resistance[1]		Unipolar	●	8			kΩ
		Bipolar	●	6			kΩ
Reference -3dB bandwidth		All 1 code			2		MHz
Reference Feedthrough		All 0 codes, V_{REF}=1 V_{P-P}, 100 kHz			1.5		mV_{P-P}
SINAD					92		dB
Reference Input Capacitance		DAC code=0x0000			130		pF
		DAC code=0xFFFF			190		pF
Digital Input							
Input High Voltage	V_{IH}		●	2.4/0.9*V_{LOGIC}			V
Input Low Voltage	VIL		●			0.8/0.1*V_{LOGIC}	V
Input Current			●	-1		+1	µA
Input Capacitance						10	pF
Hysteresis Voltage					0.15		V

[1] Reference input resistance varies with code, 16-bit minimum at 0x8555.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Power Supply							
Power Supply	V_{DD}		●	2.7		5.5	V
Electric Current	I_{VDD}	V_{DD}=5 V			120		μA
Digital Interface Power	V_{LOGIC}			1.8		5.5	V
Temperature Range							
Rated Performance		T_{MIN} to T_{MAX}		-40		+125	°C

Timing Index

The ● denotes the full temperature range for specified performance. Unless otherwise specified, T_A=25 °C, V_{DD}=2.7 V to 5.5 V, V_{REF}=2.5 V, V_{LOGIC}=1.8 V to V_{DD}, V_{INH}=3 V and 90% of V_{DD}, V_{INL}=0 V and 10% of V_{DD}, AGND=DGND=0 V.

Parameters [1,2]	Symbol		Limit 1.8 V≤V_{LOGIC}<2.7 V	Limit 2.7 V≤V_{LOGIC}≤5.5 V	Unit
SCLK Frequency	f_{SCLK}	●	14	50	MHz max
SCLK Period	t_1	●	70	20	ns min
SCLK High Level Time	t_2	●	35	9	ns min
SCLK Low Level Time	t_3	●	35	9	ns min
$\overline{CS}$ Low To SCLK High Setup Time	t_4	●	5	5	ns min
$\overline{CS}$ High To SCLK High Setup Time	t_5	●	50	50	ns min
SCLK High To $\overline{CS}$ Low Hold Time	t_6	●	5	5	ns min
SCLK High To $\overline{CS}$ High Hold Time	t_7	●	10	5	ns min
Data Creation Time	t_8	●	35	10	ns min
Data Hold Time (V_{INH}=90% of V_{DD}, V_{INL}=10% of V_{DD})	t_9	●	5	5	ns min
$\overline{CS}$ High Time Between Low Levels	t_{10}	●	15	15	ns min
$\overline{LDAC}$ Low Pulse Width	t_{11}	●	20	20	ns min
$\overline{CS}$ High To $\overline{LDAC}$ Low Settling Time	t_{12}	●	10	10	ns min
$\overline{LDAC}$ Low To SCLK High Setup Time	t_{13}	●	60	60	ns min

DB17 for 18-bit DAC code value, DB15 for 16 -bit DAC code value, and DB13 for 14 -bit DAC code value.

For a frame of SPI data operation, if the number of SCLK cycles during the chip select low level is greater than the number of bits of the DAC, the lower 18/16/14-bit data is valid, and the redundant high bits are ignored.

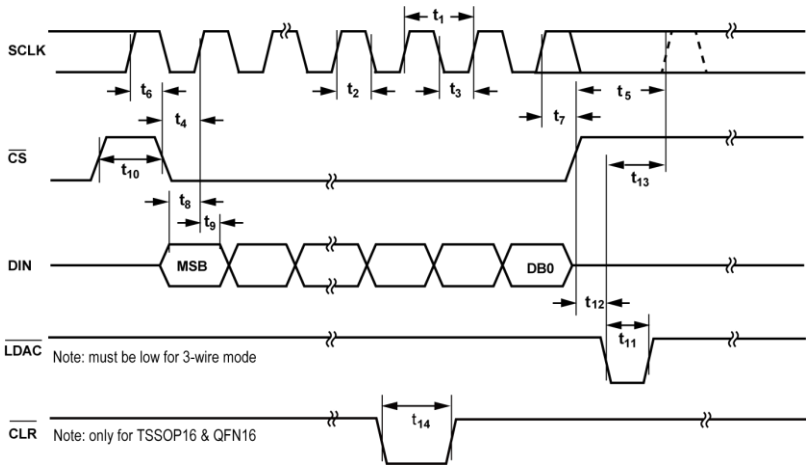

Figure 6. Digital Interface Timing

1 V_{DD}=2.7 V to 5.5 V, the maximum SCLK frequency is 50 MHz.
2 All input signals are specified with t_R=t_F=1 ns/V and from (V_{IL}+V_{IH})/2 level to start timing.

Typical Performance Characteristics

Unless otherwise noted, V_{DD}=5.0 V, V_{REF}=2.5 V, T_A=25 °C.

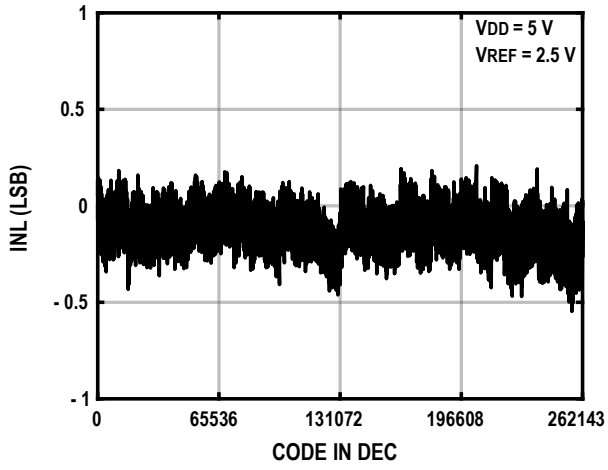

Figure 7. Integral Nonlinearity vs. Code-18 bits

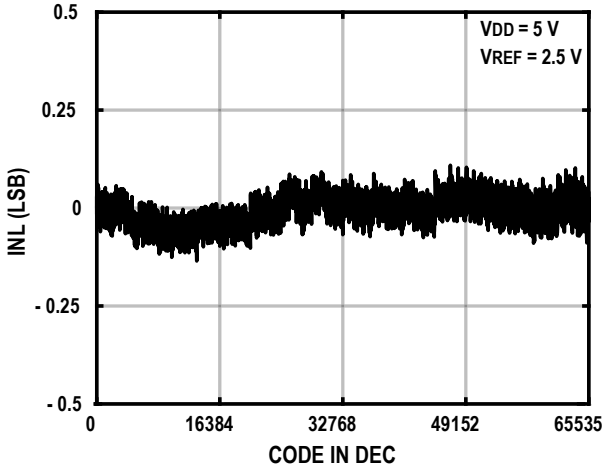

Figure 8. Integral Nonlinearity vs Code-16 bit

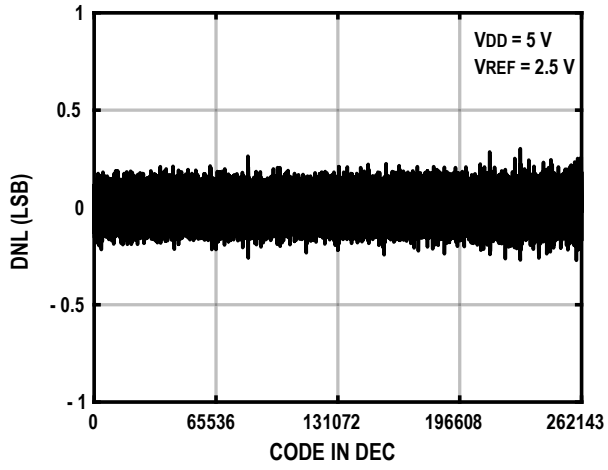

Figure 9. Differential Nonlinearity vs. Code-18 Bits

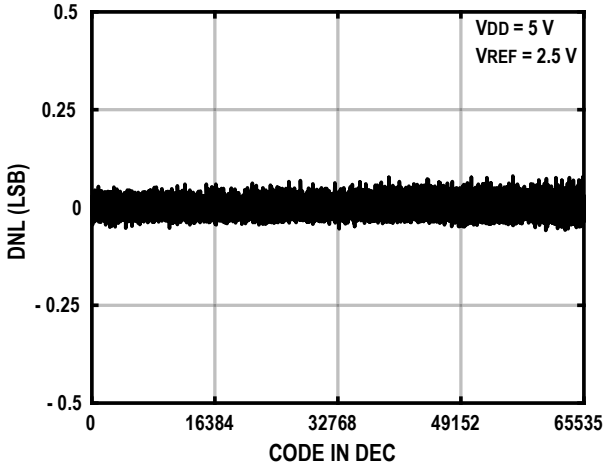

Figure 10. Differential Nonlinearity vs. Code-16 bits

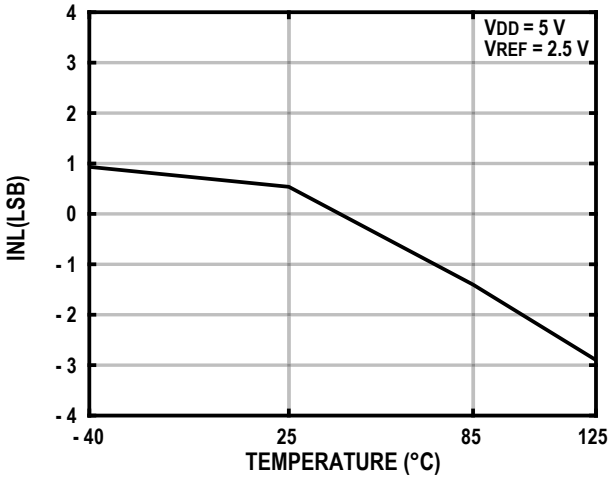

Figure 11. Integral Nonlinearity vs. Temperature-18 bits

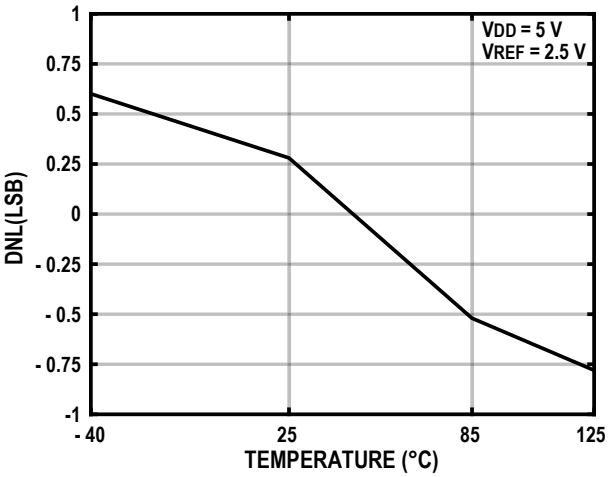

Figure 12. Differential Nonlinearity vs. Temperature-18 Bits

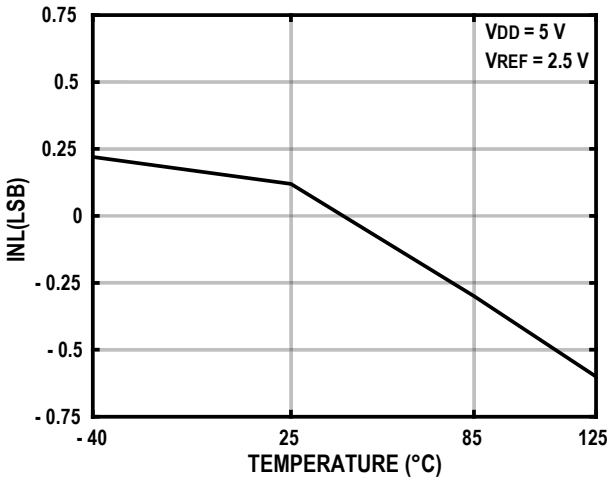

Figure 13. Integral Nonlinearity vs. Temperature-16 bits

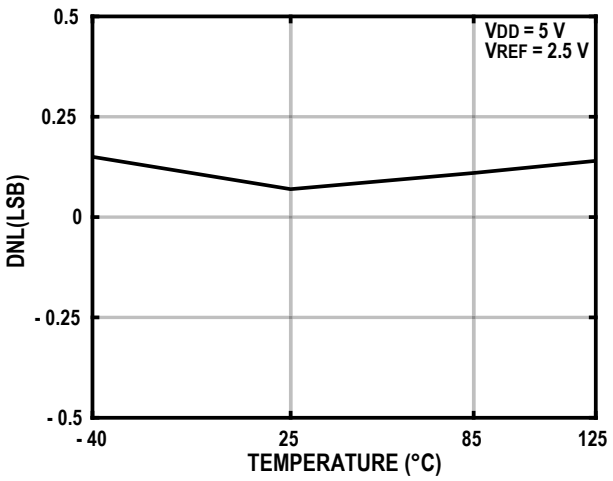

Figure 14. Differential Nonlinearity vs. Temperature-16 bits

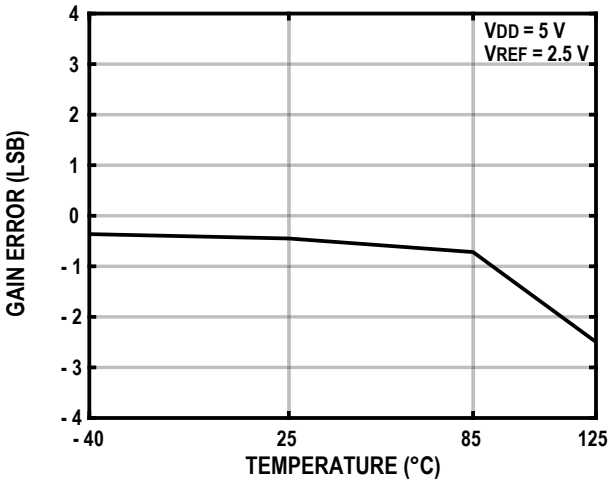

Figure 15. Gain Error vs Temperature-18 Bit

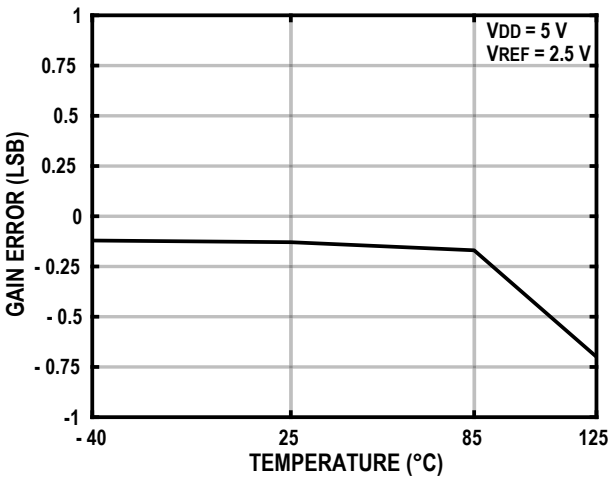

Figure 16. Gain Error vs Temperature-16 Bit

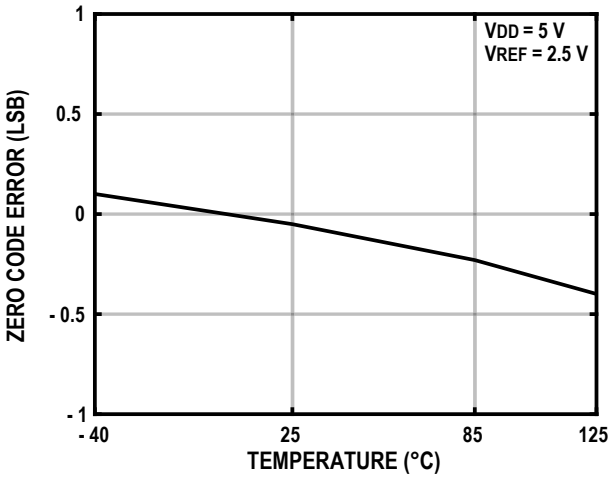

Figure 17. Zero Code Error vs Temperature-18 Bit

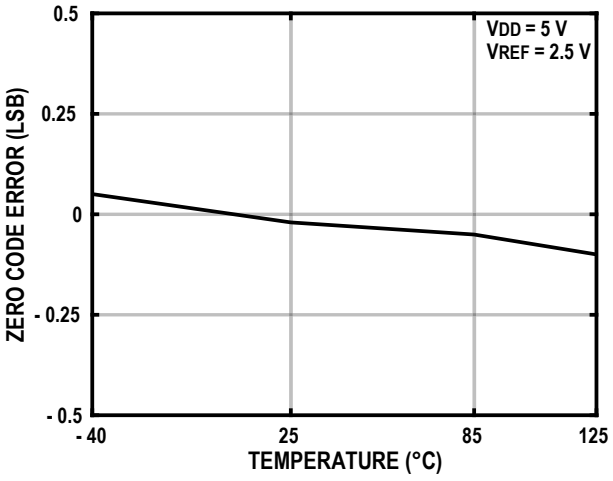

Figure 18. Zero Code Error vs Temperature-16 Bit

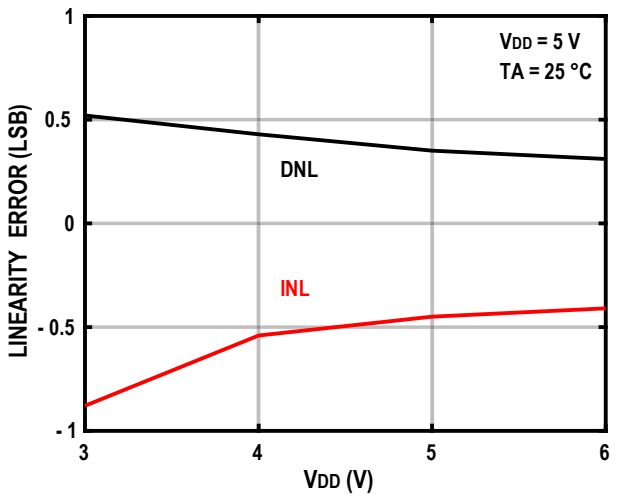

Figure 19. Linearity Error vs Supply Voltage-18 Bit

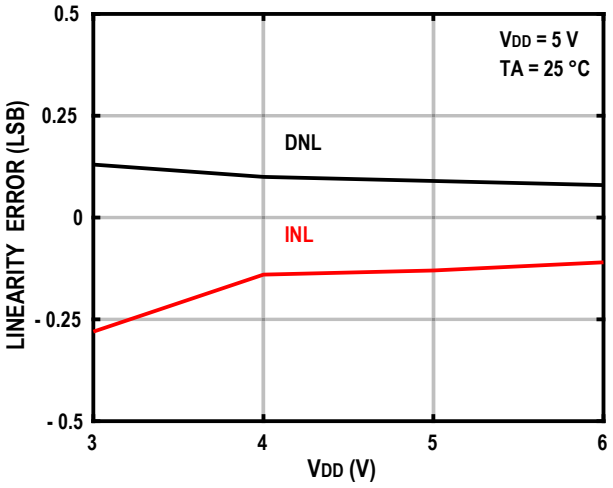

Figure 20. Linearity Error vs Supply Voltage-16 Bit

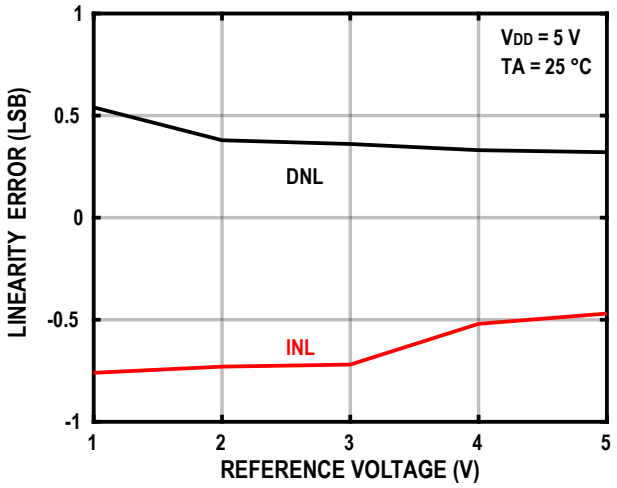

Figure 21. Linearity Error vs. Reference Voltage-18 Bit

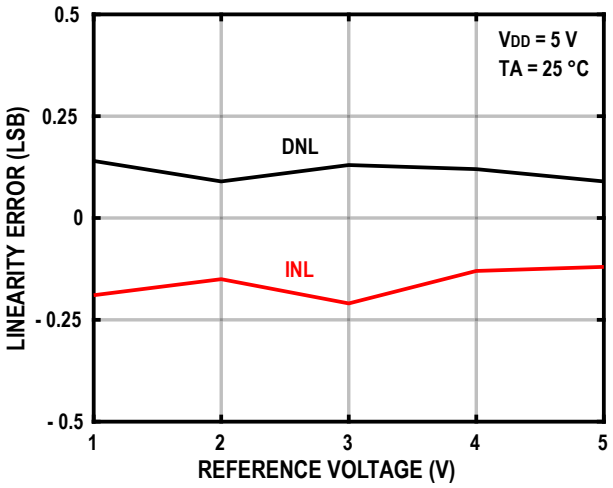

Figure 22. Linearity Error vs. Reference Voltage-16 Bit

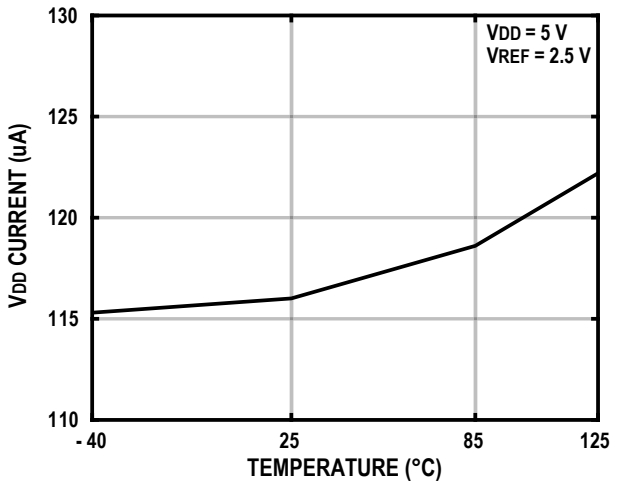

Figure 23. Supply Current vs. Temperature

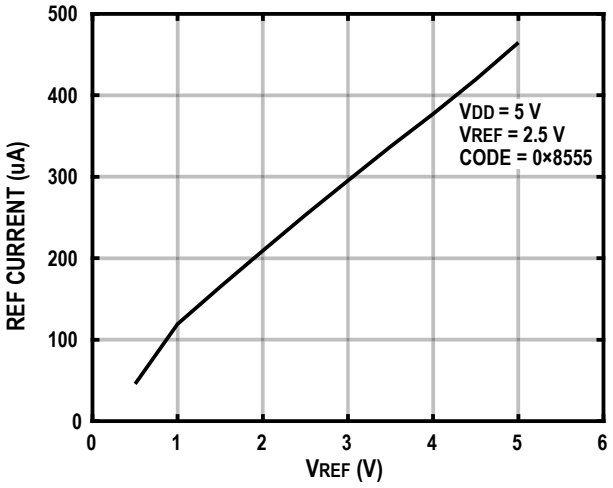

Figure 24. 16-bit DAC Reference Current vs. Voltage

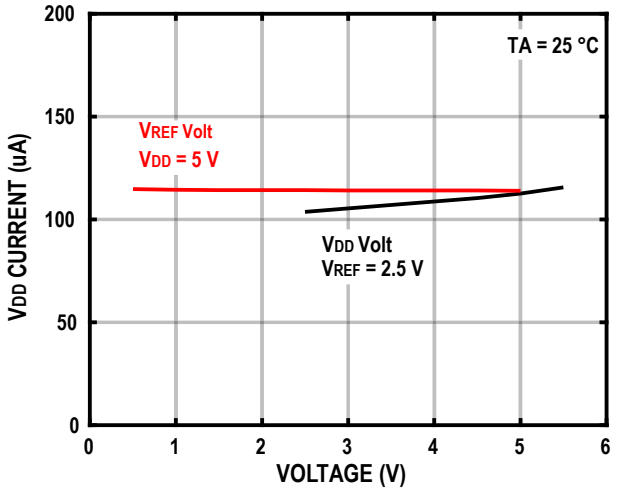

Figure 25. Current vs. Supply Voltage

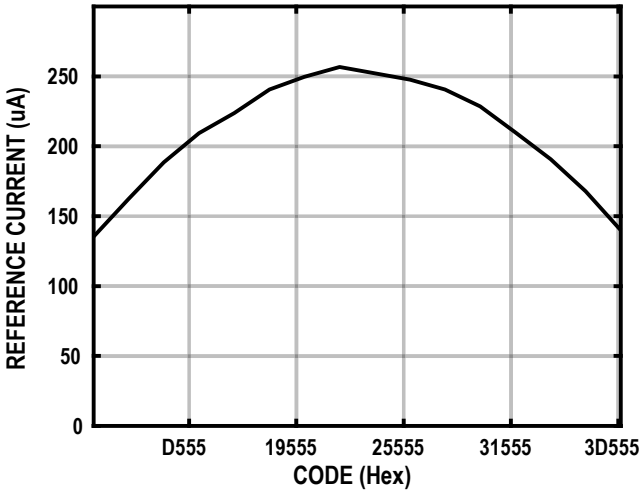

Figure 26. Reference Current vs. Code-18-bit

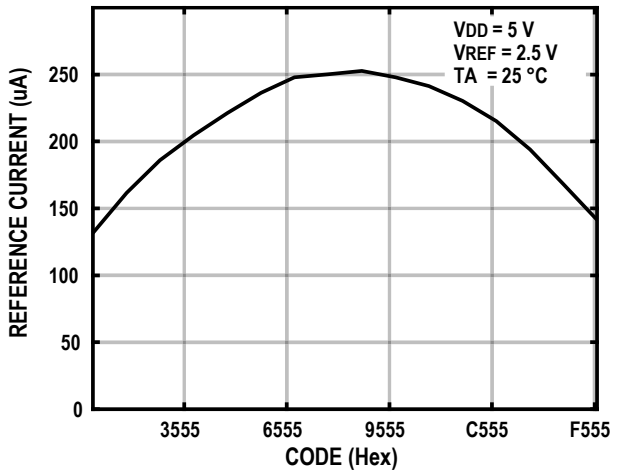

Figure 27. Reference Current vs. Code-16 bits

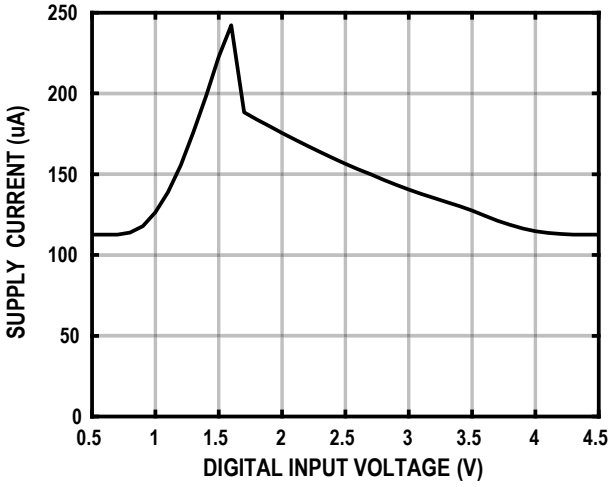

Figure 28. Supply Current vs. Digital Input Voltage

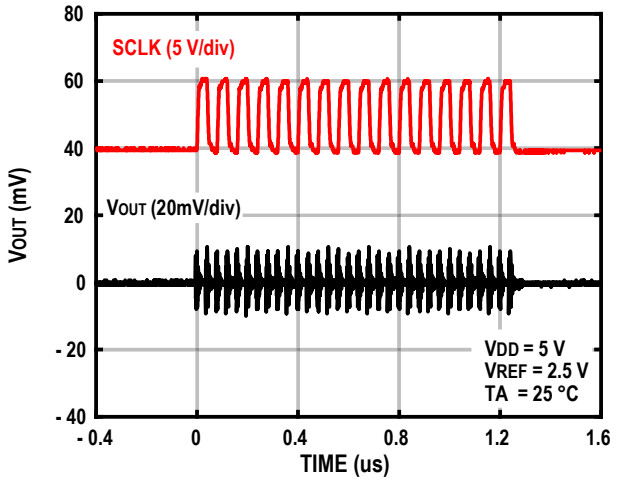

Figure 29. Digital Feedthrough

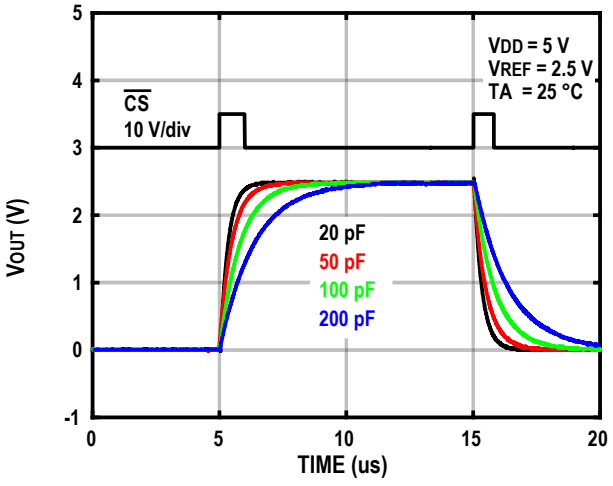

Figure 30. Large Signal Settling Time

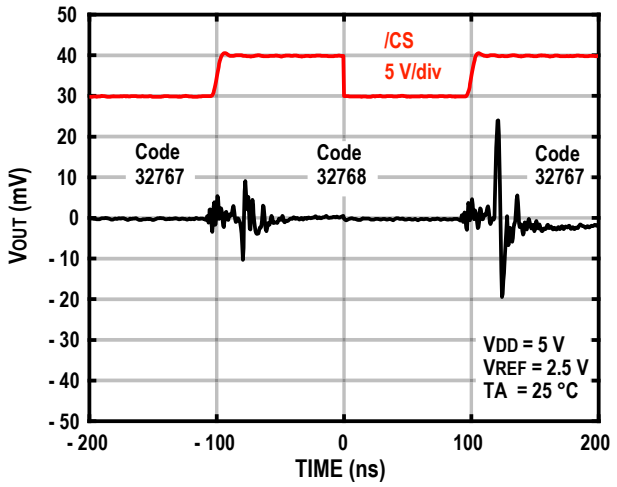

Figure 31. ZJC2542/4-16 DAC Glitch Pulse

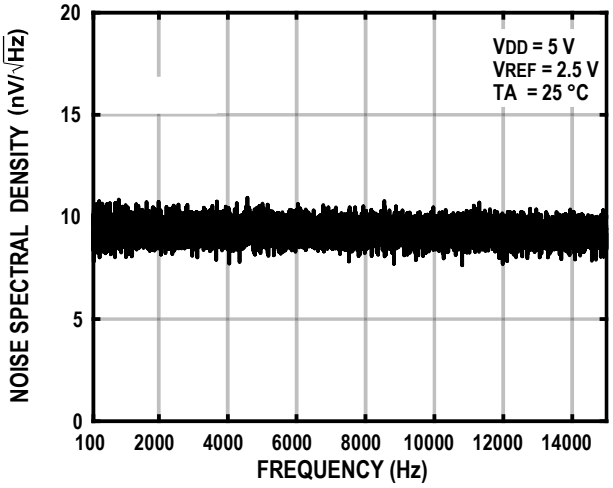

Figure 32. Noise Spectral Density vs. Frequency

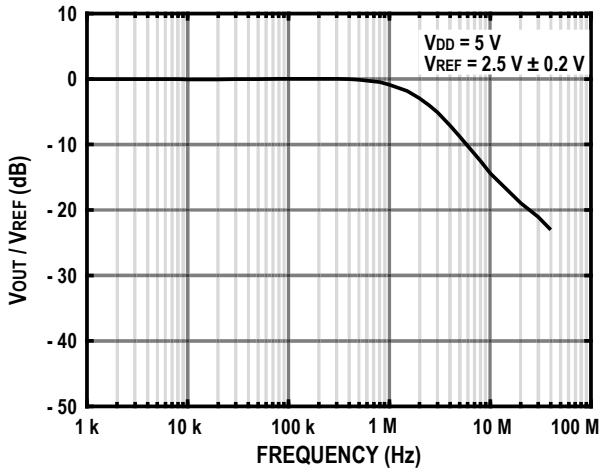

Figure 33. Multiplication Bandwidth

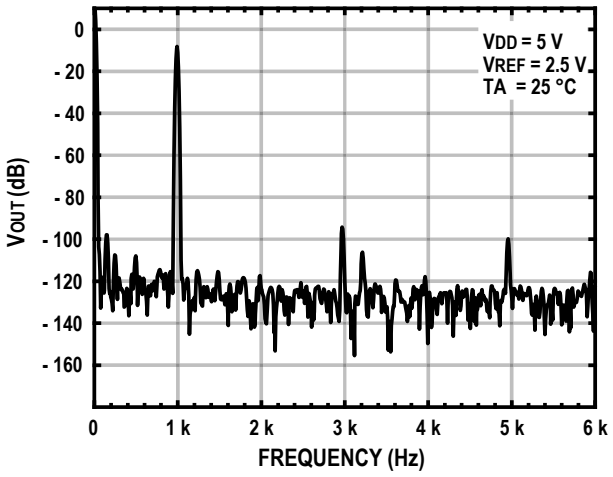

Figure 34. Harmonic Distortion

Theory Of Operation

ZJC2542/4-18/16/14 is a single-channel 18/16/14-bit, serial input, voltage output DAC. They operate from a single supply range of 2.7 V to 5.5 V and typically draw 120 μA from a 5 V supply. Data is written in 18/16/14 bit word format via a 3-wire serial interface. To ensure a known power-on state, these parts are designed with a power-on reset function. After ZJC2542 is powered on, the default output is 0 V; and after ZJC2544 is powered on, the default output is the middle level $V_{REF}/2$ of the reference.

Digital-to-Analog Conversion

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 35. The DAC structure of ZJC2542/4 is segmented. Taking ZJC2542-16 as an example, the four MSBs of the 16-bit data word are decoded to drive 15 switches, from E1 to E15. A switch connected to each termination resistor can gate AGND or V_{REF}. The lower 12 bits of the data word control the switching of switches S11 to S0 of the R-2R ladder network.

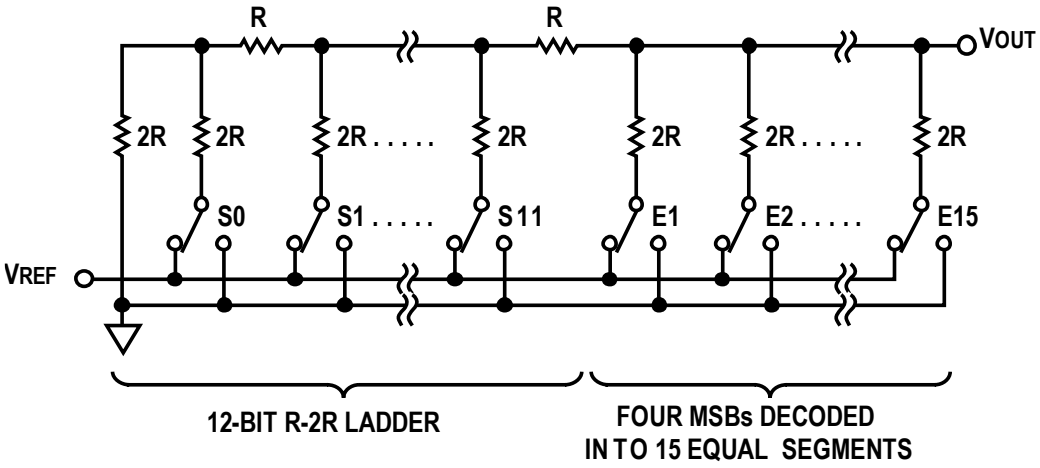

Figure 35. 16-bit DAC structure

With this type of DAC configuration, the output impedance is code independent, while the input impedance seen by the reference is code dependent. The output voltage is related to the reference level as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

Where:

D is the decimal data word loaded into the DAC register.

N is the resolution of the DAC.

For a reference level of 2.5 V, the equation simplifies to:

$$V_{OUT} = \frac{2.5\ V \times D}{2^N}$$

This makes intermediate codes correspond to a V_{OUT} of 1.25 V and full codes correspond to a V_{OUT} of the DAC of 2.5 V-1 LSB.

The size of the LSB is $V_{REF}/2^N$.

Serial Interface

ZJC2542/4 is controlled by a general-purpose 3-wire serial interface with an operating clock frequency up to 50 MHz. The timing is shown in Figure 6. After $\overline{CS}$ a high-to-low transition, data is clocked by the serial (SCLK) Rising edge transfers synchronously into the input register. Data is loaded MSB first into 18/16/14-bit words. When all the data bits have been loaded into the serial input register, $\overline{CS}$ a rising edge on OUT transfers the contents of the shift register to the DAC.

$\overline{LDAC}$ allows the DAC latch to be updated asynchronously by pulling $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be held high when data is being written to the input shift register. Alternatively, $\overline{LDAC}$ can be fixed low to update the DAC output by $\overline{CS}$ rising edge.

When initially loading data into the DAC, the specified number of bits of data should be loaded to prevent erroneous data in the output. If more than the specified number of digits are loaded, the data of the last few specified digits will be retained; if less than the specified number of digits is loaded, the previous valid data will be retained. For example, if ZJC2542-16 needs to interface with data less than 16 bits, it should be filled with 0 on the LSB bits.

Unipolar Output

ZJC2542/4 directly provides unipolar output swing from 0 V to $V_{REF.}$ With an external op amp, the ZJC2542/4 can be used to provide a bipolar voltage output.

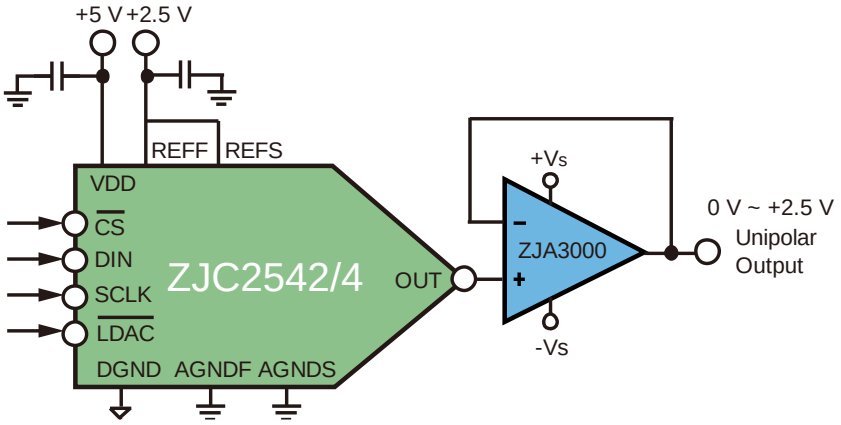

Figure 36. Typical Output Connections

ZJC2542/4-16 digital code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
1111 1111 1111 1111	V_{REF}×(65535/65536)
1000 0000 0000 0000	V_{REF}×(32768/65536)=½ V_{REF}
0000 0000 0000 0001	V_{REF}×(1/65536)
0000 0000 0000 0000	0 V

The unipolar worst-case output voltage can be obtained by:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF-IDEAL} - V_{REF-ERROR} + V_{GE}) + V_{ZSE} + INL$$

Where:

$V_{OUT-UNI}$ is output in unipolar mode, and the unit is V.

D is the code value sent to the DAC.

$V_{REF-IDEAL}$ is the ideal voltage of the reference source, the unit is V.

$V_{REF-ERROR}$ is the voltage error of the reference source, the unit is V.

V_{GE} is gain error, the unit is V.

V_{ZCE} is the zero code error, the unit is V.

INL is the integral nonlinearity error in LSB.

ZJC2542/4-18- digit code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
11 1111 1111 1111 1111	V_{REF}×(262143/262144)
10 0000 0000 0000 0000	V_{REF}×(131072/262144)=½ V_{REF}
00 0000 0000 0000 0001	V_{REF}×(1/262144)
00 0000 0000 0000 0000	0 V

ZJC2542/4-14 digital code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
11 1111 1111 1111	V_{REF}×(16383/16384)
10 0000 0000 0000	V_{REF}×(8192/16384)=½ V_{REF}
00 0000 0000 0001	V_{REF}×(1/16384)
00 0000 0000 0000	0 V

Bipolar Output

With an external op amp, the ZJC2542/4 can be used to provide a bipolar voltage output.

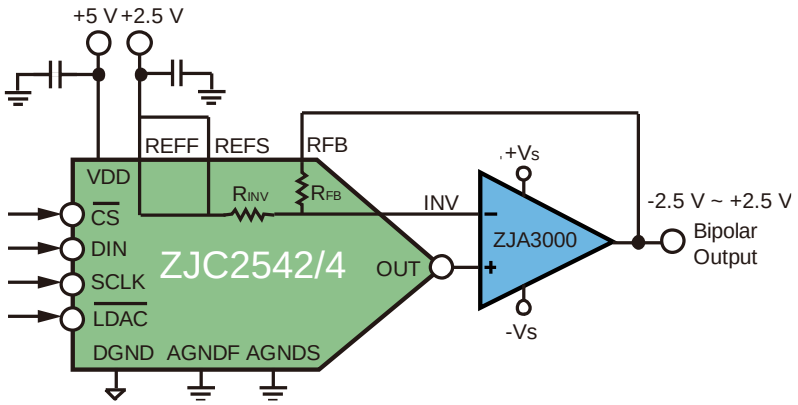

Figure 37. Typical Output Connections

For bipolar output mode, ZJC2542/4-16 digital code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
1111 1111 1111 1111	$-V_{REF}+V_{REF}\times(65535/32768)=V_{REF}-1$ LSB
1000 0000 0000 0001	$-V_{REF}+V_{REF}\times(32769/32768)$
1000 0000 0000 0000	$-V_{REF}+V_{REF}\times(32768/32768)=0$ V
0000 0000 0000 0001	$-V_{REF}+V_{REF}\times(1/32768)$
0000 0000 0000 0000	$-V_{REF}+V_{REF}\times(0/32768)=-V_{REF}$

The unipolar worst-case output voltage can be obtained by:

$$V_{OUT-BIP}=\frac{\left[\left(V_{OUT-UNI}+V_{OS-A}\right)\left(2+RD\right)-\left(V_{REF-IDEAL}-V_{REF-ERROR}\right)\left(1+RD\right)\right]}{1+\frac{\left(2+RD\right)}{A}}$$

Where:

$V_{OUT-BIP}$ is output in bipolar mode, and the unit is V.

$V_{OUT-UNI}$ is output in unipolar mode, and the unit is V.

D is the code value sent to the DAC.

$V_{REF-IDEAL}$ is the ideal voltage of the reference source, the unit is V.

$V_{REF-ERROR}$ is the voltage error of the reference source, the unit is V.

V_{OS-A} is the amplifier offset voltage, and the unit is V.

RD is the matching error of R_{FB} and R_{INV}.

A is the amplifier open loop gain.

For bipolar output mode, ZJC2542/4-18- digit code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
11 1111 1111 1111 1111	$-V_{REF}+V_{REF}\times(262143/131072)=V_{REF}$-1 LSB
10 0000 0000 0000 0001	$-V_{REF}+V_{REF}\times(131073/131072$
10 0000 0000 0000 0000	$-V_{REF}+V_{REF}\times(131072/131072)=0$ V
00 0000 0000 0000 0001	$-V_{REF}+V_{REF}\times(1/131072)$
00 0000 0000 0000 0000	$-V_{REF}+V_{REF}\times(0/131072)=-V_{REF}$

For bipolar output mode, ZJC2542/4-14 digital code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
11 1111 1111 1111	$-V_{REF}+V_{REF}\times(16383/8192)=V_{REF}$-1 LSB
10 0000 0000 0001	$-V_{REF}+V_{REF}\times(8193/8192)$
10 0000 0000 0000	$-V_{REF}+V_{REF}\times(8192/8192)=0$ V
00 0000 0000 0001	$-V_{REF}+V_{REF}\times(1/8192)$
00 0000 0000 0000	$-V_{REF}+V_{REF}\times(0/8192)=-V_{REF}$

Output Amplifier Selection

The selected op amp needs to have a very low offset voltage (For example, ZJC2542/4-16 when using 2.5 V reference voltage, 1 LSB is 38 μV) to eliminate the need for trimming the output bias. The input bias current should also be low because the bias current multiplied by the DAC output impedance (about 6.25 kΩ) will increase the zero code error. At the same time, the response of the operational amplifier should consider the settling time of the DAC. The output impedance of the DAC is constant and code independent, but to minimize gain error, the input impedance of the output amplifier should be as high as possible. The amplifier adds another time constant to the system, thus increasing the overall output settling time.

Precision operational amplifier ZJA3000 has low offset voltage (ambient temperature 35 μV), low noise (11 $nV/\sqrt{Hz}$), low input bias current (2 pA), is an excellent choice.

Reference Source And Ground

ZJC2542/4 input impedance is code dependent, so the reference pin should be driven from a low impedance source. The reference voltage range of ZJC2542/4 is 2 V~V_{DD}. The full-scale output voltage of the DAC is determined by the reference voltage.

Power On Reset

ZJC2542/4 has a power-on reset function to ensure that the output is in a known state when powered on. At power-on, the ZJC2542-18/16/14 output voltage is 0 V; the ZJC2544-18/16/14 output voltage is $V_{REF}/2$ until the latch register data is loaded from the serial register. However, the serial input register is not cleared on power-up, so its contents are undefined.

Power Supply and Reference Decoupling

For accurate high-resolution performance, it is recommended that the reference voltage and supply pins be bypassed with a 10 μF capacitor in parallel with a 0.1 μF capacitor.

Controller Interface

Controllers, like MCU or FPGA, can communicate with ZJC2542/4 through a serial bus. The communication channel requires a 3-wire interface consisting of a clock signal, a data signal, and a chip select signal. ZJC2542/4 requires a 18/16/14-bit data word, and the data is valid on the rising edge of SCLK. ZJC2542/4 voltage output can be automatically completed after all data bits are locked (chip select $\overline{CS}$ rising edge).

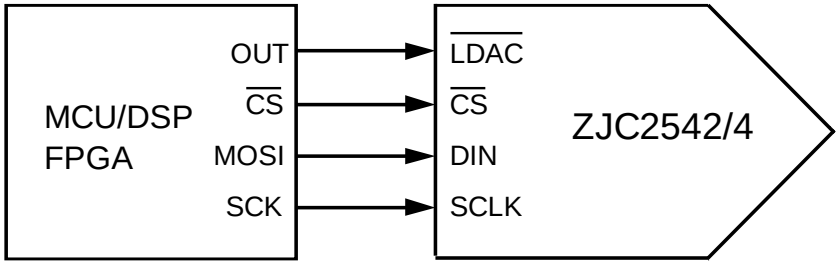

Figure 38. Connection between ZJC2542/4 and controller interface

Outline Dimensions

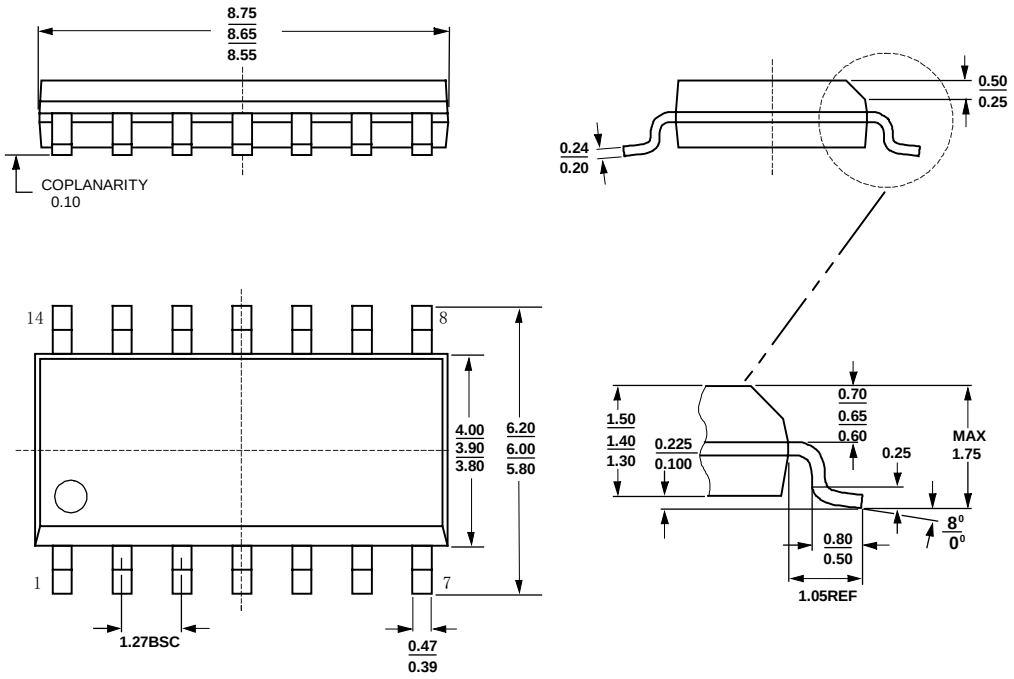

Figure 39. 14-Lead SOIC Package Dimensions shown in millimeter

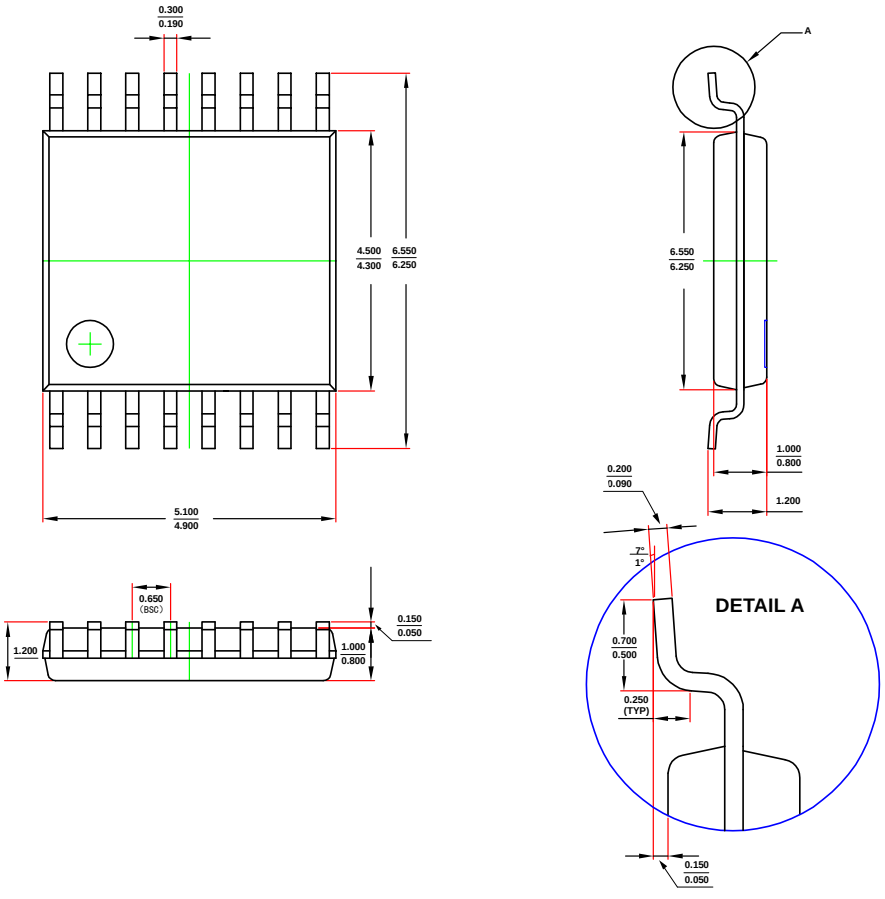

Figure 40. 16-Lead TSSOP Package Dimensions shown in millimeter

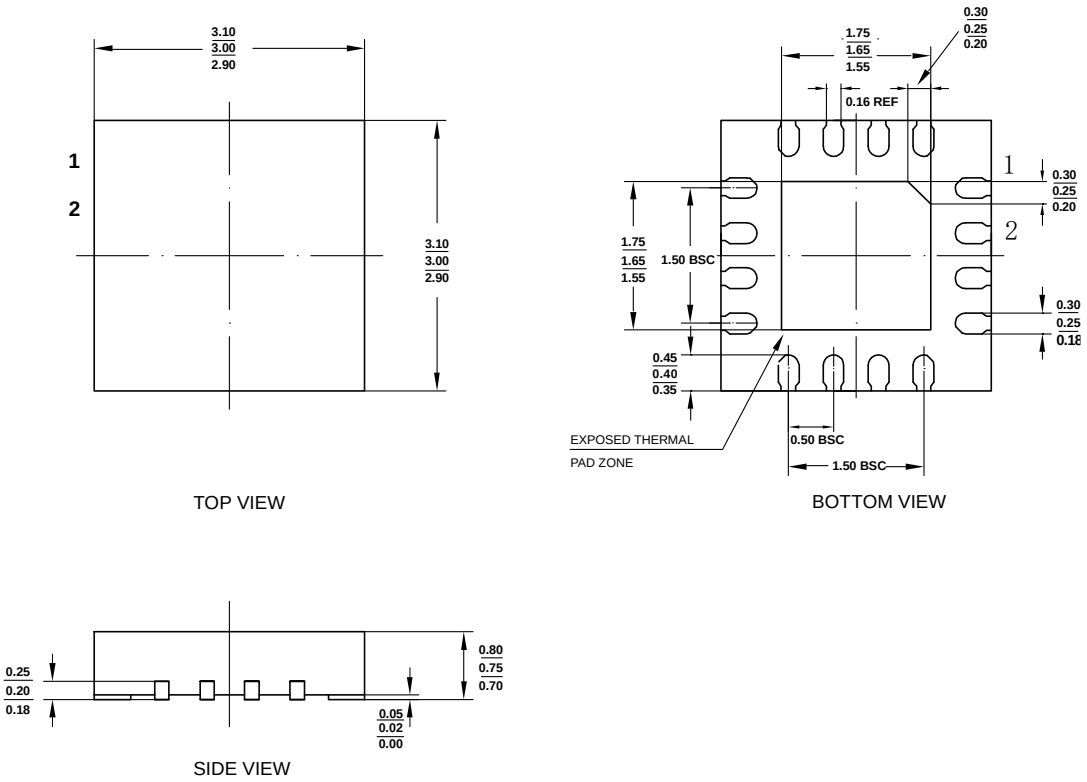

Figure 41. 16-Lead QFN Package Dimensions shown in millimeter

Ordering Guide

Model	Status[1]	Orderable Device	Package	Resolution (bit)	Silk Screen	Temperature Range (°C)	External Package
ZJC2542	ACTIVE	ZJC2542-18BSDBT	SOIC-14	18	2542-R	-40 to +125	Tube
		ZJC2542-18BSDBR	SOIC-14				13” Reel
		ZJC2542-18BUEBT	TSSOP-16				Tube
		ZJC2542-18BUEBR	TSSOP-16				13” Reel
		ZJC2542-18BTEBR	QFN-16				13” Reel
	ACTIVE	ZJC2542-16BSDBT	SOIC-14	16	2542-P	-40 to +125	Tube
		ZJC2542-16BSDBR	SOIC-14				13” Reel
		ZJC2542-16BUEBT	TSSOP-16				Tube
		ZJC2542-16BUEBR	TSSOP-16				13” Reel
		ZJC2542-16BTEBR	QFN-16				13” Reel
	ACTIVE	ZJC2542-14BSDBT	SOIC-14	14	2 542-N	-40 to +125	Tube
		ZJC2542-14BSDBR	SOIC-14				13” Reel
		ZJC2542-14BUEBT	TSSOP-16				Tube
		ZJC2542-14BUEBR	TSSOP-16				13” Reel
		ZJC2542-14BTEBR	QFN-16				13” Reel
ZJC2544	ACTIVE	ZJC2544-18BSDBT	SOIC-14	18	2544-R	-40 to +125	Tube
		ZJC2544-18BSDBR	SOIC-14				13” Reel
		ZJC2544-18BUEBT	TSSOP-16				Tube
		ZJC2544-18BUEBR	TSSOP-16				13” Reel
		ZJC2544-18BTEBR	QFN-16				13” Reel
	ACTIVE	ZJC2544-16BSDBT	SOIC-14	16	2544-P	-40 to +125	Tube
		ZJC2544-16BSDBR	SOIC-14				13” Reel
		ZJC2544-16BUEBT	TSSOP-16				Tube
		ZJC2544-16BUEBR	TSSOP-16				13” Reel
		ZJC2544-16BTEBR	QFN-16				13” Reel
	ACTIVE	ZJC2544-14BSDBT	SOIC-14	14	2544-N	-40 to +125	Tube
		ZJC2544-14BSDBR	SOIC-14				13” Reel
		ZJC2544-14BUEBT	TSSOP-16				Tube
		ZJC2544-14BUEBR	TSSOP-16				13” Reel
		ZJC2544-14BTEBR	QFN-16				13” Reel

[1] The marketing status values are defined as follows:
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
ACTIVE: Product device recommended for new designs.
NRND: Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.
LIFEBUY: ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.
OBSOLETE: ZJW has discontinued the production of the device.

Product Order Model

ZJXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T=tube; R=reel
- Temperature range: A=-40 °C to 125 °C Automotive Grade 1; B=-40 °C to 125 °C; E=-40 °C to 85 °C
- Number of Pins: K=5; T=6, A=8; B=10; D=14; E=16; P=20;
- Package type: S=SOIC; U=MSOP, TSSOP, SOT; T=DFN, QFN
- Grade: B grade is better than A grade
- Base: R=Voltage reference; A=Amplifier; C=Data Converter; G=Switch and Multiplexer; M=Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1nV-S glitch, MSOP-10/8, SOIC-8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, input to V-, RRO, 4.5 V to 36 V
ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, RRO, 4.5 V to 36 V
ZJA3512-2	Dual/Quad 36 V 7MHz precision JFET Op Amps	7 MHz GBW, 35 V/µS SR, 50 µV max Vos, 1 µV/°C max Vos drift, 2 mA/Amplifier, RRO, 9 V to 36 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G=1), 25 pA max Ibias, 25 µV max Vosi, gain error 1 ppm max (G=1), 3.3 mA Iq, ±2.4 V to ±18 V, -40 °C to 125 °C specified
ZJA3622/8	36 V low-cost precision in-amp	CMRR 93 dB min (G=10), 0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G=10), 3.3 mA Iq, ±2.4 V to ±18 V
ZJA3611, ZJA3609	36 V ultra-high precision wider bandwidth precision in-amp (min gain of 10)	CMRR 120 dB min (G=10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G=10), 3.3 mA Iq, ±2.4 V to ±18 V, -40 °C to 125 °C specified
ZJA3676/7	Low power, G=1 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min, Vos 100 µV max, gain error 15 ppm max, 500 kHz BW, 330µA/channel, 2.7 V to 36V
ZJA3100	15 V precision fully differential amplifier	145 MHz GBW, 447 V/µS SR, 16-bit settling time 50 nS, 50 µV max Vos, 4.6 mA Iq, 3 V to 15 V, SOIC/MS-8, QFN-16
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1000	15 V supply precision voltage reference	V_{OUT} = 1.25/2.048/2.5/3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MS-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection up to ±50 V power on & off, latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch<100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV