AK4468

117dB 768kHz 32-bit 8ch Premium DAC

1. General Description

The AK4468 is a new generation 32-bit 8ch Premium DAC which adopts VELVET SOUND™ technology. It corresponds to a 768 kHz PCM input and an DSD512 input at maximum, suitable for playback of high resolution audio sources that are becoming widespread in network audios, USB-DACs and Car Audio Systems. In addition, “OSR-Doubler” technology is adopted, making the AK4468 capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4468 has six types of 32-bit digital filters, realizing simple and flexible sound reproduction in wide range of applications.

Applications: AV Receivers, CD/SACD Players, Network Audio, USB DACs, USB Headphones, Sound Plate/Bars, Car Audio, Automotive External Amplifiers, Measuring Instruments and Control Systems.

2. Features

(1) Dynamic Range, S/N: 117 dB
(2) THD+N: -107 dB
(3) Differential Voltage Output: 5.6 Vpp
(4) 256x Over Sampling
(5) Sampling Rate: 8 kHz–768 kHz
(6) 32 Bit 8x Digital Filter
- Ripple: ±0.0032 dB, Attenuation: 80 dB (Sharp Roll-Off Filter Setting)
- Six Types of High Quality Sound Filter Option
  - ・Sharp Roll-off
  - ・Slow Roll-off
  - ・Short Delay Sharp Roll-off, (GD = 5.8/fs)
  - ・Short Delay Slow Roll-off, (GD = 4.8/fs)
  - ・Super Slow Roll-off
  - ・Low Dispersion Short Delay Filter

(7) High Tolerance to Clock Jitter
(8) Low Distortion/ Low Noise High Performance Differential Amplifier Output
(9) DSD64, DSD128, DSD256, DSD512 Input Support
(10) Daisy Chain
(11) Digital De-emphasis for 32 kHz, 44.1 kHz and 48 kHz sampling
(12) Soft Mute
(13) Digital Attenuator (0 dB– -127 dB, 0.5 dB step + mute)
(14) Audio I/F Format:
- MSB justified
- LSB justified
- I^2S
- DSD
- TDM

(15) PCM/DSD Automatic Switching Function
(16) 3-wire Serial and I^2C µP I/F
(17) Supports Pin Control Mode

(18) Master Clock:
- fs = 7.2 kHz-32 kHz: 256 fs, 384 fs, 512 fs, 768 fs, 1152 fs
- fs = 32 kHz-54 kHz: 256 fs, 384 fs, 512 fs, 768 fs
- fs = 54 kHz-108 kHz: 256 fs, 384 fs
- fs = 108 kHz-216 kHz: 128 fs, 192 fs
- fs = 216 kHz-388 kHz: 32 fs, 48 fs, 64 fs, 96 fs
- fs = 388 kHz-776 kHz: 16 fs, 32 fs, 48 fs, 64 fs

(19) Digital Input Level: CMOS

(20) Power Supply:
by Internal LDO (LDOE pin = "H"): TVDD = 3.0-3.6 V, AVDD = 3.0-5.5 V
by external supply (LDOE pin = "L"): TVDD = 1.7-3.6 V, AVDD = 3.0-5.5 V,
VDD18 = 1.7-1.98 V

(21) Operational Temperature: -40 to 105 °C (when the Exposed Pad is connected to AVSS)

(22) Package: 48-pin QFN

VELVET SOUND ™

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

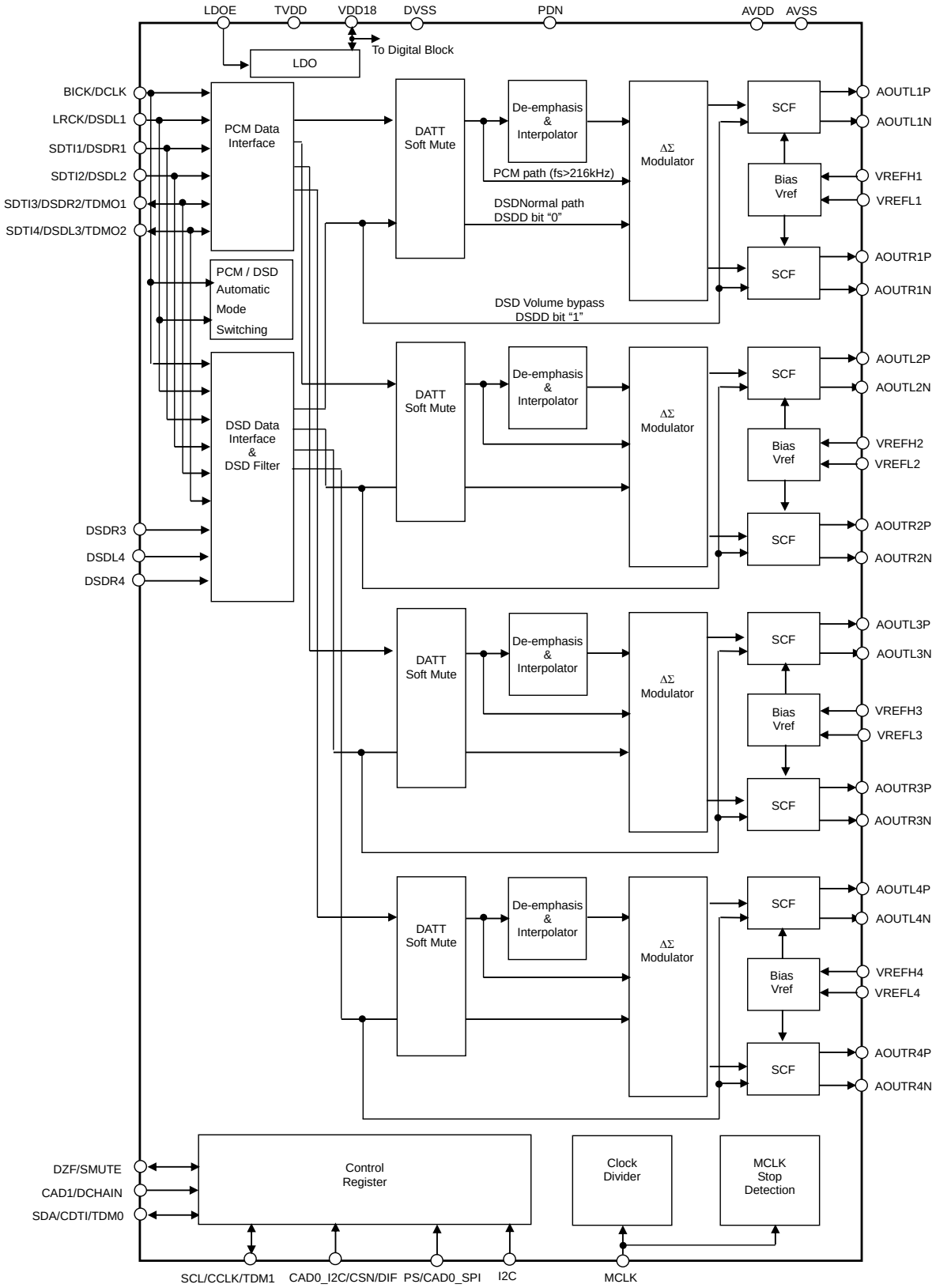


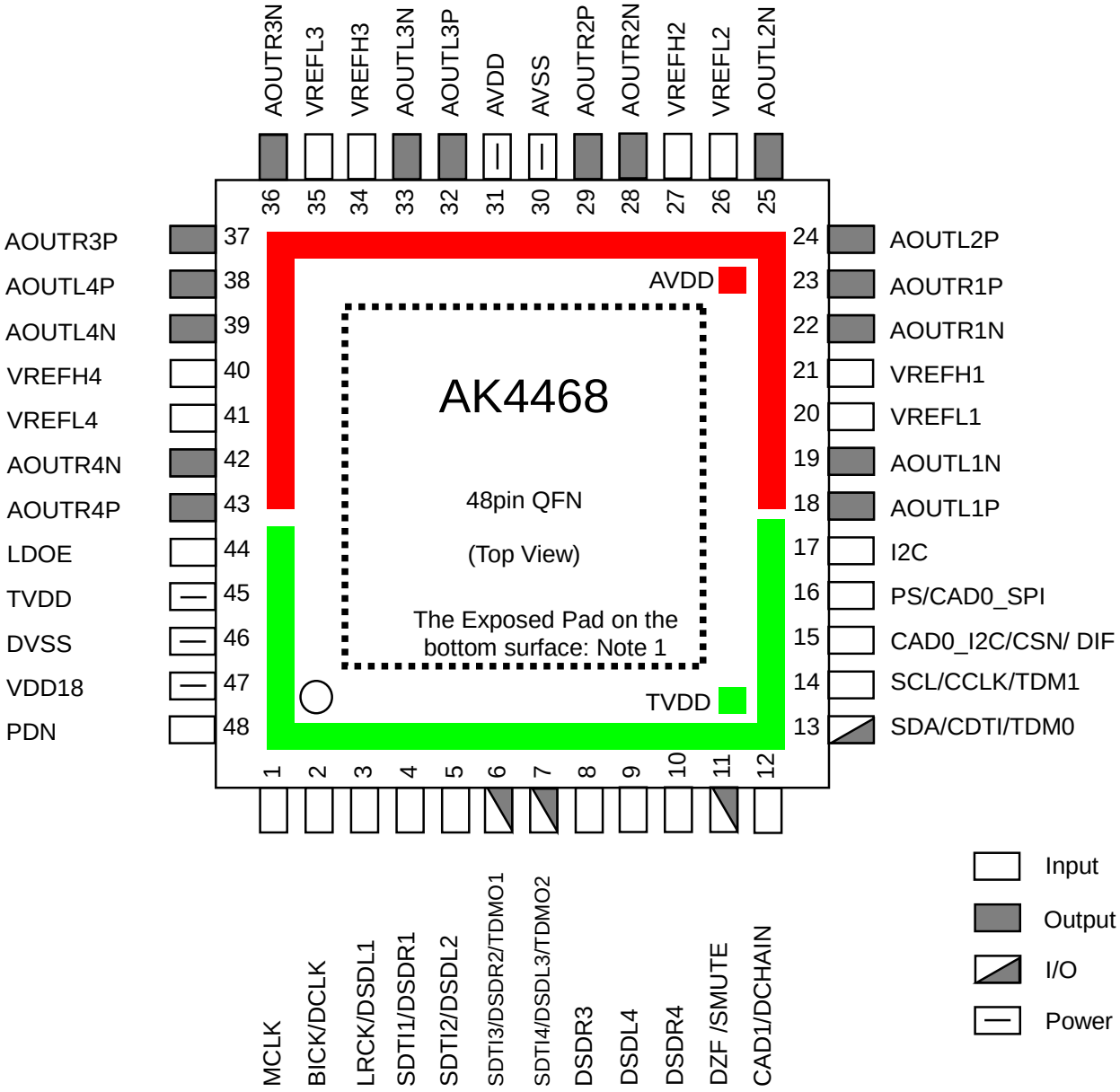
Figure 1. AK4468 Block Diagram

4.2. Functions

Block	Function
PCM Data Interface	Execute serial/parallel conversion of SDTI input data by synchronizing with LRCK and BICK.
DSD Data Interface	1-bit data that is input from DSDL1/2/3/4 and DSDR1/2/3/4 pins is received by synchronizing with DCLK.
DSD Filter	FIR filter that reduces high frequency noise of DSD input data
PCM / DSD Automatic Mode Switching	Switch PCM/DSD modes by detecting PCM or DSD mode according to the input signal.
DATT, Soft Mute	Apply DATT and Soft Mute process to input data.
ΔΣ Modulator	Output multi-bit data to SCF. This block consists of a third-order digital delta-sigma modulator.
De-emphasis & Interpolator	A digital filter that applies De-emphasis process to input data and executes over sampling.
SCF	A primary switched capacitor filter that converts a multi-bit output of ΔΣ modulator to an analog signal.
Control Register	Keep register settings for each mode. Control registers are accessed in 3-wire (CSN, CCLK, CDTI) or I^2C-Bus (SCL, SDA) control mode.
Clock Divider	Divide Master Clock In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.
MCLK Stop Detection	Detects when the master clock input is absent.
Bias, Vref	Generate SCF reference voltage from the reference voltage (VREFH1/2/3/4, VREFL1/2/3/4) that are externally supplied.
LDO	Generate power for internal digital circuit (1.8 V typ.).

5. Pin Configurations and Functions

5.1. Pin Configurations



Note 1. The Exposed Pad on the bottom surface of the package must be open or connected to AVSS. Do not connect this pin to other signal lines.

5.2. Functions

No.	Pin Name	I/O	Function	Power Down State
1	MCLK	I	External Master Clock Input Pin	Hi-Z
2	BICK	I	Audio Serial Data Clock Pin in PCM mode	Hi-Z
	DCLK	I	DSD Clock Pin in DSD mode	
3	LRCK	I	Input Channel Clock Pin in PCM mode	Hi-Z
	DSDL1	I	Audio Serial Data Input in DSD mode	
4	SDTI1	I	Audio Serial Data Input in PCM mode	Hi-Z
	DSDR1	I	Audio Serial Data Input in DSD mode	
5	SDTI2	I	Audio Serial Data Input in PCM mode	Hi-Z
	DSDL2	I	Audio Serial Data Input in DSD mode	
6	SDTI3	I	Audio Serial Data Input in PCM mode	Pull-Down to DVSS (100 kΩ)
	DSDR2	I	Audio Serial Data Input in DSD mode	
	TDMO1	O	Audio Serial Data Output in Daisy Chain mode	
7	SDTI4	I	Audio Serial Data Input in PCM mode	Pull-Down to DVSS (100 kΩ)
	DSDL3	I	Audio Serial Data Input in DSD mode	
	TDMO2	O	Audio Serial Data Output in Daisy Chain mode	
8	DSDR3	I	Audio Serial Data Input in DSD mode	Hi-Z
9	DSDL4	I	Audio Serial Data Input in DSD mode	Hi-Z
10	DSDR4	I	Audio Serial Data Input in DSD mode	Hi-Z
11	DZF	O	Zero Input Detect in Register control mode	Pull-Down to DVSS (100 kΩ)
	SMUTE	I	Soft Mute Pin in Pin control mode. When this pin is changed to “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.	
12	CAD1	I	Chip Address 1 Pin in Register control mode	Hi-Z
	DCHAIN	I	Daisy Chain Mode select pin in Pin control mode.	
13	SDA	I/O	Control Data Pin in I²C-Bus Register control mode	Hi-Z
	CDTI	I	Control Data Input Pin in 3-wire serial Register control mode	
	TDM0	I	TDM Mode select pin in Pin control mode.	
14	SCL	I	Control Data Clock Pin in I²C-Bus Register control mode	Hi-Z
	CCLK	I	Control Data Clock Pin in 3-wire serial Register control mode	
	TDM1	I	TDM Mode select pin in Pin control mode.	
15	CAD0_I2C	I	Chip Address 0 Pin in I²C-Bus Register control mode	Hi-Z
	CSN	I	Chip Select Pin in 3-wire serial Register control mode	
	DIF	I	Audio Data Format Select in Pin control mode. “L”: 32-bit MSB, “H”: 32-bit I²S	
16	PS	I	Control Mode Select Pin (I2C pin = “H”) “L”: I²C-Bus Register control mode, “H”: Pin control mode.	Hi-Z
	CAD0_SPI	I	Chip Address 0 Pin (I2C pin = “L”) In 3-wire serial Register control mode	
17	I2C	I	Control Mode Select Pin “L”: 3-wire serial Register control mode “H”: I²C-Bus Register control mode or Pin control mode.	Hi-Z
18	AOUTL1P	O	Lch Positive Analog Output 1 Pin	Hi-Z
19	AOUTL1N	O	Lch Negative Analog Output 1 Pin	Hi-Z
20	VREFL1	I	Negative Reference Voltage Input 1 Pin	Hi-Z
21	VREFH1	I	Positive Reference Voltage Input 1 Pin	Hi-Z
22	AOUTR1N	O	Rch Negative Analog Output 1 Pin	Hi-Z
23	AOUTR1P	O	Rch Positive Analog Output 1 Pin	Hi-Z
24	AOUTL2P	O	Lch Positive Analog Output 2 Pin	Hi-Z

No.	Pin Name	I/O	Function	Power Down State
25	AOUTL2N	O	Lch Negative Analog Output 2 Pin	Hi-Z
26	VREFL2	I	Negative Reference Voltage Input 2 Pin	Hi-Z
27	VREFH2	I	Positive Reference Voltage Input 2 Pin	Hi-Z
28	AOUTR2N	O	Rch Negative Analog Output 2 Pin	Hi-Z
29	AOUTR2P	O	Rch Positive Analog Output 2 Pin	Hi-Z
30	AVSS	-	Ground Pin	-
31	AVDD	-	Analog Power Supply Pin, 3.0–5.5 V	-
32	AOUTL3P	O	Lch Positive Analog Output 3 Pin	Hi-Z
33	AOUTL3N	O	Lch Negative Analog Output 3 Pin	Hi-Z
34	VREFH3	I	Positive Reference Voltage Input 3 Pin	Hi-Z
35	VREFL3	I	Negative Reference Voltage Input 3 Pin	Hi-Z
36	AOUTR3N	O	Rch Negative Analog Output 3 Pin	Hi-Z
37	AOUTR3P	O	Rch Positive Analog Output 3 Pin	Hi-Z
38	AOUTL4P	O	Lch Positive Analog Output 4 Pin	Hi-Z
39	AOUTL4N	O	Lch Negative Analog Output 4 Pin	Hi-Z
40	VREFH4	I	Positive Reference Voltage Input 4 Pin	Hi-Z
41	VREFL4	I	Negative Reference Voltage Input 4 Pin	Hi-Z
42	AOUTR4N	O	Rch Negative Analog Output 4 Pin	Hi-Z
43	AOUTR4P	O	Rch Positive Analog Output 4 Pin	Hi-Z
44	LDOE	I	Internal LDO Enable Pin. “L”: Disable, “H”: Enable	Hi-Z
45	TVDD	-	Digital Power Supply Pin, 3.0–3.6 V	-
46	DVSS	-	Ground Pin	-
47	VDD18	O	LDO Output Pin (LDOE pin = “H”) This pin should be connected to DVSS with 1.0 µF (±50 %). This pin is prohibited from connecting with other devices.	Pull-down to DVSS (500 Ω)
		-	1.8 V Power Input Pin (LDOE pin = “L”)	Hi-Z
48	PDN	I	Power-Up, Power-Down Pin When at “L”, the AK4468 is in power-down state. The AK4468 must always be in power-down state upon power on.	Hi-Z (PDN = “L”)
-	Exposed Pad	-	The Exposed Pad on the bottom surface of the package must be open or connected to AVSS. Do not connect this pin to other signal lines.	-

Note 2. All input pins except internal pull-up/down pins must not be left floating.
Note 3. The AK4468 must be powered down by the PDN pin when changing the PS pin and the I2C pin settings.
Note 4. DSD mode is selectable only in Register Control Mode. Daisy Chain Mode is selectable both Pin Control Mode and Register Control Mode.

5.3. Handling of Unused Pin

5.3.1. Pin Control Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTL1P/N, AOUTR1P/N AOUTL2P/N, AOUTR2P/N AOUTL3P/N, AOUTR3P/N AOUTL4P/N, AOUTR4P/N	Open
	VREFH1/2/3/4	Connect to AVDD or AVSS
	VREFL1/2/3/4	Connect to AVSS
Digital	SDTI1/2/3/4, DSDR3/4, DSDL4	Connect to DVSS
	TDMO2	Open

5.3.2. Register Control Mode

5.3.2.1. PCM mode

Classification	Pin Name	Setting
Analog	AOUTL1P/N, AOUTR1P/N AOUTL2P/N, AOUTR2P/N AOUTL3P/N, AOUTR3P/N AOUTL4P/N, AOUTR4P/N	Open
	VREFH1/2/3/4	Connect to AVDD or AVSS
	VREFL1/2/3/4	Connect to AVSS
Digital	DZF	Open
	SDTI1/2/3/4, DSDR3/4, DSDL4	Connect to DVSS
	TDMO2	Open

5.3.2.2. DSD mode

Classification	Pin Name	Setting
Analog	AOUTL1P/N, AOUTR1P/N AOUTL2P/N, AOUTR2P/N AOUTL3P/N, AOUTR3P/N AOUTL4P/N, AOUTR4P/N	Open
	VREFH1/2/3/4	Connect to AVDD or AVSS
	VREFL1/2/3/4	Connect to AVSS
Digital	DZF	Open
	DSDL1/2/3/4, DSDR1/2/3/4	Connect to DVSS

5.3.3. Pull-down pin List

Classification	Pin Name	Internal connection
pull-down pin (Typ = 100 kΩ)	SDTI3/4, SMUTE	DVSS

6. Absolute Maximum Ratings

(AVSS = DVSS = 0 V; Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	–0.3	6.0	V
	Digital I/O	TVDD	–0.3	4.0	V
	Digital Core	VDD18	–0.3	2.5	V
	|AVSS – DVSS| (Note 6)	ΔGND	-	0.3	V
Reference Voltage (Note 7)	High VREF	VREFH 1/2/3/4	AVSS–0.3	AVDD+0.3 or 6.0	V
	Low VREF	VREFL 1/2/3/4	AVSS–0.3	AVSS+0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 8)		VIND	–0.3	TVDD+0.3 or 4.0	V
Ambient Temperature (Power applied)					
Exposed Pad: Connected to AVSS		Ta	–40	105	°C
Exposed Pad: Open		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 5. All voltages are with respect to ground.
Note 6. AVSS and DVSS must be connected to the same analog ground plane.
Note 7. Maximum input voltage of VREFH1/2/3/4 pins is lower value between (AVDD+0.3) V and 6.0 V.
Note 8. Maximum input voltage of digital input pins is lower value between (TVDD+0.3) V and 4.0 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = 0 V; Note 5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	(LDOE pin = "L"; Note 9)					
	Analog	AVDD	3.0	5.0	5.5	V
	Digital I/O	TVDD	VDD18	1.8	3.6	V
	Digital Core	VDD18	1.7	1.8	1.98	V
	(LDOE pin = "H"; Note 10)					
	Analog	AVDD	3.0	5.0	5.5	V
	Digital I/O	TVDD	3.0	3.3	3.6	V
Reference Voltage (Note 11)	High VREF	VREFH 1/2/3/4	AVDD–0.5	-	AVDD	V
	Low VREF	VREFL 1/2/3/4	-	AVSS	-	V

Note 9. When the LDOE pin = "L", VDD18 must be supplied at the same time as or after TVDD. The power up sequence between AVDD and TVDD or AVDD and VDD18 is not critical.
Note 10. When the LDOE pin = "H", the internal LDO supplies 1.8 V (typ). The power up sequence between AVDD and TVDD is not critical.
Note 11. VREFH1/2/3/4 must be input at the same time as or after AVDD.

8. Electrical Characteristics

8.1. Analog Characteristics

8.1.1. PCM Mode (AVDD = 5.0 V)

(Ta = 25 °C; LDOE pin = "H", TVDD = 3.3 V, AVDD = 5.0 V; AVSS = DVSS = 0 V; VREFH1/2/3/4 = 5.0 V, VREFL1/2/3/4 = 0 V; fs = 44.1 kHz; BICK = 64 fs; Signal Frequency = 1 kHz; 32-bit Input Data; RL ≥ 1.4 kΩ; measurement bandwidth = 20 Hz-20 kHz; External Circuit: (Figure 76); unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution			-	-	32	bit
Dynamic Characteristics		(Note 12)				
THD+N	fs = 44.1 kHz	0 dBFS	-	-107	-100	dB
	BW = 20 kHz	–60 dBFS	-	-54	-	dB
	fs = 96 kHz	0 dBFS	-	-104	-	dB
	BW = 40 kHz	–60 dBFS	-	-50	-	dB
	fs = 192/384/768 kHz	0 dBFS	-	-104	-	dB
	BW = 40 kHz	–60 dBFS	-	-50	-	dB
	BW = 80 kHz	–60 dBFS	-	-46	-	dB
Dynamic Range (–60 dBFS with A-weighted)		(Note 13)	-	117	-	dB
S/N (A-weighted)			112	117	-	dB
Interchannel Isolation (1 kHz)			100	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift		(Note 14)	-	20	-	ppm/°C
Differential Output Voltage		(Note 15)	5.3	5.6	5.9	Vpp
Load Resistance		(Note 16)	1.4	-	-	kΩ
Load Capacitance		(Note 17)	-	-	30	pF
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H") (LDOE pin = "L", VDD18 = 1.8 V)						
AVDD			-	43	59	mA
TVDD			-	1	1.2	mA
VDD18 (fs = 44.1 kHz)			-	8	13	mA
VDD18 (fs = 96 kHz)			-	13	20	mA
VDD18 (fs = 192 kHz)			-	20	31	mA
VDD18 (fs = 384 kHz)			-	7	-	mA
VDD18 (fs = 768 kHz)			-	10	-	mA
(LDOE pin = "H")						
AVDD			-	43	59	mA
TVDD (fs = 44.1 kHz)			-	9	15	mA
TVDD (fs = 96 kHz)			-	14	22	mA
TVDD (fs = 192 kHz)			-	21	33	mA
TVDD (fs = 384 kHz)			-	8	-	mA
TVDD (fs = 768 kHz)			-	11	-	mA
Power down (PDN pin = "L")		(Note 18)				
AVDD+TVDD			-	1	400	μA
VREF Supplies						
VREF Supply Current (VREFH1+VREFH2+VREFH3+VREFH4)						
Normal operation (PDN pin = "H")			-	0.5	0.9	mA

Note 12. Measured by Audio Precision APx555, averaging mode.

Note 13. When using the circuit shown in Figure 76. 100 dB at 16-bit data.
Note 14. The voltage of (VREFH1/2/3/4 - VREFL1/2/3/4) is held at 5 V.
Note 15. The output voltage scale with the voltage of (VREFH1/2/3/4 - VREFL1/2/3/4).
DAC1: AOUTL1/R1 (typ.@0dB) = (AOUTL1P/R1P) − (AOUTL1N/R1N) = 1.12Vpp × (VREFH1 − VREFL1)
DAC2: AOUTL2/R2 (typ.@0dB) = (AOUTL2P/R2P) − (AOUTL2N/R2N) = 1.12Vpp × (VREFH2 − VREFL2)
DAC3: AOUTL3/R3 (typ.@0dB) = (AOUTL3P/R3P) − (AOUTL3N/R3N) = 1.12Vpp × (VREFH3 − VREFL3)
DAC4: AOUTL4/R4 (typ.@0dB) = (AOUTL4P/R4P) − (AOUTL4N/R4N) = 1.12Vpp × (VREFH4 − VREFL4)
Note 16. The load resistance value is without a DC cut capacitor, and is with respect to ground. The AC load is 1.0 kΩ (min) with a DC cut capacitor.
Note 17. Load Capacitance value is with respect to ground.
Note 18. All other digital input pins including clock pins, (MCLK, BICK and LRCK), are held to DVSS.

8.1.2. PCM Mode (AVDD = 3.3 V)

(Ta = 25 °C; LDOE pin = "H", TVDD = 3.3 V, AVDD = 3.3 V; AVSS = DVSS = 0 V; VREFH1/2/3/4 = 3.3 V, VREFL1/2/3/4 = 0 V; fs = 44.1 kHz; BICK = 64 fs; Signal Frequency = 1 kHz; 32-bit Input Data; RL ≥ 1.4 kΩ; measurement bandwidth = 20 Hz-20 kHz; External Circuit (Figure 76); unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution			-	-	32	bit
Dynamic Characteristics		(Note 12)				
THD+N	fs = 44.1 kHz, BW = 20 kHz	0 dBFS	-	-100	-93	dB
		–60 dBFS	-	-50	-	dB
	fs = 96 kHz, BW = 40 kHz	0 dBFS	-	-99	-	dB
		–60 dBFS	-	-46	-	dB
	fs = 192/384/768 kHz, BW = 40 kHz	0 dBFS	-	-99	-	dB
		–60 dBFS	-	-46	-	dB
	BW = 80 kHz	–60 dBFS	-	-42	-	dB
Dynamic Range (–60 dBFS with A-weighted)		(Note 13)	-	113	-	dB
S/N (A-weighted)			108	113	-	dB
Interchannel Isolation (1 kHz)			100	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift		(Note 19)	-	20	-	ppm/°C
Differential Output Voltage		(Note 15)	3.32	3.7	4.08	Vpp
Load Resistance		(Note 16)	1.4	-	-	kΩ
Load Capacitance		(Note 17)	-	-	30	pF
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H") (LDOE pin = "L", VDD18 = 1.8 V)						
AVDD			-	35	49	mA
TVDD			-	1	1.2	mA
VDD18 (fs = 44.1 kHz)			-	8	13	mA
VDD18 (fs = 96 kHz)			-	13	20	mA
VDD18 (fs = 192 kHz)			-	20	31	mA
VDD18 (fs = 384 kHz)			-	7	-	mA
VDD18 (fs = 768 kHz)			-	10	-	mA
(LDOE pin = "H")						
AVDD			-	35	49	mA
TVDD (fs = 44.1 kHz)			-	9	15	mA
TVDD (fs = 96 kHz)			-	14	22	mA
TVDD (fs = 192 kHz)			-	21	33	mA
TVDD (fs = 384 kHz)			-	8	-	mA
TVDD (fs = 768 kHz)			-	11	-	mA
Power down (PDN pin = "L")		(Note 18)				
AVDD+TVDD			-	1	400	μA
VREF Supplies						
VREF Supply Current (VREFH1+VREFH2+VREFH3+VREFH4)						
Normal operation (PDN pin = "H")			-	0.4	0.9	mA

Note 19. The voltage of (VREFH1/2/3/4 - VREFL1/2/3/4) is held at 3.3 V.

8.1.3. DSD mode

(Ta = 25°C: LDOE pin = "H", TVDD = 3.3 V, AVDD = 5.0 V: AVSS = DVSS = 0 V: VREFH1/2/3/4 = 5.0 V, VREFL1/2/3/4 = 0 V: fs = 44.1 kHz: Signal Frequency = 1 kHz: RL ≥ 1.4 kΩ: measurement bandwidth = 20 Hz-20 kHz: External Circuit: (Figure 76): unless otherwise specified.)

Parameter			Min	Typ	Max	Unit
Dynamic Characteristics						
THD+N	DSD data stream: DSD64	0dB (Note 20)	-	-107	-	dB
	DSD data stream: DSD128	0dB (Note 20)	-	-107	-	dB
	DSD data stream: DSD256	0dB (Note 20)	-	-107	-	dB
	DSD data stream: DSD512	0dB (Note 20)	-	-107	-	dB
S/N (A-weighted, Normal path)	DSD data stream: DSD64	Digital "0" (Note 21)	-	116	-	dB
	DSD data stream: DSD128	Digital "0" (Note 21)	-	116	-	dB
	DSD data stream: DSD256	Digital "0" (Note 21)	-	116	-	dB
	DSD data stream: DSD512	Digital "0" (Note 21)	-	116	-	dB
DC Accuracy						
Differential Output Voltage (Normal path) (Note 22)			-	5.0	-	Vpp
Differential Output Voltage (Volume Bypass) (Note 22)			-	5.0	-	Vpp

Note 20. The output level is assumed as 0 dB when a 1 kHz 25%-75% duty sine wave is input. Click noise may occur if the input signal exceeds 0 dB.

Note 21. Digital "0" is a "01101001" digital zero code pattern.

Note 22. The analog output voltage at 25%-75% input signal duty is calculated by the following equation:

DAC1: AOUTL1/R1 (typ.@0dB) = (AOUTL1P/R1P) – (AOUTL1N/R1N) = 1.0Vpp × (VREFH1 – VREFL1)
DAC2: AOUTL2/R2 (typ.@0dB) = (AOUTL2P/R2P) – (AOUTL2N/R2N) = 1.0Vpp × (VREFH2 – VREFL2)
DAC3: AOUTL3/R3 (typ.@0dB) = (AOUTL3P/R3P) – (AOUTL3N/R3N) = 1.0Vpp × (VREFH3 – VREFL3)
DAC4: AOUTL4/R4 (typ.@0dB) = (AOUTL4P/R4P) – (AOUTL4N/R4N) = 1.0Vpp × (VREFH4 – VREFL4)

8.2. DAC Digital-Filter Characteristics (PCM Mode)

8.2.1. Sharp Roll-Off Filter Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; DEM[1:0] bits = "01"(OFF), ADPE bit = "0", SYNCE bit = "1", SLOW bit = "0", SD bit = "0", SSLOW bit = "0")

・fs = 44.1 kHz (Normal Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	20.0	kHz
	−3.0 dB	-	-	21.5	-	kHz
Pass band	(Note 24)	PB	0	-	20.0	kHz
Stop band	(Note 24)	SB	24.1	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.0032	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	26.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–20.0 kHz		-	-0.2	-	0.1	dB

・fs = 96 kHz (Double Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	43.5	kHz
	−3.0 dB	-	-	46.8	-	kHz
Pass band	(Note 24)	PB	0	-	43.5	kHz
Stop band	(Note 24)	SB	52.5	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.0032	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	26.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–40.0 kHz		-	-0.6	-	0.1	dB

・fs = 192 kHz (Quad Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	87.0	kHz
	−3.0 dB	-	-	93.6	-	kHz
Pass band	(Note 24)	PB	0	-	87.0	kHz
Stop band	(Note 24)	SB	105	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.0032	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	26.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–80.0 kHz		-	-2.0	-	0.1	dB

Note 23. Frequency response refers to the output level of 1 kHz. Stopband attenuation band ranges from SB to fs.

Note 24. The passband and stopband frequencies scale with fs. For example, PB = 0.454 × fs(@±0.05 dB), SB = 0.546 × fs.

Note 25. This value is the gain ripple in pass band width.

Note 26. The calculating delay time which occurred by digital filtering. This value is from setting the 16/20/24/32-bit data of both channels to the output of analog signal.

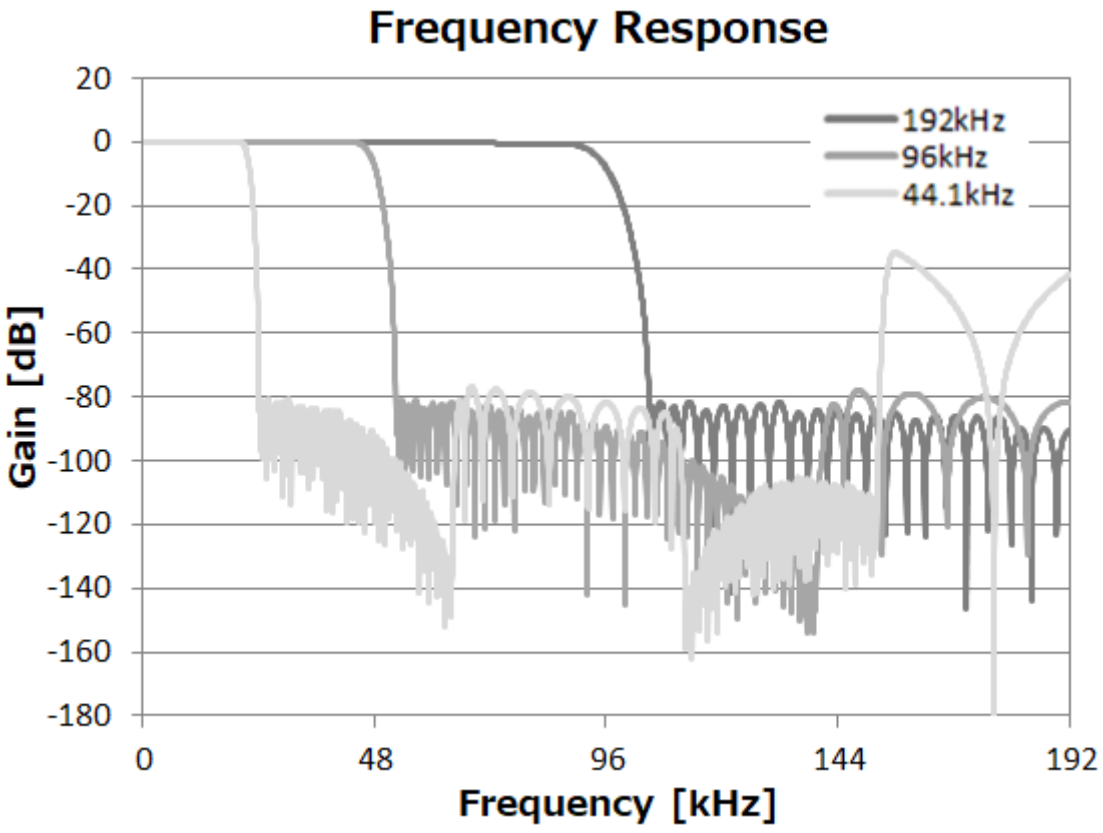


Figure 2. Sharp Roll-off Filter Frequency Response

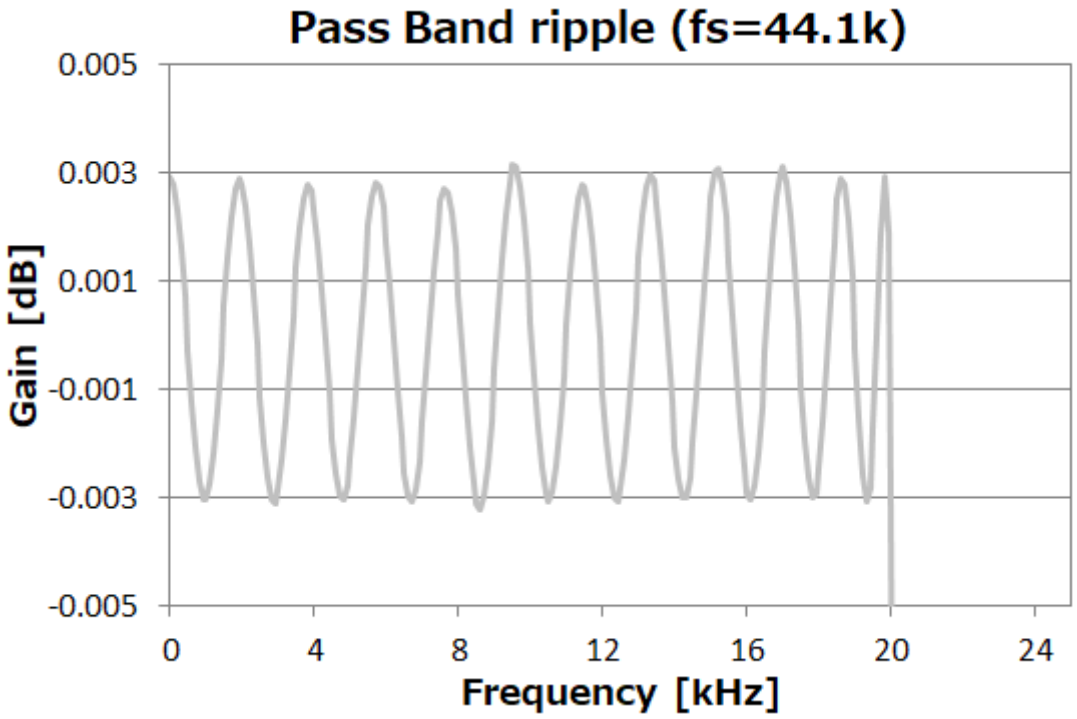


Figure 3. Sharp Roll-off Filter Passband Ripple

8.2.2. Slow Roll-Off Filter Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; DEM[1:0] bits = "01"(OFF), ADPE bit = "0", SYNCE bit = "1", SLOW bit = "1", SD bit = "0", SSLOW bit = "0")

・fs = 44.1 kHz (Normal Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	8.1	kHz
	−3.0 dB	-	-	18.2	-	kHz
Pass band	(Note 27)	PB	0	-	8.1	kHz
Stop band	(Note 27)	SB	39.2	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.043	dB
Stop band Attenuation	(Note 23)	SA	73	-	-	dB
Group Delay	(Note 26)	GD	-	6.3	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–20.0 kHz		-	-5.0	-	+0.1	dB

・fs = 96 kHz (Double Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	17.7	kHz
	−3.0 dB	-	-	39.5	-	kHz
Pass band	(Note 27)	PB	0	-	17.7	kHz
Stop band	(Note 27)	SB	85.3	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.043	dB
Stop band Attenuation	(Note 23)	SA	73	-	-	dB
Group Delay	(Note 26)	GD	-	6.3	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–40.0 kHz		-	-5.0	-	+0.1	dB

・fs = 192 kHz (Quad Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	35.5	kHz
	−3.0 dB	-	-	79.0	-	kHz
Pass band	(Note 27)	PB	0	-	35.5	kHz
Stop band	(Note 27)	SB	171	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.043	dB
Stop band Attenuation	(Note 23)	SA	73	-	-	dB
Group Delay	(Note 26)	GD	-	6.3	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–80.0 kHz		-	-5.0	-	+0.1	dB

Note 27. The passband and stopband frequencies scale with fs. For example, PB = 0.184 × fs(@±0.05 dB), SB = 0.888 × fs.

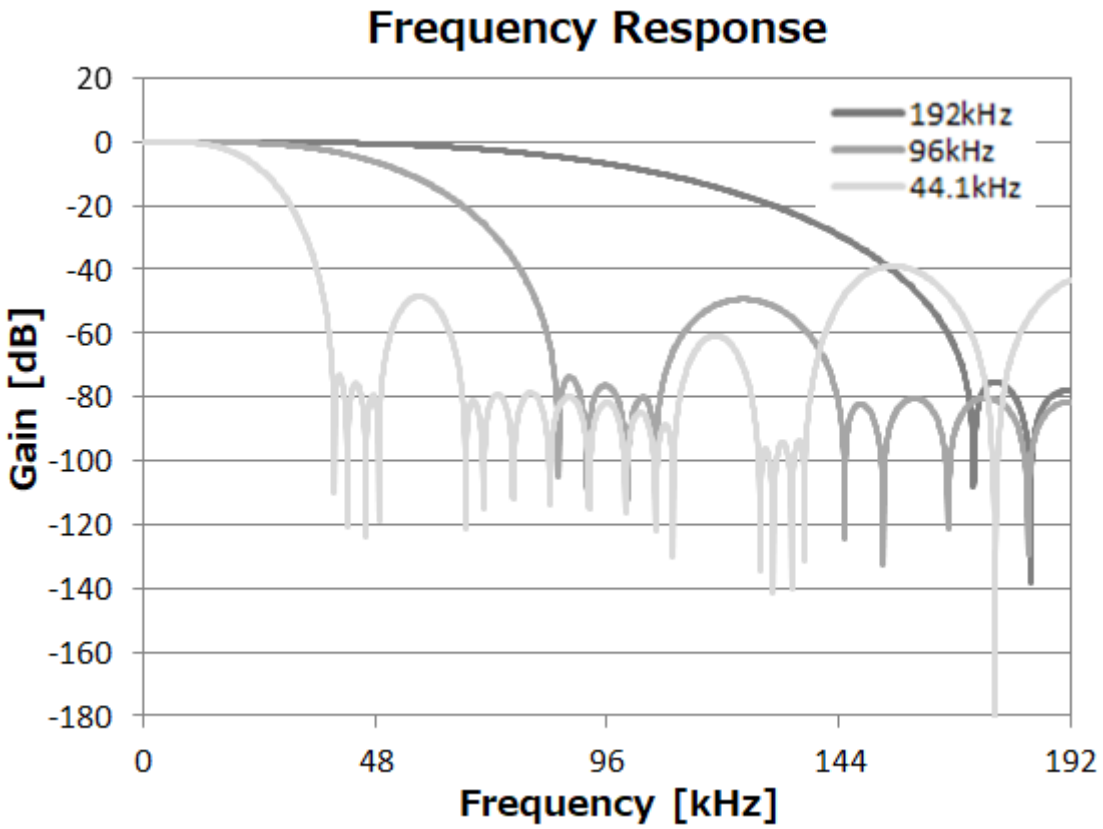


Figure 4. Slow Roll-off Filter Frequency Response

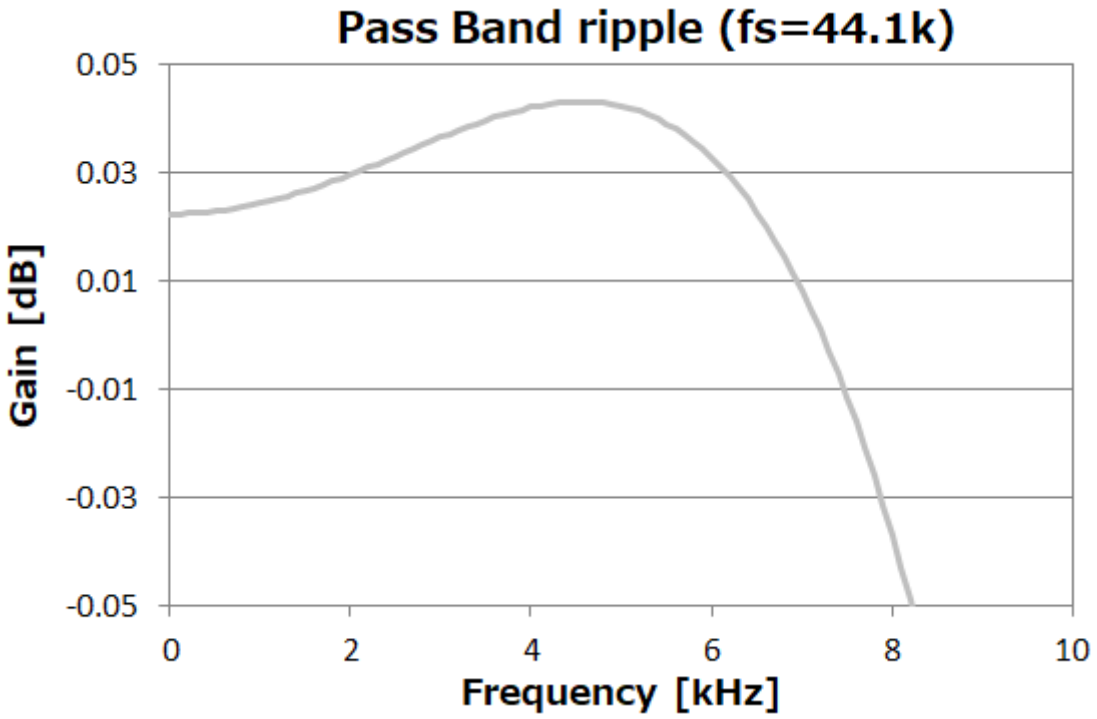


Figure 5. Slow Roll-off Filter Passband Ripple

8.2.3. Short Delay Sharp Roll-Off Filter Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; DEM[1:0] bits = "01"(OFF), ADPE bit = "0", SYNCE bit = "1", SLOW bit = "0", SD bit = "1", SSLOW bit = "0")

・fs = 44.1 kHz (Normal Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	20.0	kHz
	−3.0 dB	-	-	21.5	-	kHz
Pass band	(Note 28)	PB	0	-	20.0	kHz
Stop band	(Note 28)	SB	24.1	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.0031	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	5.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–20.0 kHz		-	-0.2	-	+0.1	dB

・fs = 96 kHz (Double Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	43.5	kHz
	−3.0 dB	-	-	46.8	-	kHz
Pass band	(Note 28)	PB	0	-	43.5	kHz
Stop band	(Note 28)	SB	52.5	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.0031	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	5.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–40.0 kHz		-	-0.6	-	+0.1	dB

・fs = 192 kHz (Quad Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	87.0	kHz
	−3.0 dB	-	-	93.6	-	kHz
Pass band	(Note 28)	PB	0	-	87.0	kHz
Stop band	(Note 28)	SB	105	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.0031	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	5.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–80.0 kHz		-	-2.0	-	+0.1	dB

Note 28. The passband and stopband frequencies scale with fs. For example, PB = 0.453 × fs(@±0.05 dB), SB = 0.547 × fs.

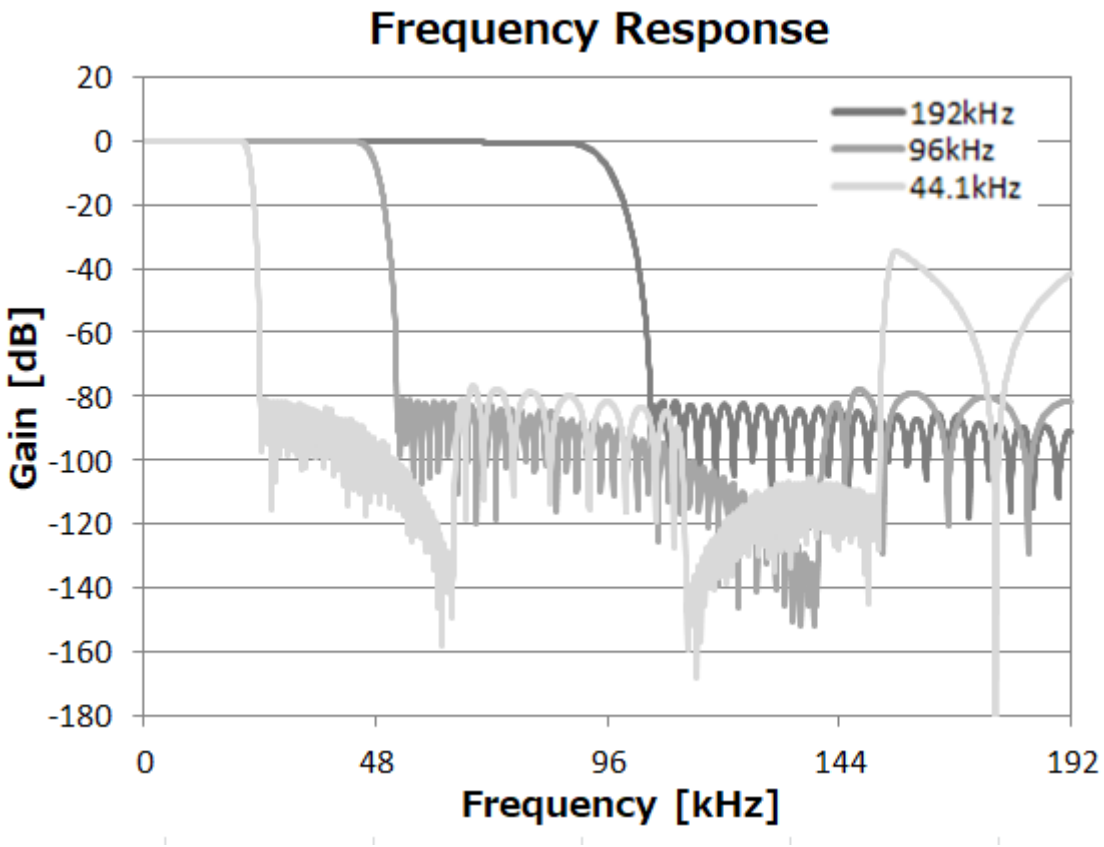


Figure 6. Short-delay Sharp Roll-off Filter Frequency Response

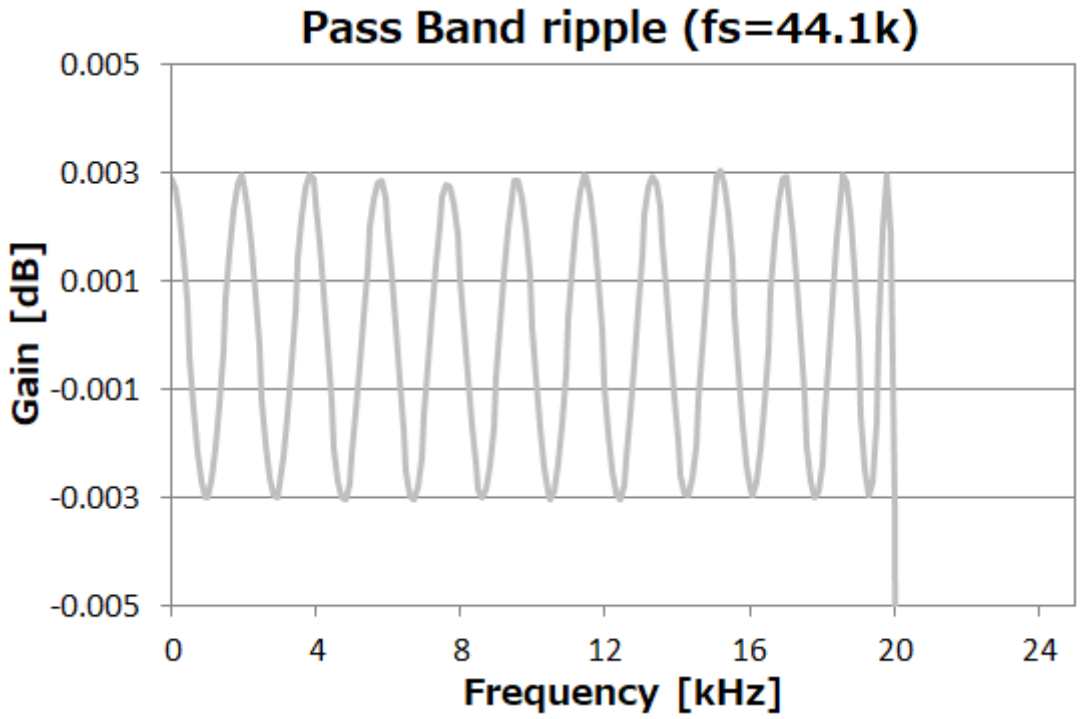


Figure 7. Short-delay Sharp Roll-off Filter Passband Ripple

8.2.4. Short Delay Slow Roll-Off Filter Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; DEM[1:0] bits = "01"(OFF), ADPE bit = "0", SYNCE bit = "1", SLOW bit = "1", SD bit = "1", SSLOW bit = "0")

・fs = 44.1 kHz (Normal Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	11.1	kHz
	−3.0 dB	-	-	19.4	-	kHz
Pass band	(Note 29)	PB	0	-	11.1	kHz
Stop band	(Note 29)	SB	38.1	-	-	kHz
Pass band Ripple	(Note 25)	PR		-	±0.05	dB
Stop band Attenuation	(Note 23)	SA	82	-	-	dB
Group Delay	(Note 26)	GD	-	4.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–20.0 kHz		-	-5.0	-	+0.1	dB

・fs = 96 kHz (Double Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	24.2	kHz
	−3.0 dB	-	-	42.1	-	kHz
Pass band	(Note 29)	PB	0	-	24.2	kHz
Stop band	(Note 29)	SB	83	-	-	kHz
Pass band Ripple	(Note 25)	PR		-	±0.05	dB
Stop band Attenuation	(Note 23)	SA	82	-	-	dB
Group Delay	(Note 26)	GD	-	4.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–40.0 kHz		-	-5.0	-	+0.1	dB

・fs = 192 kHz (Quad Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	48.4	kHz
	−3.0 dB	-	-	84.3	-	kHz
Pass band	(Note 29)	PB	0	-	48.4	kHz
Stop band	(Note 29)	SB	165.9	-		kHz
Pass band Ripple	(Note 25)	PR		-	±0.05	dB
Stop band Attenuation	(Note 23)	SA	82	-	-	dB
Group Delay	(Note 26)	GD	-	4.8	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–80.0 kHz		-	-5.0	-	+0.1	dB

Note 29. The passband and stopband frequencies scale with fs. For example, PB = 0.252 × fs(@±0.05 dB), SB = 0.864 × fs.

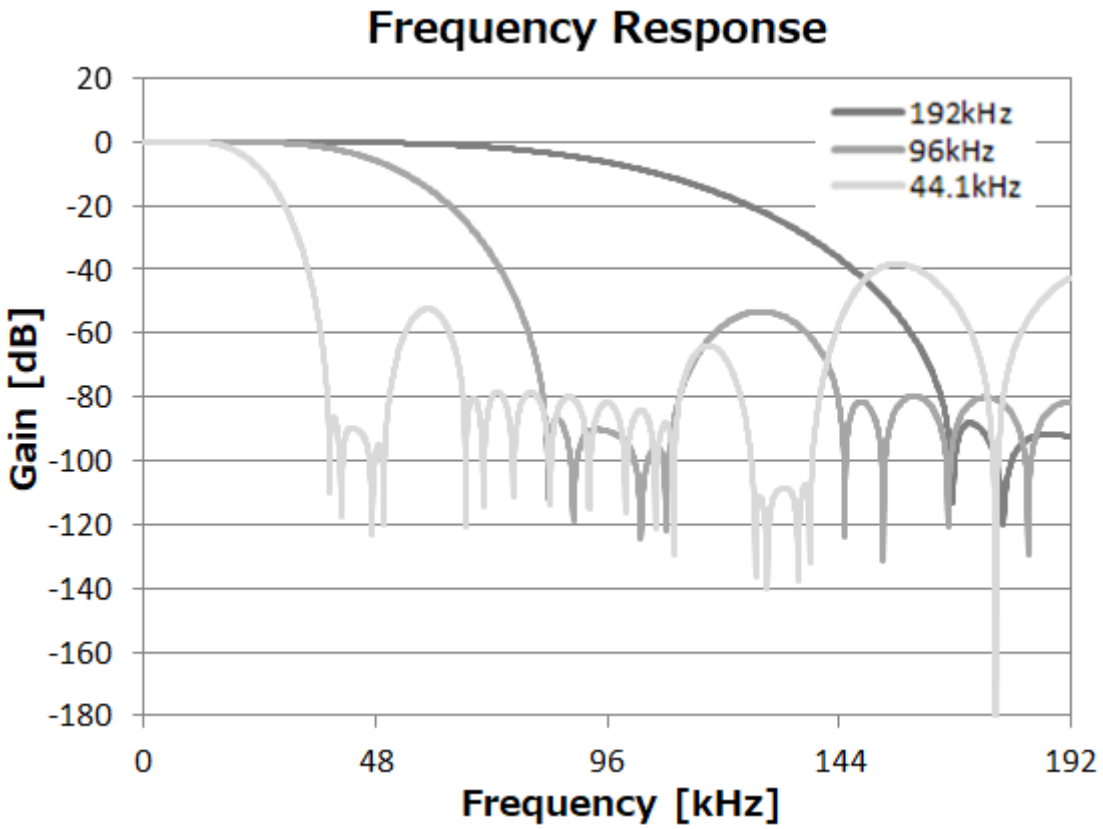


Figure 8. Short-delay Slow Roll-off Filter Frequency Response

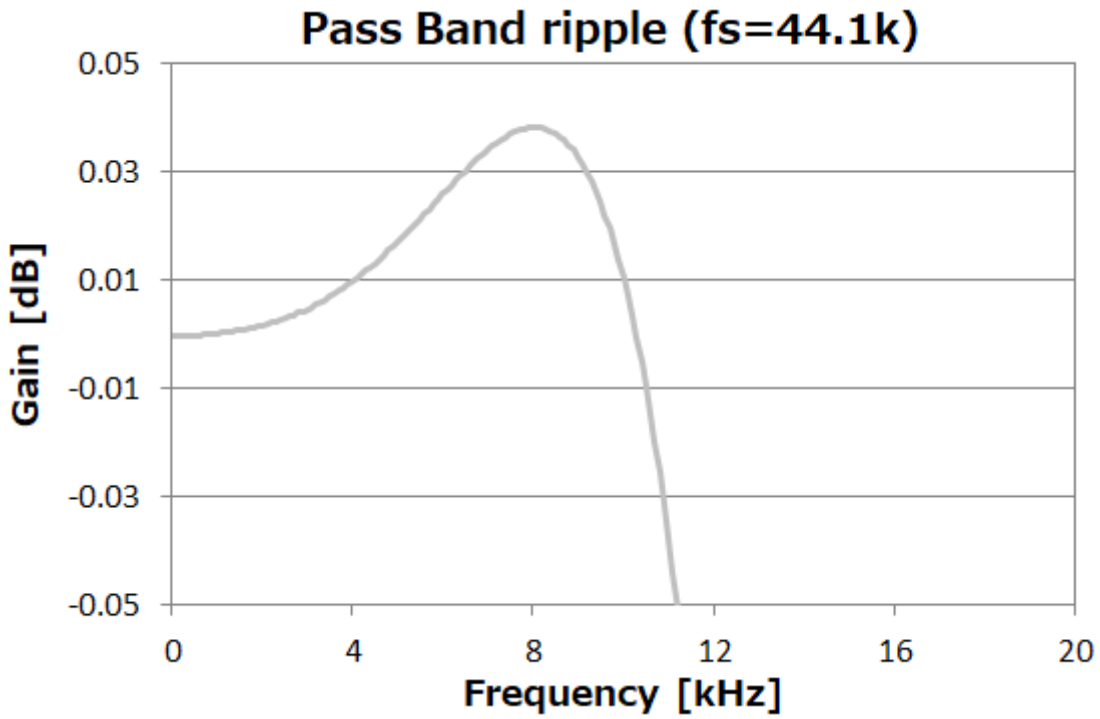


Figure 9. Short-delay Slow Roll-off Filter Passband Ripple

8.2.5. Low-dispersion Short Delay Filter Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; DEM[1:0] bits = "01"(OFF), ADPE bit = "0", SYNCE bit = "1", SLOW bit = "0", SD bit = "1", SSLOW bit = "1")

・fs = 44.1 kHz (Normal Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.1 dB	-	0	-	19.2	kHz
	−3.0 dB	-	-	21.8	-	kHz
Pass band	(Note 30)	PB	0	-	19.2	kHz
Stop band	(Note 30)	SB	25.1	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.04	dB
Stop band Attenuation	(Note 23)	SA	62.0	-	-	dB
Group Delay	(Note 26)	GD	-	10.5	-	1/fs
Group Delay Distortion		ΔGD	-	±0.12	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–20.0 kHz		-	-0.2	-	+0.1	dB

・fs = 96 kHz (Double Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.1 dB	-	0	-	41.8	kHz
	−3.0 dB	-	-	47.3	-	kHz
Pass band	(Note 30)	PB	0	-	41.8	kHz
Stop band	(Note 30)	SB	54.6	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.04	dB
Stop band Attenuation	(Note 23)	SA	62	-	-	dB
Group Delay	(Note 26)	GD	-	10.5	-	1/fs
Group Delay Distortion		ΔGD	-	±0.12	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–40.0 kHz		-	-0.6	-	+0.1	dB

・fs = 192 kHz (Quad Speed Mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.1 dB	-	0	-	83.6	kHz
	−3.0 dB	-	-	94.0	-	kHz
Pass band	(Note 30)	PB	0	-	83.6	kHz
Stop band	(Note 30)	SB	109.3	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.04	dB
Stop band Attenuation	(Note 23)	SA	62	-	-	dB
Group Delay	(Note 26)	GD	-	10.5	-	1/fs
Group Delay Distortion		ΔGD	-	±0.12	-	1/fs
Digital Filter + SCF	(Note 23)					
Frequency Response: 0–80.0 kHz		-	-2.0	-	+0.1	dB

Note 30. The passband and stopband frequencies scale with fs. For example, PB = 0.435 × fs(@±0.1 dB), SB = 0.569 × fs.

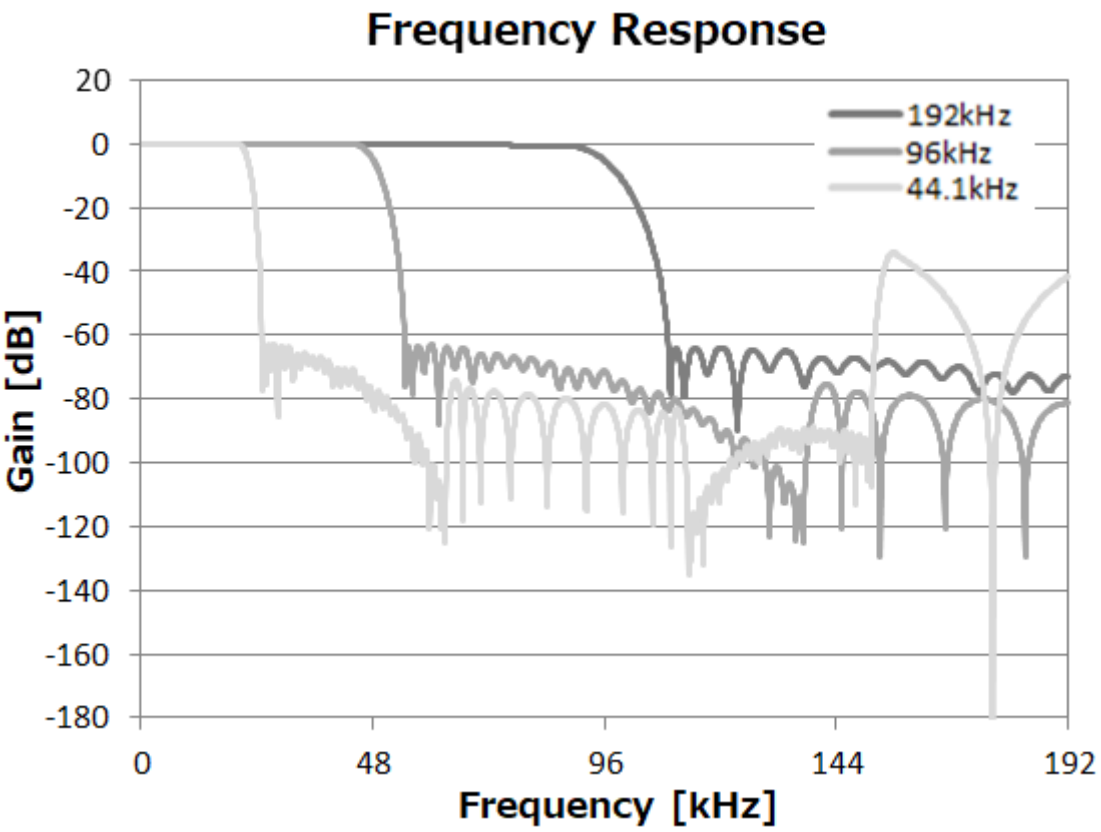


Figure 10. Low dispersion Short-delay Filter Frequency Response

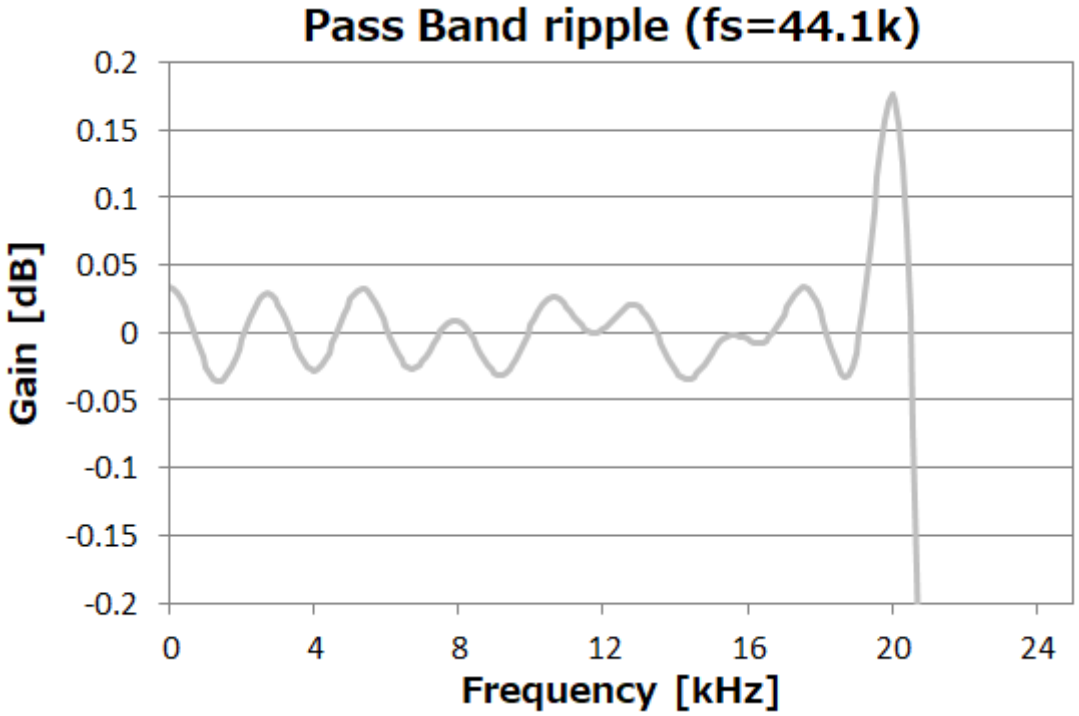


Figure 11. Low dispersion Short-delay Filter Passband Ripple

8.3. DAC Digital-Filter Characteristics (DSD mode)

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; fs = 44.1 kHz)

8.3.1. DSDD bit = "0", DSDF bit = "0"

Parameter			Min.	Typ.	Max.	Unit
DSD Filter Frequency Response (Note 32)	DSDSEL[1:0] bits					
	"00"	20 kHz 50 kHz 100 kHz		-0.8 -5.5 -19.9		dB
	"01"	40 kHz 100 kHz 200 kHz		-0.8 -5.5 -19.9		dB
	"10"	80 kHz 200 kHz 400 kHz		-0.8 -5.5 -19.9		dB
	"11"	160 kHz 400 kHz 800 kHz		-0.8 -5.5 -19.9		dB

8.3.2. DSDD bit = "0", DSDF bit = "1"

Parameter			Min.	Typ.	Max.	Unit
DSD Filter Frequency Response (Note 32)	DSDSEL[1:0] bits					
	"00"	20 kHz 50 kHz 100 kHz		-0.2 -6.3 -23.7		dB
	"01"	40 kHz 100 kHz 200 kHz		-0.2 -6.3 -23.7		dB
	"10"	80 kHz 200 kHz 400 kHz		-0.2 -6.3 -23.7		dB
	"11"	160 kHz 400 kHz 800 kHz		-0.8 -6.3 -23.7		dB

8.3.3. DSDD bit = "1"

Parameter			Min.	Typ.	Max.	Unit
DSD Filter Frequency Response (Note 32)	DSDSEL[1:0] bits					
	"00"	20 kHz 100 kHz 200 kHz		-0.2 -6.3 -23.7		dB
	"01"	40 kHz 200 kHz 400 kHz		-0.2 -6.3 -23.7		dB
	"10"	80 kHz 400 kHz 800 kHz		-0.2 -6.3 -23.7		dB
	"11"	160 kHz 500 kHz 1 MHz		-0.05 -0.5 -1.8		dB

Note 31. Do not input the signal which exceeds 25%-75% duty range.
Note 32. Frequency response refers to the output level of 1 kHz.

8.4. DC Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD = 1.7–3.0 V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
TVDD = 3.0–3.6 V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (TDMO0/1, DZF pins: Iout = -100 μA)	VOH	TVDD−0.3	-	-	V
Low-Level Output Voltage (except SDA pin: Iout = 100 μA)	VOL	-	-	0.3	V
(SDA pin, 2.0 V ≤ TVDD ≤ 3.6 V: Iout = 3 mA)	VOL	-	-	0.4	V
(SDA pin, 1.7 V ≤ TVDD ≤ 2.0 V: Iout = 3 mA)	VOL	-	-	20%TVDD	V
Input Leakage Current (Note 33)	Iin	-	-	±10	μA

Note 33. #6 SDTI3 pin, #7 SDTI4 pin, and #11 SMUTE pin have internal pull-down resistors. The resistance is 100 kΩ (Typ). Therefore, the SDTI3 pin, SDTI4 pin and SMUTE pin are not included in this value.

8.5. Switching Characteristics

(Ta = -40–105 °C; AVDD = 3.0–5.5 V, TVDD = 1.7–3.6 V; C_L = 20 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing (Note 34)					
Frequency	fCLK	1.8432		49.6640	MHz
Duty Cycle	dCLK	40		60	%
Pulse Width	tCLKH	9.05			ns
	tCLKL	9.05			ns
LRCK Clock Timing					
Normal Mode (TDM[1:0] = "00")					
Normal Speed Mode	fsn	7.2		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
Oct Speed Mode	fso	216		388	kHz
Hex Speed Mode	fsh	388		776	kHz
Duty Cycle	Duty	45		55	%
TDM128 Mode (TDM[1:0] = "01")					
Normal Speed Mode	fsn	7.2		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
High time	tLRH	1/128fs			ns
Low time	tLRL	1/128fs			ns
TDM256 Mode (TDM[1:0] = "10")					
Normal Speed Mode High time	fsn	7.2		54	kHz
Double Speed Mode	fsd	54		108	kHz
High time	tLRH	1/256fs			ns
Low time	tLRL	1/256fs			ns
TDM512 Mode (TDM[1:0] = "11")					
Normal Speed Mode	fsn	7.2		54	kHz
High time	tLRH	1/512fs			ns
Low time	tLRL	1/512fs			ns

Note 34. The MCLK frequency must be changed while the AK4468 is in power down state or reset state by setting the PDN pin = "L"or RSTN bit = "0".

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCM Audio Interface Timing					
Normal Mode (TDM[1:0] = "00")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			ns
Double Speed Mode	tBCK	1/128fsd			ns
Quad Speed Mode	tBCK	1/64fsq			ns
Oct Speed Mode	tBCK	1/64fso			ns
Hex Speed Mode	tBCK	1/64fsh			ns
BICK Pulse Width Low	tBCKL	9			ns
BICK Pulse Width High	tBCKH	9			ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	5			ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	5			ns
SDTI1/2/3/4 Hold Time	tSDH	5			ns
SDTI1/2/3/4 Setup Time	tSDS	5			ns
TDM128 Mode (TDM[1:0] = "01")					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			ns
Double Speed Mode	tBCK	1/128fsd			ns
Quad Speed Mode	tBCK	1/128fsq			ns
BICK Pulse Width Low	tBCKL	14			ns
BICK Pulse Width High	tBCKH	14			ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	14			ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	14			ns
SDTI1/2 Hold Time	tSDH	5			ns
SDTI1/2 Setup Time	tSDS	5			ns
TDM256 Mode (TDM[1:0] = "10")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			ns
Double Speed Mode	tBCK	1/256fsd			ns
BICK Pulse Width Low	tBCKL	14			ns
BICK Pulse Width High	tBCKH	14			ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	14			ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	14			ns
TDMO1/2 Setup time BICK "↑"	tBSS	5			ns
TDMO1/2 Hold time BICK "↑"	tBSH	5			ns
SDTI1/2 Hold Time	tSDH	5			ns
SDTI1/2 Setup Time	tSDS	5			ns
TDM512 Mode (TDM[1:0] = "11")					
BICK Period					
Normal Speed Mode	tBCK	1/512fsn			ns
BICK Pulse Width Low	tBCKL	14			ns
BICK Pulse Width High	tBCKH	14			ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	14			ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	14			ns
TDMO1 Setup time BICK "↑"	tBSS	5			ns
TDMO1 Hold time BICK "↑"	tBSH	5			ns
SDTI1 Hold Time	tSDH	5			ns
SDTI1 Setup Time	tSDS	5			ns

Note 35. It is defined so that LRCK edges do not occur at the same timing of a rising edge of BICK.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DSD Audio Interface Timing					
Sampling Frequency	fs	30		48	kHz
(DSD64 Mode, DSDSEL[1:0] bits= "00")					
DCLK Period	tDCK		1/64fs		ns
DCLK Pulse Width Low	tDCKL	144			ns
DCLK Pulse Width High	tDCKH	144			ns
DCLK Edge to DSDL/R (Note 36)	tDDD	−20		20	ns
(DSD128 Mode, DSDSEL[1:0] bits = "01")					
DCLK Period	tDCK		1/128fs		ns
DCLK Pulse Width Low	tDCKL	72			ns
DCLK Pulse Width High	tDCKH	72			ns
DCLK Edge to DSDL/R (Note 36)	tDDD	−10		10	ns
(DSD256 Mode, DSDSEL[1:0] bits = "10")					
DCLK Period	tDCK		1/256fs		ns
DCLK Pulse Width Low	tDCKL	36			ns
DCLK Pulse Width High	tDCKH	36			ns
DCLK Edge to DSDL/R (Note 36)	tDDD	−5		5	ns
(DSD512 Mode, DSDSEL[1:0] bits = "11")					
DCLK Period	tDCK		1/512fs		ns
DCLK Pulse Width Low	tDCKL	18			ns
DCLK Pulse Width High	tDCKH	18			ns
DSDL/R Setup Time	tDDS	5			ns
DSDL/R Hold Time	tDDH	5			ns

Note 36. DSD data transmitting device must meet this time. "tDDD" is defined from DCLK "↓" until DSDL/R edge when DCKB bit = "0" (default), "tDDD" is defined from DCLK "↑" until DSDL/R edge when DCKB bit = "1". If the audio data format is in phase modulation mode, "tDDD" is defined from DCLK edge "↓" or "↑" until DSDL/R edge regardless of DCKB bit setting.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial Control Mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C-Bus Control Mode):					
SCL Clock Frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling (Note 37)	tHD:DAT	0			µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF
Power down & Reset Timing					
PDN Accept Pulse Width	tAPD	150			ns
PDN Reject Pulse Width	tRPD			30	ns

Note 37. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 38. I^2C-Bus is a trademark of NXP B.V.

8.6. Timing Diagram

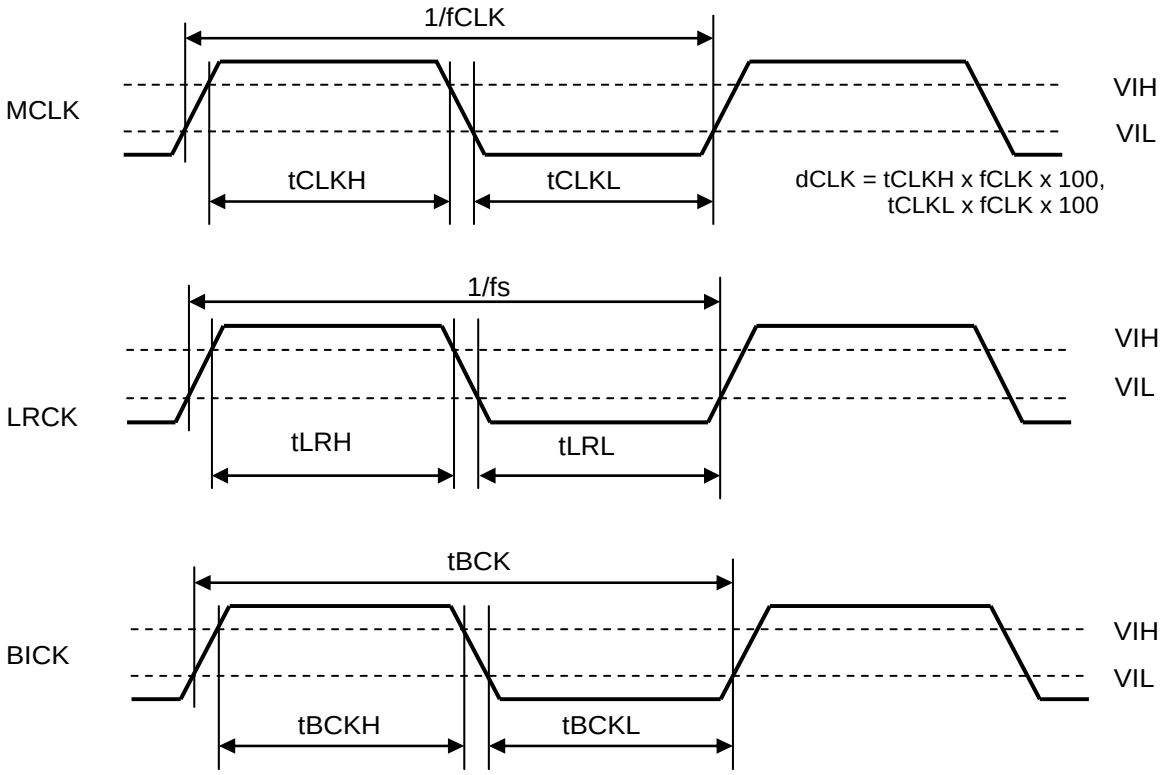


Figure 12. Clock Timing

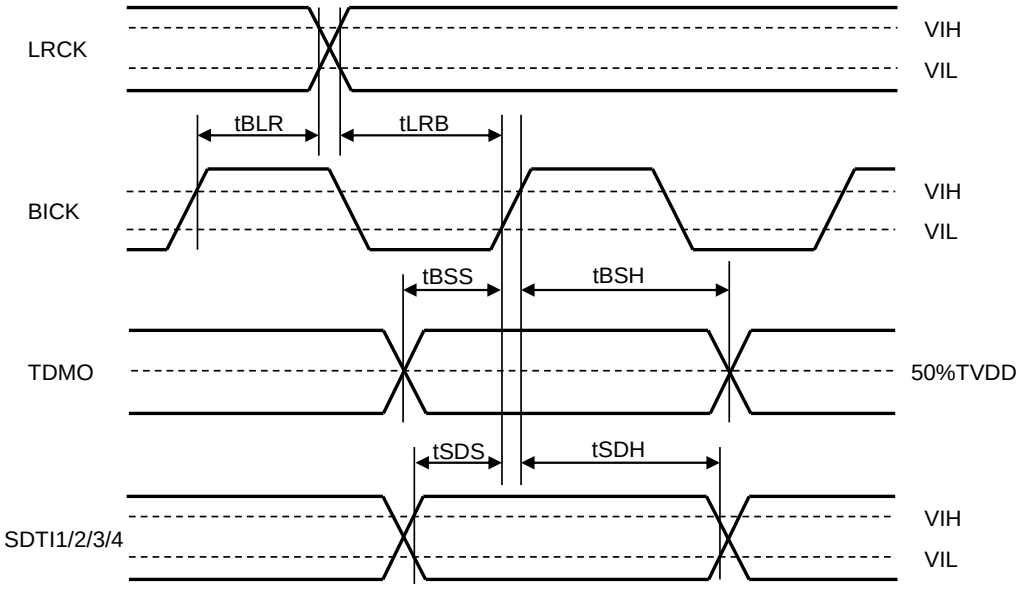
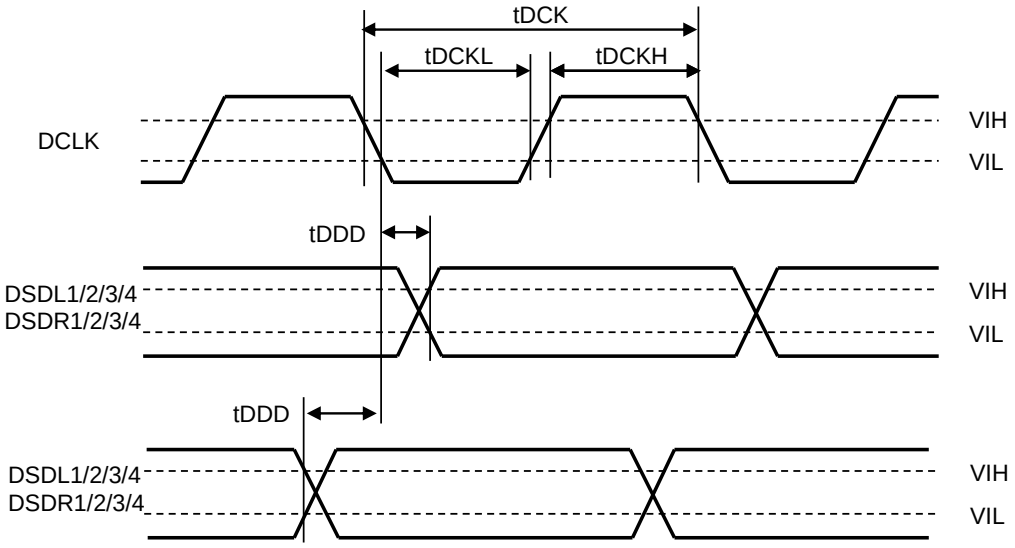
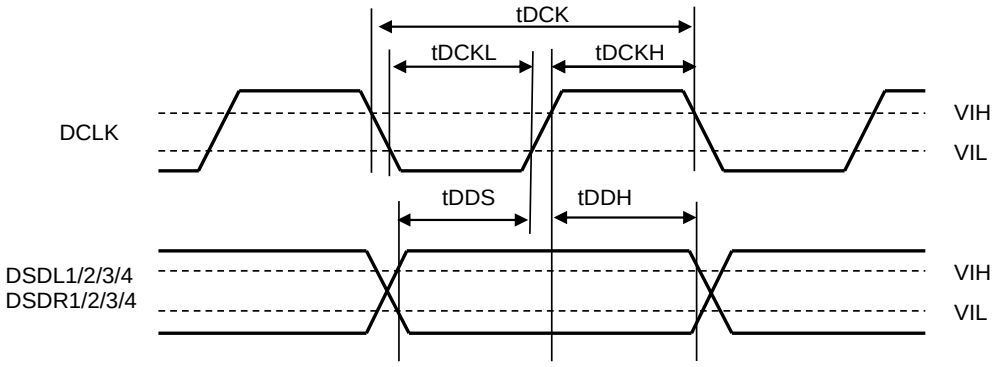


Figure 13. Audio Interface Timing (PCM mode)



DSD Audio Interface Timing (DSD64/128/256 Mode)



DSD Audio Interface Timing (DSD512 Mode)

Figure 14. Audio Interface Timing (DSD Mode, DCKB bit = “0”)

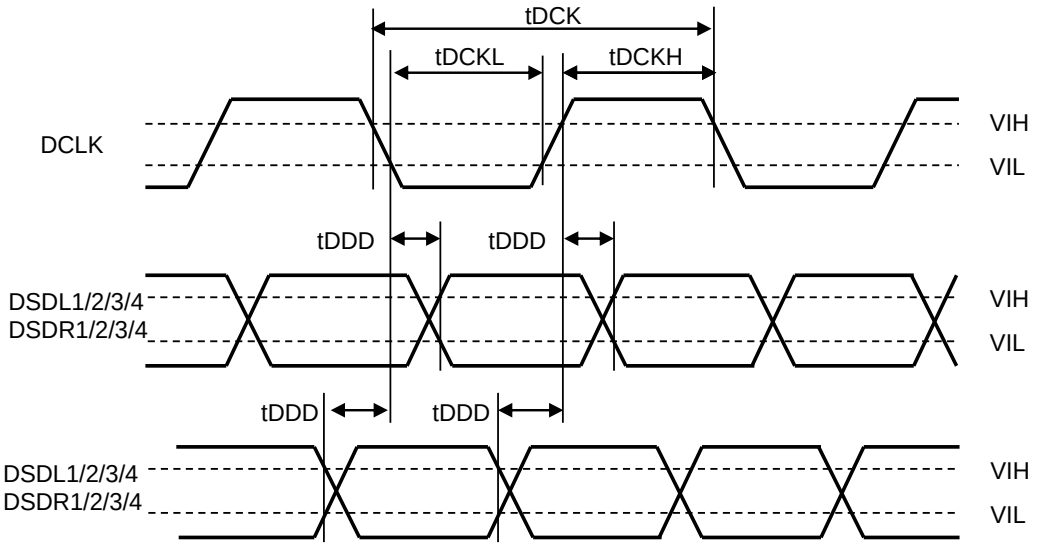


Figure 15. Audio Interface Timing (DSD Mode, Phase Modulation Format, DCKB bit = “0”)

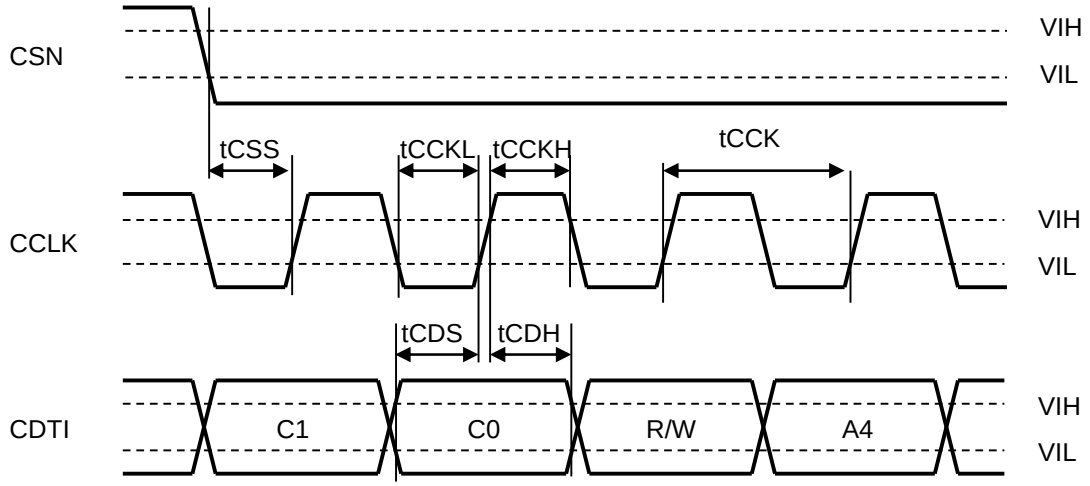


Figure 16. WRITE Command Input Timing (3-wire Serial Control Mode)

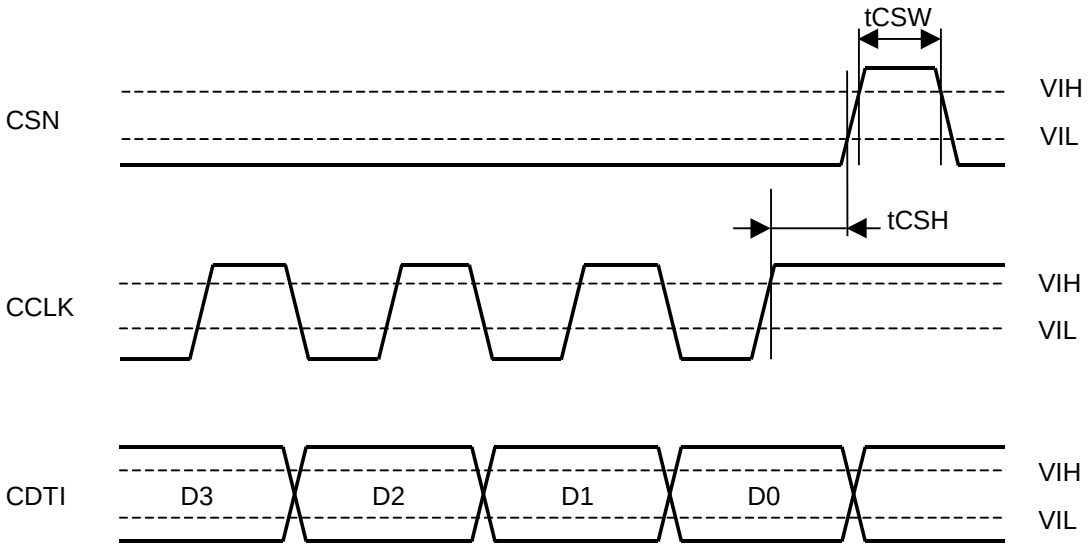


Figure 17. WRITE Data Input Timing (3-wire Serial Control Mode)

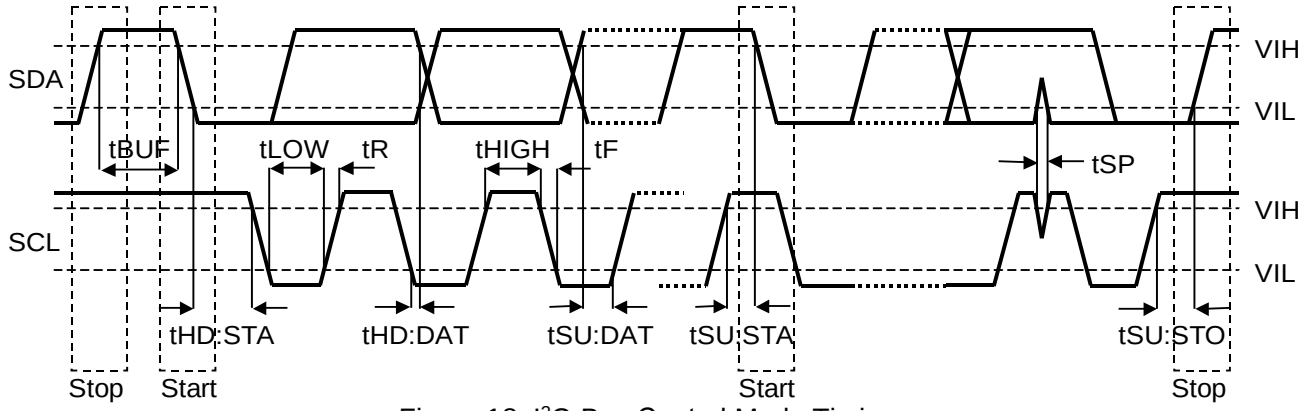


Figure 18. I²C-Bus Control Mode Timing

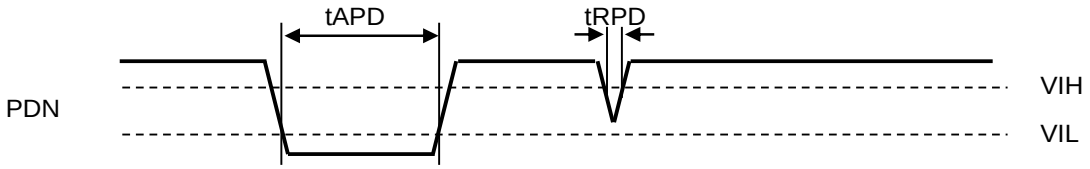


Figure 19. Power Down & Reset Timing

9. Functional Descriptions

9.1. Control Mode

Each function of the AK4468 is controlled by pins (Pin Control Mode) or registers (Register Control Mode) (Table 1). Select the control mode by setting the PS pin and the I2C pin. The AK4468 must be powered down by the PDN pin when changing the PS and the I2C pin settings. There is a possibility of malfunction if the device is not powered down when changing the control mode since the previous setting is not reinitialized. Register settings are invalid in Pin Control Mode, and pin settings are invalid in Register Control Mode.
Table 2 shows available functions of each control mode.

Table 1. Pin/Register Control Mode Select (x: do not care)

I2C pin	PS pin	Control Mode
L	x	3-wire Serial Register Control Mode
H	L	I^2C-Bus Register Control Mode
H	H	Pin Control Mode

Table 2. Function List @Pin/Register Control Mode
(Y: Available, N/A: Not available)

Function	Pin Control Mode	Register Control Mode
DSD mode Select	N/A	Y
System Clock Setting Select	Y	Y
Audio Format Select	Y	Y
TDM Mode	Y	Y
Digital Filter Select	N/A	Y
De-emphasis Filter Select	N/A	Y
Digital Attenuator	N/A	Y
Zero Detection	N/A	Y
Mono Mode	N/A	Y
Output signal select (Mono, Channel select)	N/A	Y
Output signal polarity select (Invert)	N/A	Y
DSD Full-Scale Detection	N/A	Y
Soft Mute	Y	Y
Register Reset	N/A	Y
Clock Synchronization Function disable (default: enable)	N/A	Y
Automatic Mode Switching (PCM/DSD)	N/A	Y
Register Control	N/A	Y

9.2. D/A Conversion Mode

The AK4468 is able to convert either PCM or DSD data to an analog signal. In PCM mode, clocks and PCM data can be input from the BICK, LRCK and SDTI1/2/3/4 pins. In DSD mode, clocks and DSD data can be input from the DCLK, DSDL1/2/3/4 and DSDR1/2/3/4 pins. The AK4468 only supports PCM mode in Pin Control Mode.

Table 3 shows available functions in PCM/DSD mode.

Table 3 Function List of PCM/DSD mode @Register Control Mode
(Y: Available, N/A: Not available)

Function	Default State	Addr	Bit	PCM	DSD
PCM/DSD Mode Select	PCM mode	02H	DP	Y	Y
System Clock Setting @DSD Mode	512fs	02H	DCKS	N/A	Y
Digital Filter Select @DSD Mode	39kHz filter	09H	DSDF	N/A	Y
Digital Filter Select @PCM Mode	Short-delay sharp roll-off filter	01,02,05H	SD SLOW SSLOW	Y	N/A
System Clock Setting Mode Select	Manual Setting Mode	00H	ACKS	Y	N/A
De-emphasis Response	OFF	01,0A,0EH	DEM1/2/3/4[1:0]	Y	N/A
Path Select @ DSD Mode	Normal Path	06H	DSDD	N/A	Y
Audio Data Interface Format @ PCM Mode	32bit MSB	00H	DIF[2:0]	Y	N/A
TDM Interface Format	Normal Mode	0AH	TDM[1:0]	Y	N/A
Daisy Chain	Disable	0BH	DCHAIN	Y	N/A
Attenuation Level	0dB	03-04H 0F-14H	ATTL1/2/3/4[7:0] ATTR1/2/3/4[7:0]	Y	Y
Data Zero Detection Enable	Disable	07-08H	L1/2/3/4 R1/2/3/4	Y	Y
Mono/Stereo Mode Select	Stereo	02,0DH	MONO1/2/3/4	Y	Y
Data Invert Mode Select	OFF	05,0CH	INVL1/2/3/4 INVR1/2/3/4	Y	Y
The data selection of L channel and R channel	R channel	02,05,0DH	SELLR 1/2/3/4	Y	Y
DSD Mute Function @ Full-scale Detected	Disable	06H	DDM	N/A	Y
Soft Mute Enable	Normal Operation	01H	SMUTE	Y	Y
RSTN	Reset	00H	RSTN	Y	Y
Clock Synchronization Function	Enable	07H	SYNCE	Y	N/A
Automatic Mode Switching (PCM/DSD mode)	Disable	15H	ADPE	Y	Y

Switching to DSD mode, manual and automatic settings are selectable. The AK4468 is in Manual Setting Mode when ADPE bit = "0" and it is in Automatic Setting Mode when ADPE bit = "1". (Table 4)

In manual setting mode (ADPE bit = "0"), D/A conversion mode switching between PCM and DSD is executed by DP bit. Switching PCM/DSD mode must be executed during reset state by setting RSTN bit = "0". RSTN bit should not be changed for 4/fs after switching these modes. It takes 2/fs-3/fs for data mode switching.

In Auto Setting Mode (ADPE bit = "1"), DP bit setting is ignored. The AK4468 monitors input signals of the number 3 pin to select PCM or DSD mode. Refer to "9.10 PCM/DSD Automatic Mode Switching Function" for details of PCM/DSD mode automatic switching

Table 4. PCM/DSD Mode Control @Register Control Mode (x: do not care)

ADPE bit	DP bit	D/A Conv. Mode	Pin Assign								
			#2 pin	#3 pin	#4 pin	#5 pin	#6 pin	#7 pin	#8 pin	#9 pin	#10 pin
0	0	PCM	BICK	LRCK	SDTI1	SDTI2	SDTI3	SDTI4	Not Used	Not Used	Not Used
	1	DSD	DCLK	DSDL 1	DSDR 1	DSDL 2	DSDR 2	DSDL 3	DSDR 3	DSDL 4	DSDR 4
1	x	Auto (PCM or DSD)	BICK /DCLK	LRCK /DSDL 1	SDTI1 /DSD R1	SDTI2 /DSDL 2	SDTI3 /DSD R2	SDTI4 /DSDL 3	Not Used /DSD R3	Not Used /DSDL 4	Not Used /DSD R4

9.2.1. D/A Conversion Mode Switching Timing (Manual Setting)

Figure 20 and Figure 21 show switching timing of PCM and DSD modes in manual mode (ADPE bit = "0"). To prevent noise caused by excessive input, DSD signal should be input 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to DSD mode from PCM mode. DSD signal should be stopped 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to PCM from DSD mode.

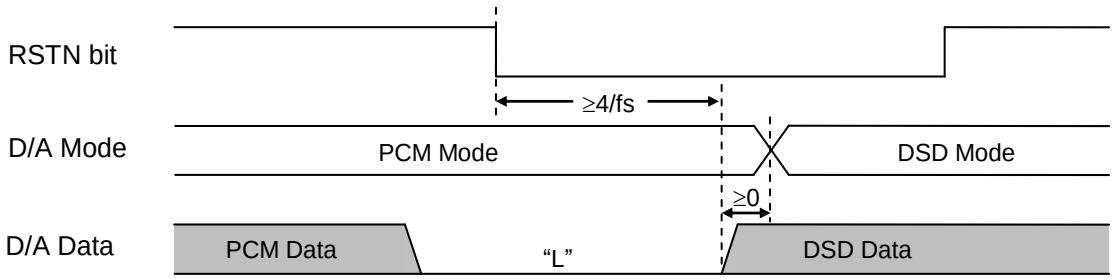


Figure 20. D/A Mode Switching Timing (from PCM to DSD)

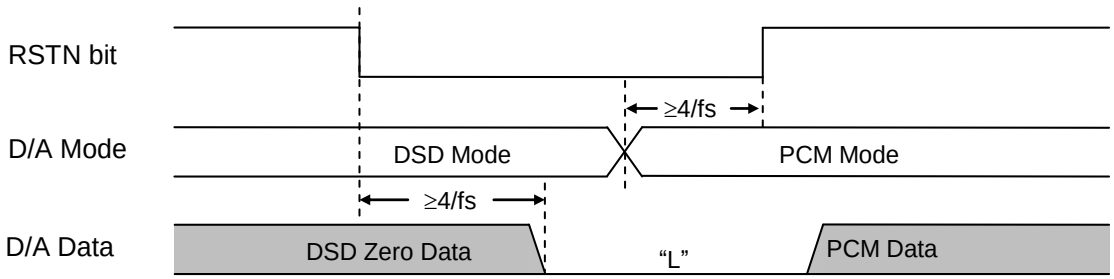


Figure 21. D/A Mode Switching Timing (from DSD to PCM)

9.3. System Clock

9.3.1. PCM mode

The external clocks, which are required to operate the AK4468, are MCLK, BICK and LRCK. MCLK, BICK and LRCK should be synchronized but the phase of MCLK is not critical. MCLK is used to operate the interpolator, the ΔΣ modulator and SCF.
There are Manual Setting Mode and Auto Setting Mode for sampling speed setting and MCLK, LRCK frequency settings (Table 5). In Pin Control Mode, it will be in Auto Setting Mode forcibly.

Table 5. System Clock Setting Mode @Register Control Mode

ACKS bit	Mode	
0	Manual setting Mode	(default)
1	Auto setting Mode	

All circuits except control registers and internal LDO (if LDOE pin = “H”) of the AK4468 are automatically placed in power down state when MCLK is stopped for more than 1 μs during normal operation, and the analog output becomes Hi-z state (Table 35).
When MCLK is input again, the AK4468 exits this power down state and starts operation again. In this case, register settings are not initialized. The AK4468 is in power down state and the analog output is floating state until MCLK, BICK and LRCK are supplied.

MCLK frequency must be changed while the AK4468 is in reset state by setting the PDN pin = “L” or RSTN bit = “0”.

9.3.1.1. Manual Setting Mode (ACKS bit = “0”)

In manual setting mode, sampling speed is set by DFS[2:0] bits (Table 6). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 7, Table 8). The AK4468 is in manual setting mode when power down is released (PDN pin = “L” → “H”). DFS[2:0] bits must be changed while the AK4468 is in reset state by setting the RSTN bit = “0”. This function is only supported in register control mode.

Table 6. Sampling Speed (Manual Setting Mode)

DFS[2:0] bits	Sampling Speed	Sampling Rate (fs)	
000	Normal Speed Mode	7.2 kHz–54 kHz	(default)
001	Double Speed Mode	54 kHz–108 kHz	
010	Quad Speed Mode	108 kHz–216 kHz	
011	Quad Speed Mode	108 kHz–216 kHz	
100	Oct Speed Mode	216 kHz–388 kHz	
101	Hex Speed Mode	388 kHz–776 kHz	
110	Oct Speed Mode	216 kHz–388 kHz	
111	Hex Speed Mode	388 kHz–776 kHz	

Table 7. System Clock Example (Manual Setting Mode) (N/A: Not available)

LRCK	MCLK(MHz)						Sampling Speed
fs	16fs	32fs	48fs	64fs	96fs	128fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	24.5760	
352.8 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	Oct
384 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
705.6 kHz	11.2896	22.5792	33.8688	45.1584	N/A	N/A	Hex
768 kHz	12.2880	24.5760	36.8640	49.1520	N/A	N/A	

Table 8. System Clock Example (Manual Setting Mode) (N/A: Not available)

LRCK	MCLK(MHz)							Sampling Speed
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal
44.1 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	
48.0 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0 kHz	N/A	24.5760	36.8640	49.1520	N/A	N/A	N/A	
176.4 kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	36.8640	49.1520	N/A	N/A	N/A	N/A	N/A	
352.8 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
705.6 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

9.3.1.2. Auto Setting Mode (ACKS bit = “1”)

In Auto Setting Mode, the MCLK and LRCK frequency ratio is detected to automatically set the Sampling Speed Mode (Table 9). Therefore, sampling speed setting by DFS[2:0] bits is not necessary. The frequencies of MCLK corresponding to each Sampling Speed Mode should be input externally (Table 10, Table 11). In Pin Control Mode, the AK4468 will be in Auto Setting Mode forcibly.

Table 9. Sampling Speed (Auto Setting Mode)

MCLK		Sampling Speed
1024fs/1152fs		Normal (fs ≤ 32 kHz)
512fs/256fs	768fs/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad
64fs	96fs	Oct
32fs	48fs	Hex

Table 10. System Clock Example (Auto Setting Mode) (N/A: Not available)

LRCK	MCLK(MHz)						Sampling
fs	32fs	48fs	64fs	96fs	128fs	192fs	Speed
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	Quad
192.0 kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	
352.8 kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	Oct
384.0 kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	
705.6 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Hex
768.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	

Table 11. System Clock Example (Auto Setting Mode) (N/A: Not available)

LRCK	MCLK(MHz)						Sampling
fs	256fs	384fs	512fs	768fs	1024fs	1152fs	Speed
32.0 kHz	8.1920(*)	12.2880(*)	16.3840	24.5760	32.7680	36.8640	Normal
44.1 kHz	11.2896(*)	16.9344(*)	22.5792	33.8688	N/A	N/A	
48.0 kHz	12.2880(*)	18.4320(*)	24.5760	36.8640	N/A	N/A	
88.2 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Double
96.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
352.8 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
384.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
705.6 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex
768.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	

When MCLK = 256fs/384fs, Auto Setting Mode supports sampling rates of 8 kHz-96 kHz (Table 11). However, the Dynamic Range and S/N performances will degrade approximately 3 dB if the sampling rate is under 54 kHz (values with (*) in Table 11) due to the internal oversampling ratio being reduced by one half comparing with when MCLK = 512fs/768fs (Table 12).

Table 12. Relationship between Dynamic Range, S/N and MCLK Frequency (fs = 44.1 kHz)

ACKS bit	MCLK	Dynamic Range, S/N (A-weighted)
0	256fs/384fs/512fs/768fs	117 dB
1	256fs/384fs	114 dB
1	512fs/768fs	117 dB

9.3.2. DSD Mode (Register Control Mode Only)

The external clocks that are required in DSD mode are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit (Table 13). The AK4468 is automatically placed in standby state when MCLK is stopped during normal operation, and the analog output becomes Hi-z state. When the reset is released (RSTN bit = "0"→"1"), the AK4468 is in standby state until MCLK and DCLK are input.

Table 13. System Clock (DSD mode, fs = 32 kHz, 44.1 kHz, 48 kHz)

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs/128fs/256fs/512fs	(default)
1	768fs	64fs/128fs/256fs/512fs	

The AK4468 supports DSD data stream rates of DSD64, DSD128, DSD256 and DSD512 modes. The data sampling speed is selected by DSDSEL[1:0] bits (Table 14).

Table 14. DSD Data Stream Select

DSDSEL[1:0] bits	DSD mode	DCLK Frequency	DSD data stream			
			fs = 32 kHz	fs = 44.1 kHz	fs = 48 kHz	
00	DSD64	64fs	2.048 MHz	2.8224 MHz	3.072 MHz	(default)
01	DSD128	128fs	4.096 MHz	5.6448 MHz	6.144 MHz	
10	DSD256	256fs	8.192 MHz	11.2896 MHz	12.288 MHz	
11	DSD512	512fs	16.284 MHz	22.5792 MHz	24.576 MHz	

The AK4468 has a Volume bypass function that bypasses DATT/Soft Mute (internal attenuation circuit) and ΔΣ modulator outputs for playing back a DSD signal. Two modes are selectable by DSDD bit (Table 15). When setting DSDD bit = "1", the output volume control and zero detection functions are not available.

Table 15. DSD Playback Path Select

DSDD bit	Mode	
0	Normal Path	(default)
1	Volume Bypass	

9.4. Audio Interface Format

9.4.1. PCM mode

Four data modes, such as Normal Mode, TDM128, TDM256, and TDM512 Modes, are available. Mode settings are available by the pins (TDM0/1 pins and DIF pin) and registers (TDM[1:0] bits and DIF[2:0] bits). However, it should not be changed during operation. The AK4468 must be reset by setting RSTN bit when the format setting is changed during operation.

9.4.1.1. Input Data Format (Pin Control Mode)

Normal Mode (TDM1 pin = “L”, TDM0 pin = “L”)
8ch Data is shifted in via the SDTI1/2/3/4 pins using BICK and LRCK inputs. Two data formats are supported and selected by the DIF pin as shown in Table 16. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM128 Mode (TDM1 pin = “L”, TDM0 pin = “H”)
8ch Data is shifted in via the SDTI1/2 pins using BICK and LRCK inputs. Input data to the SDTI3/4 pins will be ignored. BICK is fixed to 128fs. Two data formats are supported and selected by the DIF pin as shown in Table 16. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM256 Mode (TDM1 pin = “H”, TDM0 pin = “L”)
(a) Daisy Chain Mode is disabled (DCHAIN pin = “L”)
8ch Data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Input data to the SDTI2/3/4 pins will be ignored. BICK is fixed to 256fs. Two data formats are supported and selected by the DIF pin as shown in Table 16. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.
(b) Daisy Chain Mode is enabled (DCHAIN pin = “H”)
16ch Data is shifted in via the SDTI1/2 pins using BICK and LRCK inputs. Input data to the SDTI3/4 pins will be ignored. BICK is fixed to 256fs. Two data formats are supported and selected by the DIF pin as shown in Table 16. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM512 Mode (TDM1 pin = “H”, TDM0 pin = “H”)
16ch Data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Input data to the SDTI2/3/4 pins will be ignored. BICK is fixed to 512fs. Two data formats are supported and selected by the DIF pin as shown in Table 16. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

Table 16. Audio Interface Format (@Pin Control Mode)

Mode		TDM1 pin	TDM0 pin	DIF pin	SDTI Format	LRCK	BICK	Figure	
Normal (Note 39)	6	L	L	L	32-bit MSB justified	H/L	≥64fs	Figure 27	(default)
	7	L	L	H	32-bit I²S compatible	L/H	≥64fs	Figure 28	
TDM128	12	L	H	L	32-bit MSB justified	H/L	128fs	Figure 29	
	13	L	H	H	32-bit I²S compatible	L/H	128fs	Figure 30	
TDM256	18	H	L	L	32-bit MSB justified	H/L	256fs	Figure 32	
	19	H	L	H	32-bit I²S compatible	L/H	256fs	Figure 33	
TDM512	24	H	H	L	32-bit MSB justified	H/L	512fs	Figure 35	
	25	H	H	H	32-bit I²S compatible	L/H	512fs	Figure 36	

Note 39. The number of cycles of BICK must be the same as the bit length of setting format or more.

9.4.1.2. Input Data Format (Register Control Mode)

Normal Mode (TDM[1:0] bits = “00”)
8ch Data is shifted in via the SDTI1/2/3/4 pins using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF[2:0] bits as shown in Table 17. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 2 can be used for 16-bit and 20-bit and Mode 6 can be used for 16-bit, 20-bit and 24-bit MSB justified formats by zeroing the unused LSBs. Refer to 9.4.1.3 Data Slot Selection Function for options to route data to DAC outputs.

TDM128 Mode (TDM[1:0] bits = “01”)
8ch Data is shifted in via the SDTI1/2 pins using BICK and LRCK inputs. Input data to the SDTI3/4 pins will be ignored. BICK is fixed to 128fs. Six data formats are supported and selected by DIF[2:0] bits, as shown in Table 17. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Refer to 9.4.1.3 Data Slot Selection Function for options to route data to DAC outputs.

TDM256 Mode (TDM[1:0] bits = “10”)
16ch Data is shifted in via the SDTI1/2 pins using BICK and LRCK inputs. Input data to the SDTI3/4 pins will be ignored. BICK is fixed to 256fs. Six data formats are supported and selected by the DIF[2:0] bits, as shown in Table 17. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Refer to 9.4.1.3 Data Slot Selection Function or 9.4.1.4 Daisy Chain for options to route data to DAC outputs.

TDM512 Mode (TDM[1:0] bits = “11”)
16ch Data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Input data to the SDTI2/3/4 pins will be ignored. BICK is fixed to 512fs. Six data formats are supported and selected by the DIF[2:0] bits, as shown in Table 17. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Refer to 9.4.1.3 Data Slot Selection Function or 9.4.1.4 Daisy Chain for options to route data to DAC outputs.

Table 17. Audio Interface Format (@Register Control Mode) (N/A: Not available)

Mode		TDM[1:0] bits	DIF[2:0] bits	SDTI Format	LRCK	BICK	Figure	
Normal (Note 40)	0	00	000	16-bit LSB justified	H/L	≥32fs	Figure 22	
	1		001	20-bit LSB justified	H/L	≥40fs	Figure 23	
	2		010	24-bit MSB justified	H/L	≥48fs	Figure 24	
	3		011	16-bit I²S compatible	L/H	32fs	Figure 25	
				24-bit I²S compatible	L/H	≥48fs		
	4		100	24-bit LSB justified	H/L	≥48fs	Figure 23	
	5		101	32-bit LSB justified	H/L	≥64fs	Figure 26	
	6		110	32-bit MSB justified	H/L	≥64fs	Figure 27	(default)
	7		111	32-bit I²S compatible	L/H	≥64fs	Figure 28	
TDM128		01	000	N/A	N/A	N/A	N/A	
			001	N/A	N/A	N/A	N/A	
	8		010	24-bit MSB justified	H/L	128fs	Figure 29	
	9		011	24-bit I²S compatible	L/H	128fs	Figure 30	
	10		100	24-bit LSB justified	H/L	128fs	Figure 31	
	11		101	32-bit LSB justified	H/L	128fs	Figure 29	
	12		110	32-bit MSB justified	H/L	128fs		
	13		111	32-bit I²S compatible	L/H	128fs	Figure 30	
TDM256		10	000	N/A	N/A	N/A	N/A	
			001	N/A	N/A	N/A	N/A	
	14		010	24-bit MSB justified	H/L	256fs	Figure 32	
	15		011	24-bit I²S compatible	L/H	256fs	Figure 33	
	16		100	24-bit LSB justified	H/L	256fs	Figure 34	
	17		101	32-bit LSB justified	H/L	256fs	Figure 32	
	18		110	32-bit MSB justified	H/L	256fs		
	19		111	32-bit I²S compatible	L/H	256fs	Figure 33	
TDM512		11	000	N/A	N/A	N/A	N/A	
			001	N/A	N/A	N/A	N/A	
	20		010	24-bit MSB justified	H/L	512fs	Figure 35	
	21		011	24-bit I²S compatible	L/H	512fs	Figure 36	
	22		100	24-bit LSB justified	H/L	512fs	Figure 37	
	23		101	32-bit LSB justified	H/L	512fs	Figure 35	
	24		110	32-bit MSB justified	H/L	512fs		
	25		111	32-bit I²S compatible	L/H	512fs	Figure 36	

Note 40. The number of cycles of BICK must be the same as the bit length of setting format or more.

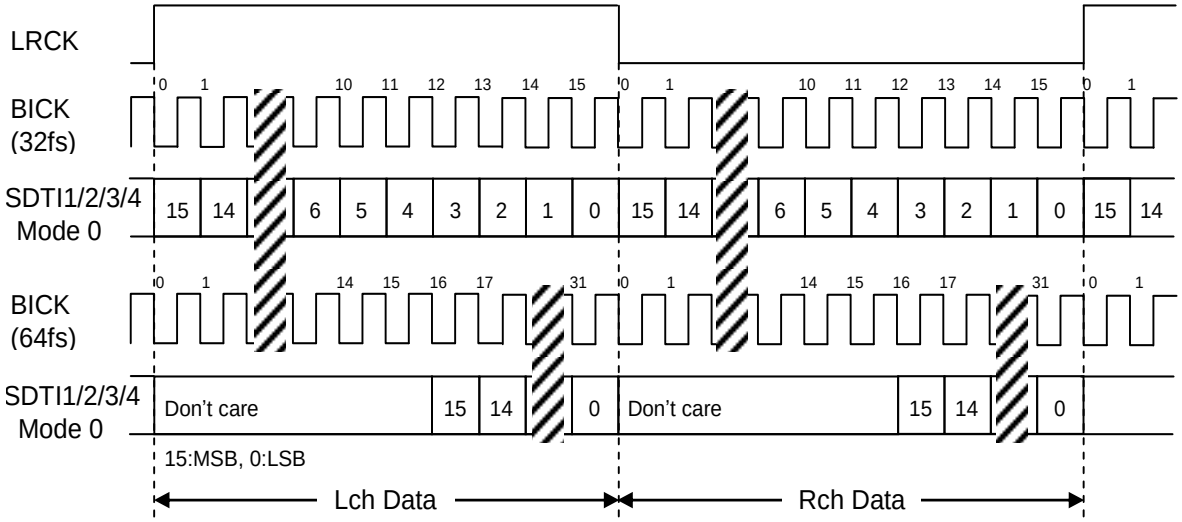


Figure 22. Mode 0 Timing

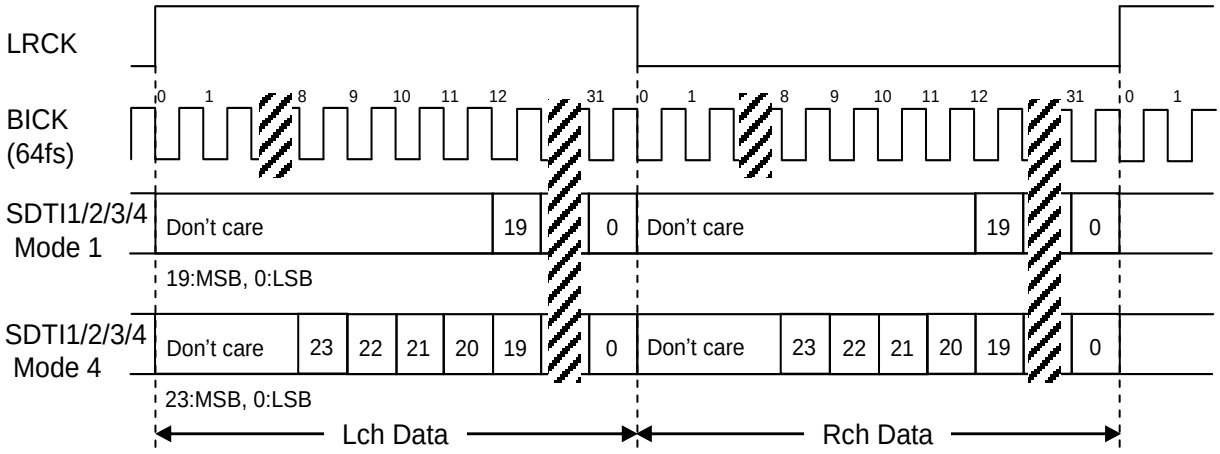


Figure 23. Mode 1, 4 Timing

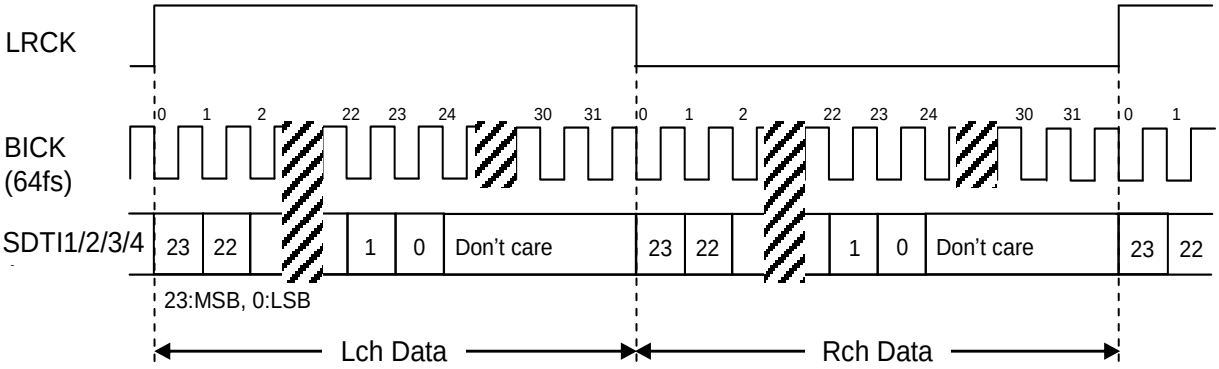


Figure 24. Mode 2 Timing

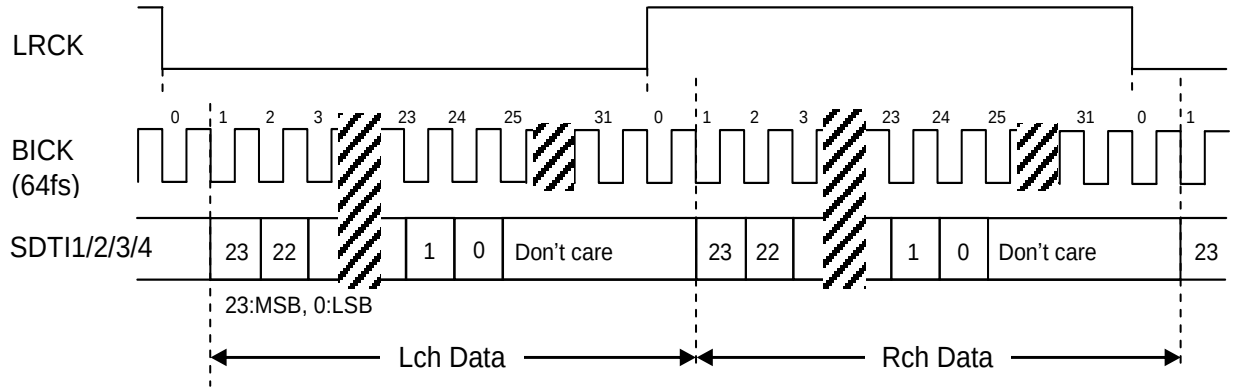


Figure 25. Mode 3 Timing

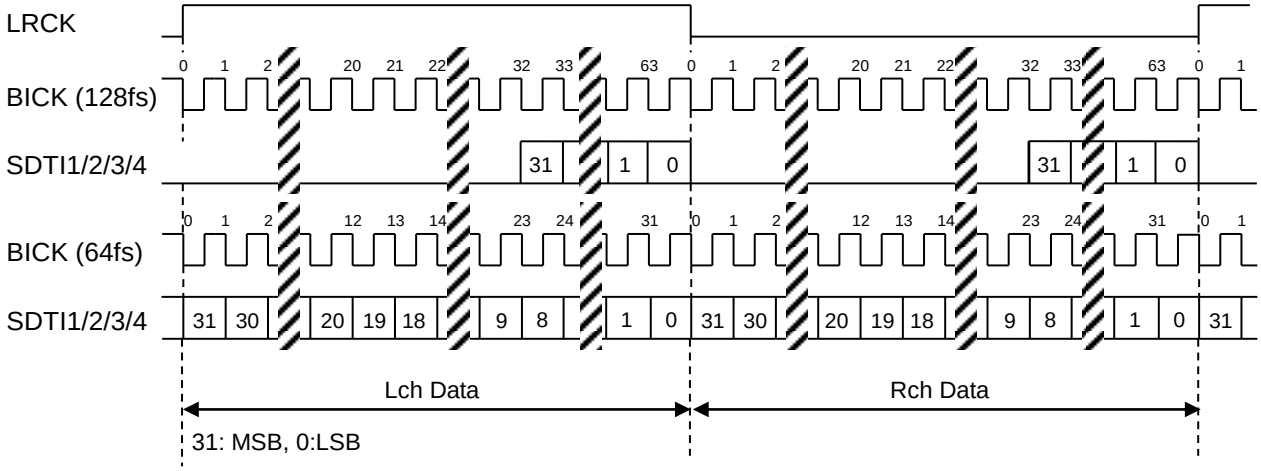


Figure 26. Mode 5 Timing

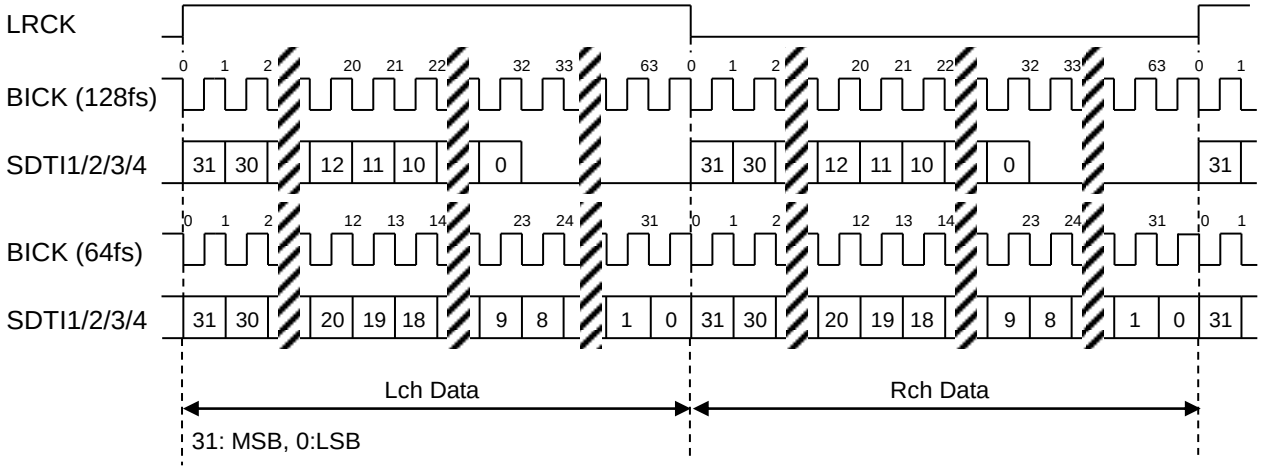


Figure 27. Mode 6 Timing

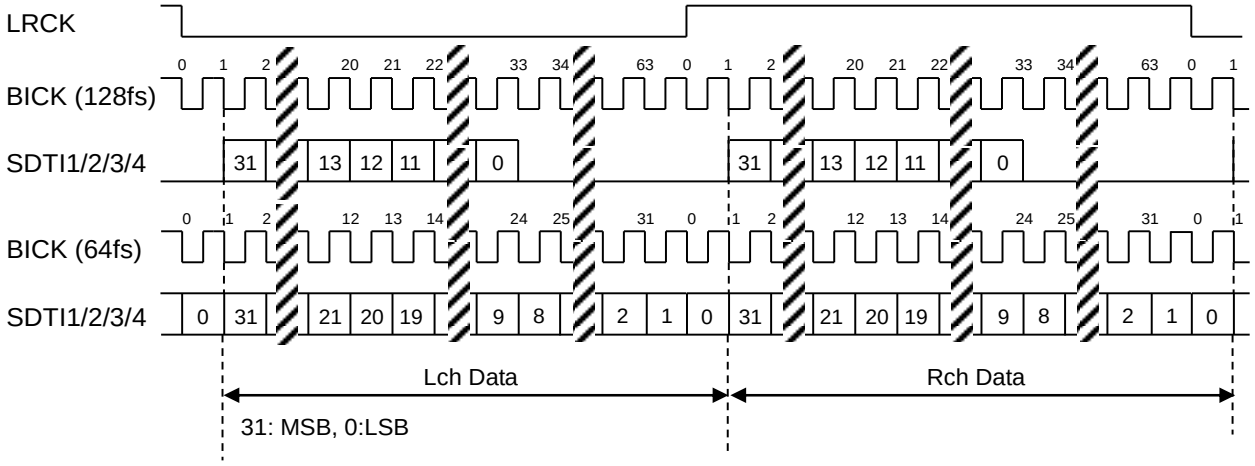


Figure 28. Mode 7 Timing

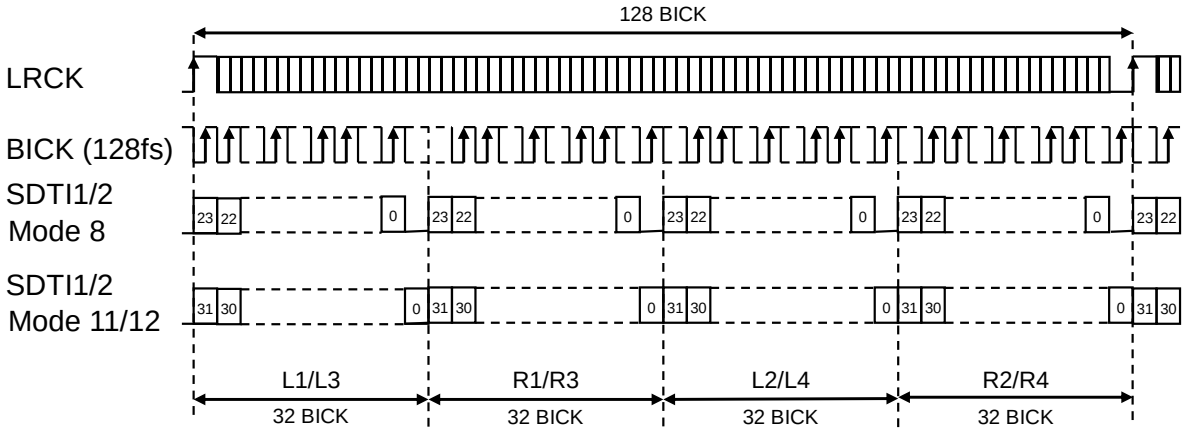


Figure 29. Mode 8/11/12 Timing

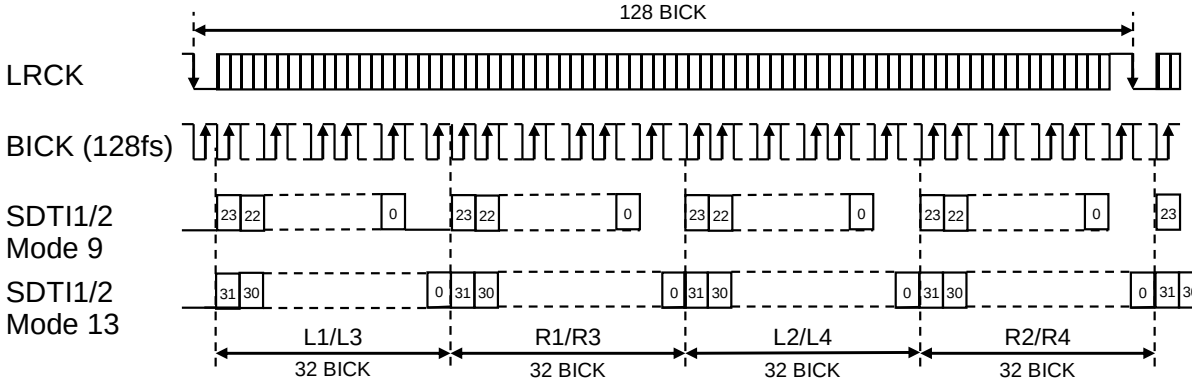


Figure 30. Mode 9/13 Timing

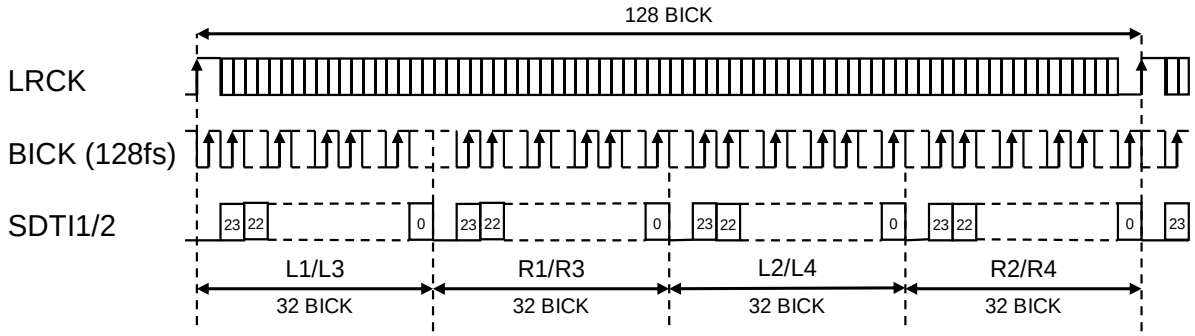


Figure 31. Mode 10 Timing

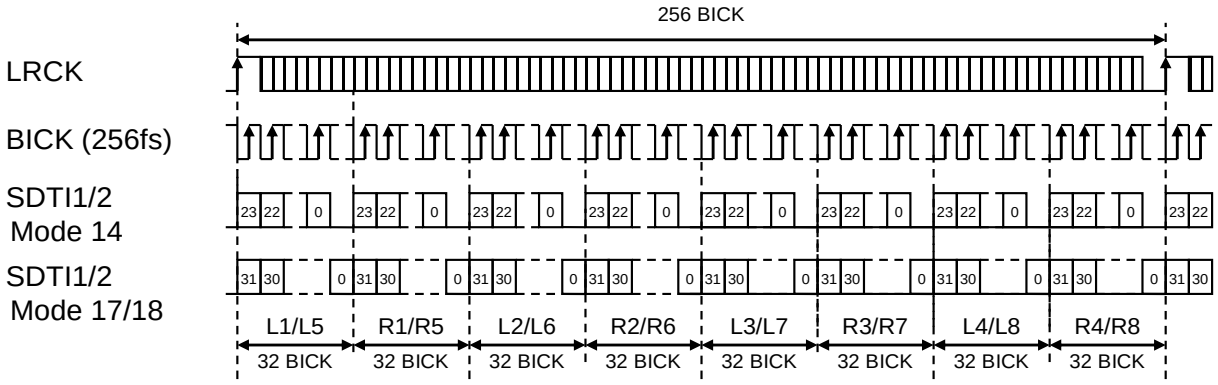


Figure 32. Mode 14/17/18 Timing

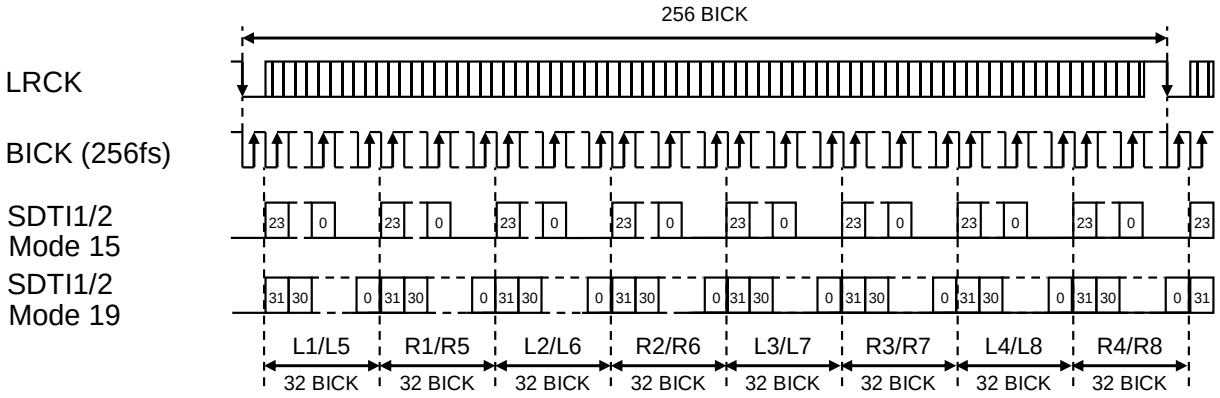


Figure 33. Mode 15/19 Timing

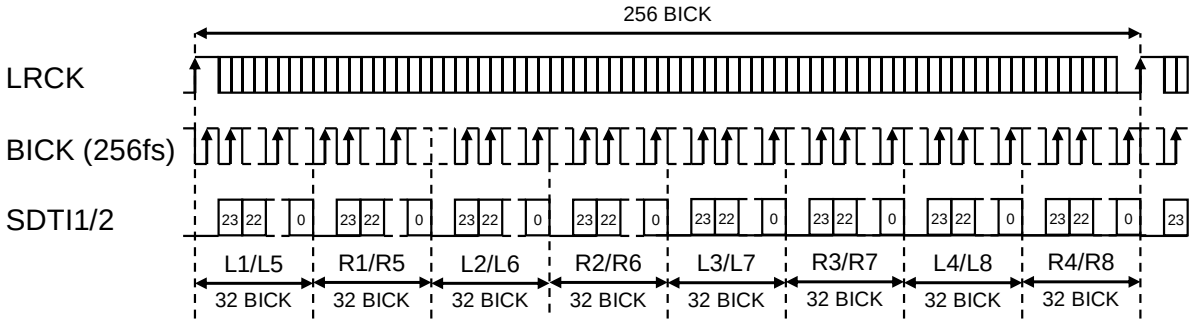


Figure 34. Mode 16 Timing

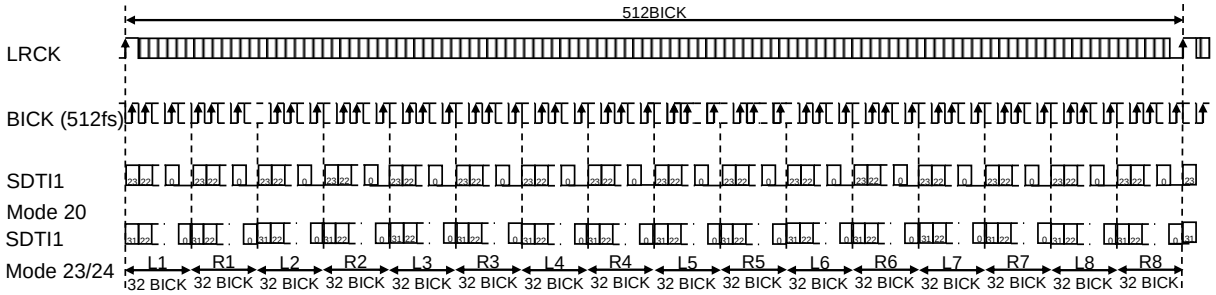


Figure 35. Mode 20/23/24 Timing

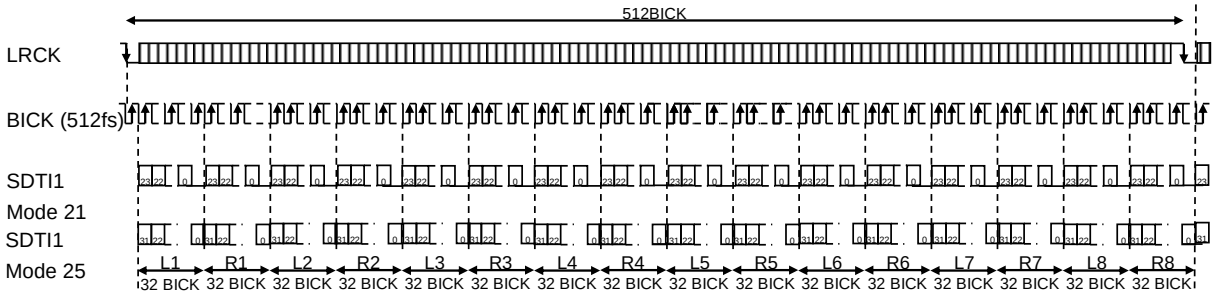


Figure 36. Mode 21/25 Timing

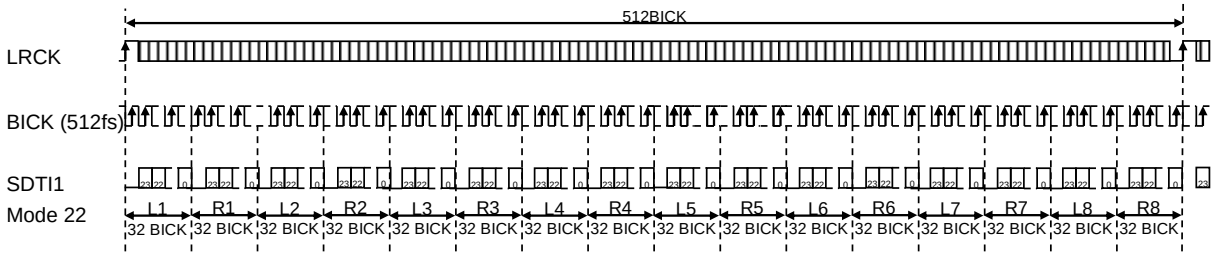


Figure 37. Mode 22 Timing

9.4.1.3. Data Slot Selection Function

Data slot of 1 cycle LRCK for each audio data format is defined as Figure 38, Figure 39, Figure 40 and Figure 41. DAC output data can be selected by SDS[2:0] bits (Register Control Mode only), as shown in Table 18.

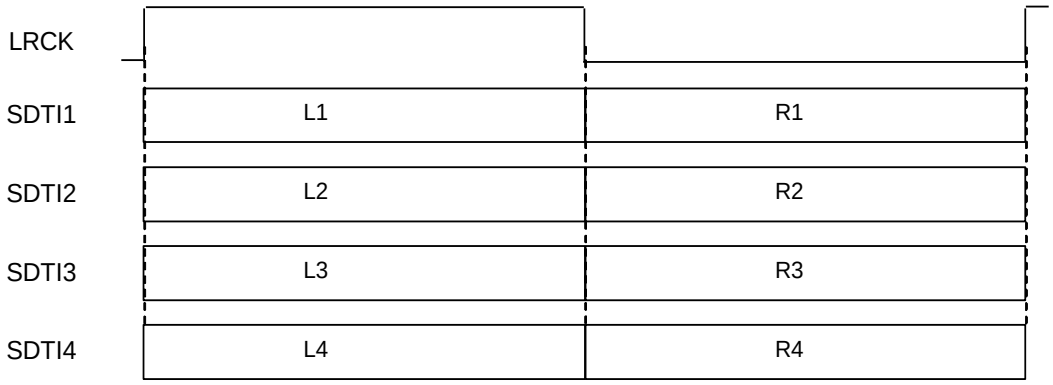


Figure 38. Data Slot in Normal Mode

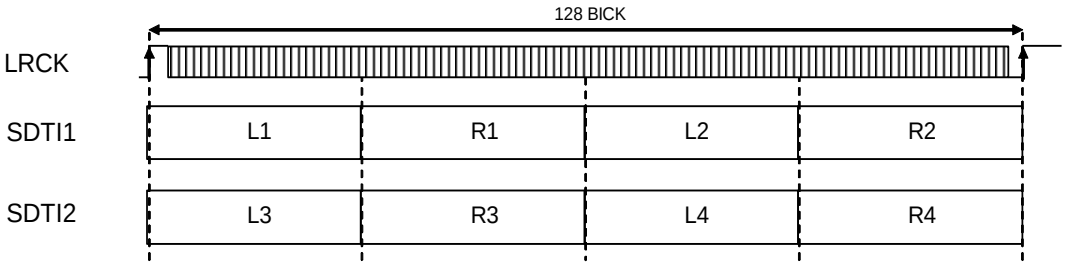


Figure 39. Data Slot in TDM128 Mode

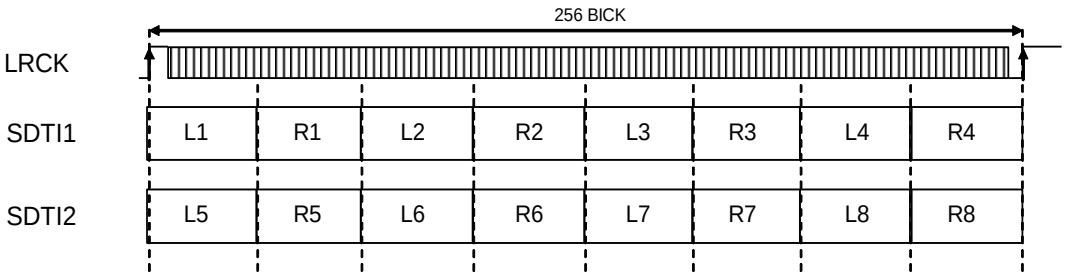


Figure 40. Data Slot in TDM256 Mode

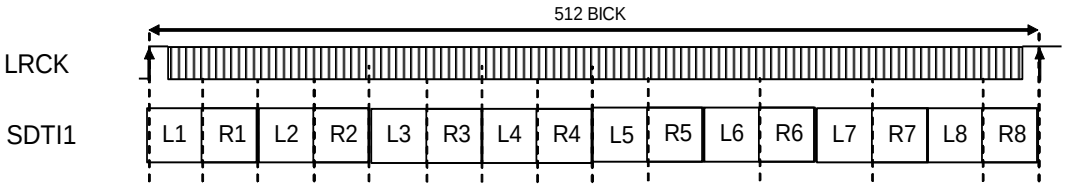


Figure 41. Data Slot in TDM512 Mode

Table 18. Data Select (x: Do not care)

	TDM[1:0] bits	SDS[2:0] bits	DAC1		DAC2		DAC3		DAC4		
			Lch	Rch	Lch	Rch	Lch	Rch	Lch	Rch	
Normal	00	x00	L1	R1	L2	R2	L3	R3	L4	R4	(default)
		x01	L2	R2	L3	R3	L4	R4	L1	R1	
		x10	L3	R3	L4	R4	L1	R1	L2	R2	
		x11	L4	R4	L1	R1	L2	R2	L3	R3	
TDM128	01	x00	L1	R1	L2	R2	L3	R3	L4	R4	
		x01	L2	R2	L3	R3	L4	R4	L1	R1	
		x10	L3	R3	L4	R4	L1	R1	L2	R2	
		x11	L4	R4	L1	R1	L2	R2	L3	R3	
TDM256	10	000	L1	R1	L2	R2	L3	R3	L4	R4	
		001	L2	R2	L3	R3	L4	R4	L5	R5	
		010	L3	R3	L4	R4	L5	R5	L6	R6	
		011	L4	R4	L5	R5	L6	R6	L7	R7	
		100	L5	R5	L6	R6	L7	R7	L8	R8	
		101	L6	R6	L7	R7	L8	R8	L1	R1	
		110	L7	R7	L8	R8	L1	R1	L2	R2	
		111	L8	R8	L1	R1	L2	R2	L3	R3	
TDM512	11	000	L1	R1	L2	R2	L3	R3	L4	R4	
		001	L2	R2	L3	R3	L4	R4	L5	R5	
		010	L3	R3	L4	R4	L5	R5	L6	R6	
		011	L4	R4	L5	R5	L6	R6	L7	R7	
		100	L5	R5	L6	R6	L7	R7	L8	R8	
		101	L6	R6	L7	R7	L8	R8	L1	R1	
		110	L7	R7	L8	R8	L1	R1	L2	R2	
		111	L8	R8	L1	R1	L2	R2	L3	R3	

9.4.1.4. Daisy Chain

Multiple AK4468s can be connected by Daisy Chain. Daisy Chain mode can be arranged from DCHAIN bit or DCHAIN pin (Table 19). Daisy Chain supports TDM512/256 mode. SDS[2:0] bits setting will be ignored in Daisy Chain mode.

Table 19 Daisy Chain Control

DCHAIN bit DCHAIN pin	Daisy Chain Mode	#6 pin Function	#7 pin Function	
0	Disable	Input (SDTI3)	Input (SDTI4)	(default)
1	Enable	Output (TDMO1)	Output (TDMO2)	

9.4.1.4.1. TDM512 Mode

Figure 42 shows an example of TDM512 mode Daisy Chain structure (TDM[1:0] bits= “11”). 16ch data is input to the second AK4468’s SDTI1 pin from a DSP. Connect the second AK4468’s TDMO1 pin to the first AK4468’s SDTI1 pin. At TDM512 mode, TDMO2 outputs "L".

Figure 43 shows a data I/O example of TDM512 mode. SDTI1 (L5/6/7/8, R5/6/78) data is the input for the DAC of the second AK4468, and the second AK4468 outputs the data from TDMO1 by shifting 8ch. The first AK4468 accepts SDTI1 (L1/2/3/4, R1/2/3/4) data as input data of DAC. DIF[2:0] bits setting of both first AK4468 and the second AK4468 must be the same.

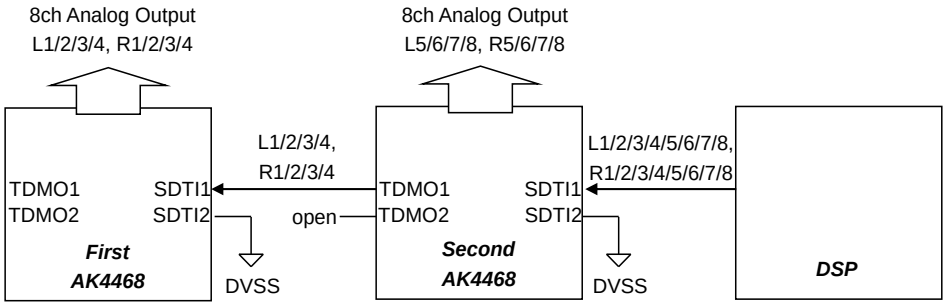


Figure 42. Daisy Chain (TDM512 Mode)

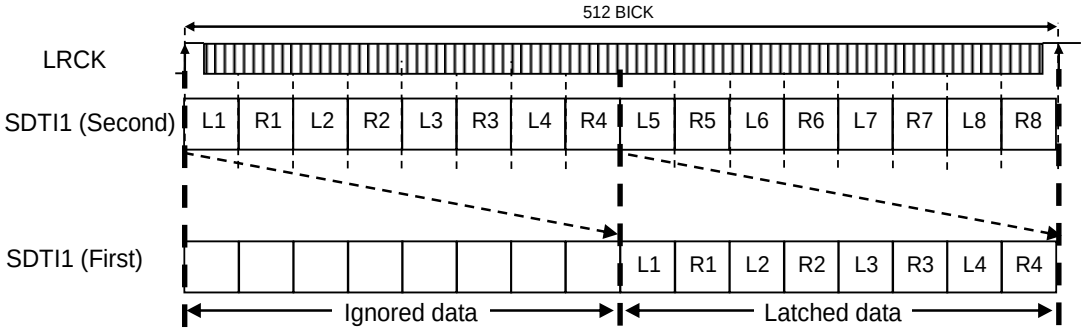


Figure 43. Daisy Chain (TDM512 Mode)

9.4.1.4.2. TDM256 Mode

Figure 44 shows an example of TDM256 mode Daisy Chain structure (TDM[1:0] bits = “10”). 16ch data is input to the second AK4468’s SDTI1/2 pin from a DSP. Connect the second AK4468’s TDMO1/2 pin to the first AK4468’s SDTI1/2 pin.

Figure 45 shows a data I/O example of TDM256 mode. SDTI1 (L3/4, R3/4) and SDTI2 (L7/8, R7/8) data is the input for the DAC of the second AK4468, and the second AK4468 outputs the data from TDMO1/2 by shifting 4ch. The first AK4468 accepts SDTI1 (L1/2, R1/2) and SDTI2 (L5/6, R5/6) data as input data of DAC. DIF[2:0] bits setting of both first AK4468 and the second AK4468 must be the same.

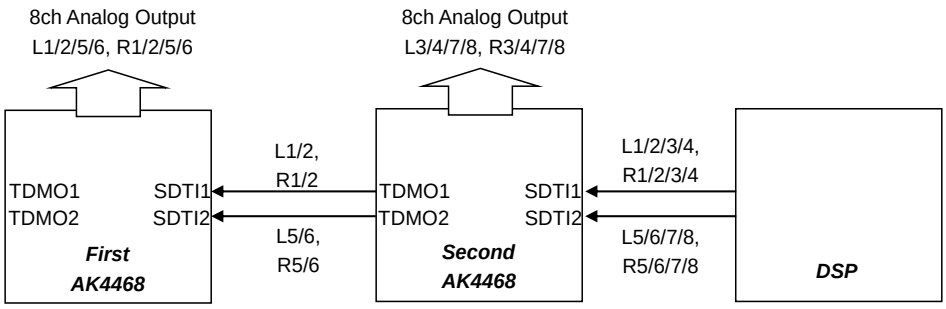


Figure 44. Daisy Chain (TDM256 Mode)

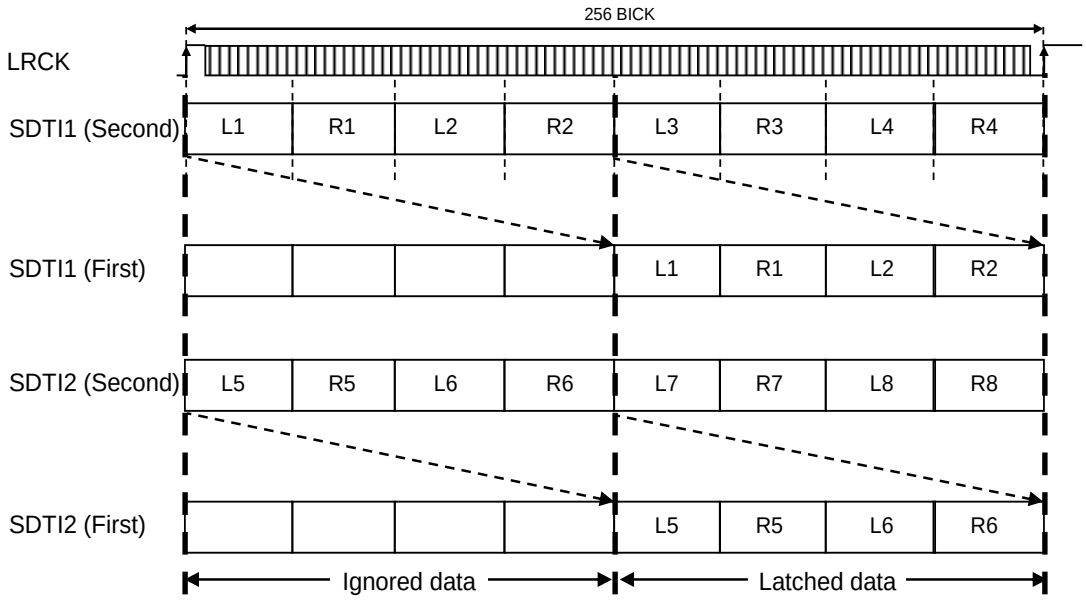


Figure 45. Daisy Chain (TDM256 Mode)

9.4.2. DSD Mode (Register Control mode only)

8ch Data is shifted in via the DSDL1/2/3/4 and DSDR1/2/3/4 pins using DCLK inputs. DSD data is supported by both Normal mode (Figure 46) and Phase Modulation mode (Figure 47). The AK4468 does not support phase modulation when DCLK is 512fs (DSDSEL[1:0] bits = “11”).
Polarity of DCLK is possible to invert by DCKB bit. Input data is clocked in on a rising edge of DCLK when DCKB bit = “0” and it is clocked in on a falling edge of DCLK when DCKB bit = “1”.
In case of DSD mode, the setting of DIF[2:0] bits is ignored.

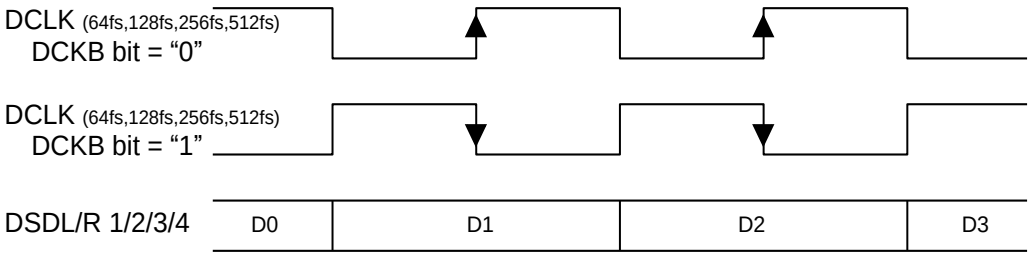


Figure 46. DSD Mode Timing

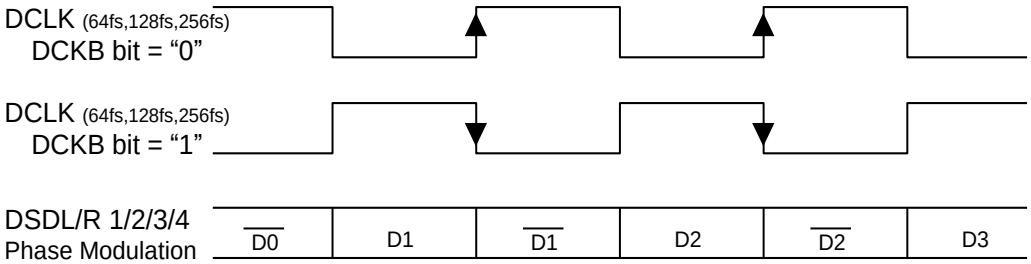


Figure 47. DSD Mode Timing (Phase Modulation Format)

9.5. Digital Filter

Six types of digital filter in PCM mode and two types of digital filter in DSD mode are available in the AK4468 for sound color selection of music playback.

9.5.1. PCM Mode

In PCM mode, the digital filter is available as shown in Table 20. The digital filter can be selected by the SD, SLOW and SSLOW bits if the AK4468 is in Register Control Mode and the sampling speed is in Normal, Double and Quad Speed Mode (Table 21).

Table 20. Digital Filter Setting Table by Control Mode (@PCM mode)

Sampling Speed	Control Mode	
	Pin	Register
Normal	Short delay sharp roll-off filter (fixed)	Selectable (Table 21)
Double		
Quad		
Oct	Super slow roll-off filter (fixed)	
Hex		

Table 21. Digital Filter Setting Table by Control Register (@PCM mode) (x: do not care)

SSLOW bit	SD bit	SLOW bit	Mode	
0	0	0	Sharp roll-off filter	
0	0	1	Slow roll-off filter	
0	1	0	Short delay sharp roll-off filter	(default)
0	1	1	Short delay slow roll-off filter	
1	0	x	Super slow roll-off filter	
1	1	x	Low dispersion short delay filter	

9.5.2. DSD Mode

When DSDD bit = “0”, two kinds of digital filters are available by setting DSDF bit (Table 22). Only one digital filter is available when DSDD bit = “1”. Filter characteristics are different when DSDSEL[1:0] bits = “11” comparing to other settings such as “00”, “01” or “01”. Table 22 shows the cutoff frequency @fs = 44.1 kHz. The cutoff frequency tracks the sampling frequency (fs).

Table 22. Digital Filter Setting Table (@DSD mode) (x: do not care)

DSDD bit	DSDF bit	Cut Off Frequency @fs = 44.1 kHz				
		DSDSEL[1:0] bits = “00” (DSD64)	DSDSEL[1:0] bits = “01” (DSD128)	DSDSEL[1:0] bits = “10” (DSD256)	DSDSEL[1:0] bits = “11” (DSD512)	
0	0	39 kHz	78 kHz	156 kHz	312 kHz	(default)
	1	76 kHz	152 kHz	304 kHz	608 kHz	
1	x	76 kHz	152 kHz	304 kHz	1230 kHz	

9.6. De-emphasis Filter (PCM Mode)

A digital de-emphasis filter is available for 32 kHz, 44.1 kHz or 48 kHz sampling rates (tc = 50/15μs) and is enabled or disabled by the DEM1/2/3/4[1:0] bits (Table 23). This function is valid only in PCM Normal Speed Mode. DEM[1:0] bits are ignored in DSD mode. DEM setting value is held even if the data mode is switched between PCM and DSD modes.

Table 23. De-emphasis Control (Register Control Mode)

DEM1/2/3/4[1:0] bits	Mode	
00	44.1 kHz	
01	OFF	(default)
10	48 kHz	
11	32 kHz	

9.7. Digital Attenuation

The AK4468 includes channel independent digital attenuation for output volumes (ATT) with 256 levels at 0.5 dB step including MUTE (Table 24). When changing output levels, it is executed in soft transition, thus no switching noise occurs during these transitions. It can attenuate the input data from 0 dB to -127 dB and MUTE when assuming the output signal level is 0dB when ATTL1/2/3/4[7:0] bits and ATTR1/2/3/4[7:0] bits = “FFH”.

Table 24. Attenuation Level of Digital Attenuator

ATTL1/2/3/4[7:0] bits ATTR1/2/3/4[7:0] bits	Attenuation Level (PCM mode)	Attenuation Level (DSD mode)	
FFH	+0 dB	+0 dB	(default)
FEH	-0.5 dB	-0.5 dB	
FDH	-1.0 dB	-1.0 dB	
:	:	:	
03H	-126.0 dB	-126.0 dB	
02H	-126.5 dB	MUTE (-∞)	
01H	-127.0 dB	MUTE (-∞)	
00H	MUTE (-∞)	MUTE (-∞)	

The transition time of when changing digital output volume is defined as (Transition time of 1 code shift) x (previous ATT level – changed ATT level). The transition time of 1 code shift is set by ATS[1:0] bits (Table 25). Register setting values will be kept even switching the PCM and DSD modes.

Table 25. Attenuation Transition Time Setting

ATS[1:0] bits	Transition Time of 1 code shift	Attenuation Transition Time from “FFH” to “00H”
00	16/fs	4080/fs
01	8/fs	2040/fs
10	2/fs	510/fs
11	1/fs	255/fs

It takes 4080/fs (92.5 ms @fs = 44.1 kHz) from “FFH” (0dB) to “00H” (MUTE) when ATS[1:0] bits = “0”. ATTL1/2/3/4[7:0] bits and ATTR1/2/3/4[7:0] bits are initialized to “FFH” (0dB) by setting the PDN pin = “L”. If the digital volume attenuation level is changed during reset period, the output volume will become a setting value after releasing the reset. It will change to a setting value immediately if the volume is changed within 10/fs after releasing reset.

9.8. Zero Detection, DSD Full-scale Detection

The AK4468 has a zero detection function and a DSD full-scale detection function. These detection flags can be output from the DZF pin. DDMOE bit (06H: D4) selects the output detection flag of the DZF pin.
The output polarity of the DZF pin can be inverted by DZFB bit (02H: D2). The DZF pin goes "H" for zero/DSD full-scale detection when DZFB bit = "0", the DZF pin goes "L" when DZFB bit = "1". Table 26 shows output signal settings of the DZF pin.

Table 26. Output Select for DZF Pin

DDMOE bit	DZFB bit	DZF pin Output	
0	0	Zero Detection Flag ("H" when detect zero)	(default)
	1	Zero Detection Flag ("L" when detect zero)	
1	0	DSD Full-scale Detection Flag ("H" when detect DSD full-scale)	
	1	DSD Full-scale Detection Flag ("L" when detect DSD full-scale)	

When DDMOE bit is set to "1" in PCM mode, the DZF pin outputs "L" if DZFB bit = "0" and outputs "H" if DZFB bit = "1".

9.8.1. Zero Detection

When the zero detection function is enabled, monitoring channels are selected by L1/2/3/4 bits and R1/2/3/4 bits (07H: D7-4, 08H: D7-4). In this case, multiple channels can be selected. As shown in Figure 48, DATT soft mute block outputs are the monitor nodes. Zero detection flag is generated when all monitor nodes of selected channels, whose corresponding (L1/2/3/4 or R1/2/3/4) bit is set to "1", are continuously "0" for a detection time shown in Table 27.

Table 27. Zero Detection Time

Sampling Speed		Detection Time
PCM	Normal/Double/Quad Speed mode	8192 / fs
	Oct/Hex Speed mode	65536 / fs
DSD	DSD64/128/256/512	4096 / fs

Zero detection flag is cleared if any of data of the selected channel is no longer "0".
Zero detection flag is generated immediately when the AK4468 is reset state (RSTN bit = "0"). Zero detection flag will be cleared in 4/fs-5/fs by releasing reset (RSTN bit = "1").
When each channel is in standby state, zero detection flag is generated after counting the detection period shown in Table 27. Zero detection flag is output from the DZF pin. DZFB bit controls the polarity of zero detection flag (Table 26).

The zero detection function is disabled if Volume Bypass is selected in DSD mode (Table 15). In this case, the DZF pin outputs "H" if DZFB bit = "0" and outputs "L" if DZFB bit = "1".

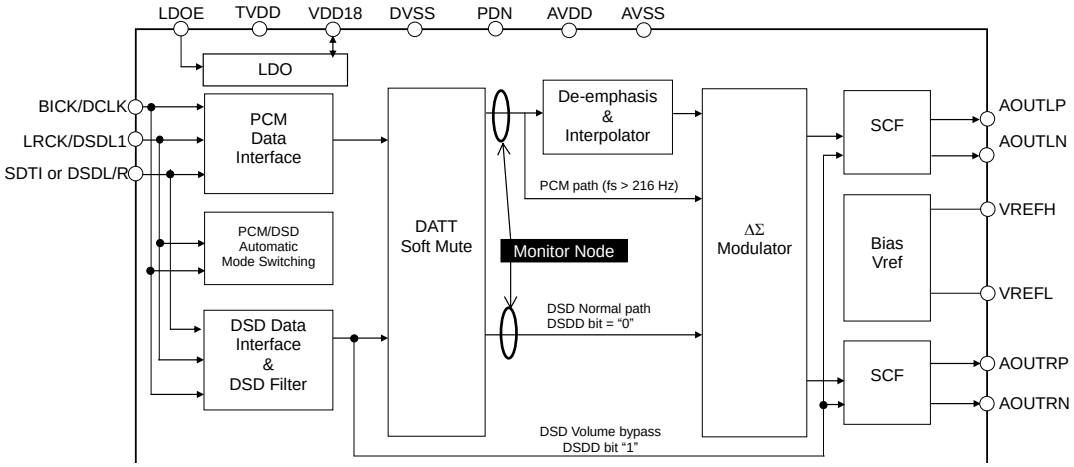


Figure 48. Zero Detection Monitor Node

9.8.2. DSD Full-Scale Detection (DSD mode)

The AK4468 has independent full-scale detection function for each channel in DSD mode. Mute function of analog output signal becomes enabled after detecting full-scale signal by setting DDM bit = "1". (DDM bit setting should be made while PW1 bit = PW2 bit = PW3 bit = PW4 bit = "0" or RSTN bit = "0")

Figure 49 shows a block diagram of DSD signal playback. Input data of each channel pin (DSDL1/2/3/4 or DSDR1/2/3/4) is received via the DSD_IF block and full-scale detection is executed at the DSD full-scale detection block. Full-scale detection is valid only the AK4468 is in power-on state (PWx bit = "1").

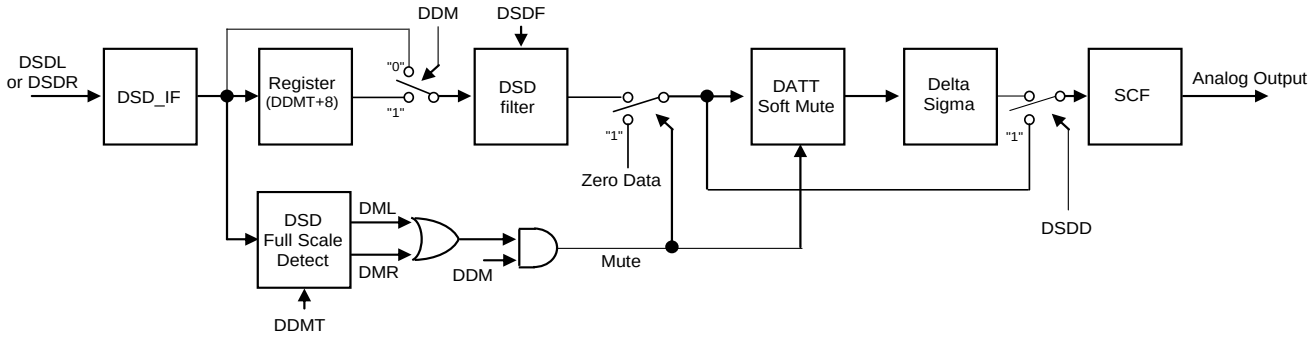


Figure 49. DSD Block Diagram

If any input data of 8ch is continuously "H" or "L" for the time set by DDMT bit, the AK4468 is in full-scale detection state (Table 28) and corresponding DML1/2/3/4 or DMR1/2/3/4 bit becomes "1" independently. These bits indicate "1" only while full-scale data is input. DML1/2/3/4 and DMR1/2/3/4 bits are "0" if the input data is not full-scale or the AK4468 is in PCM mode. DML1/2/3/4 and DMR1/2/3/4 bits can be readout by register reading.

The AK4468 mutes the analog output when full-scale data is input to any of L1/2/3/4 or R1/2/3/4 channel if DDM bit = "1". The output data of DSD_IF block is delayed by Register block for "Setting Time of DDMT bit + 8 DCLK cycles" to avoid clicking noise until the analog output is muted completely when DDM bit = "1". Therefore, the analog output delay becomes larger according to this delay time. (DDM bit setting should be made while PW1 bit = PW2 bit = PW3 bit = PW4 bit = "0" or RSTN bit = "0")

Full-scale detection state is released when the input data of the full-scale input channel is toggled. The operation after full-scale detection is released is according to DSDD bit setting that selects DSD playback path (Table 29).

When DSDD bit = “0” (Normal Path), the transition time until the output data returns to normal after releasing full-scale detection state is according to the setting of ATS[1:0] bits (Table 25).
If DSDD bit = “1” (Volume Bypass), the output data returns to normal immediately when the full-scale detection state is released.

The full-scale detection function is assuming full-scale input that occurs when switching the data mode between PCM and DSD modes. Therefore, click noise will not occur when the input signal becomes full-scale from zero data and vice versa but there is a possibility that click noise occurs when the input signal becomes full-scale from the state there is an input signal and vice versa.

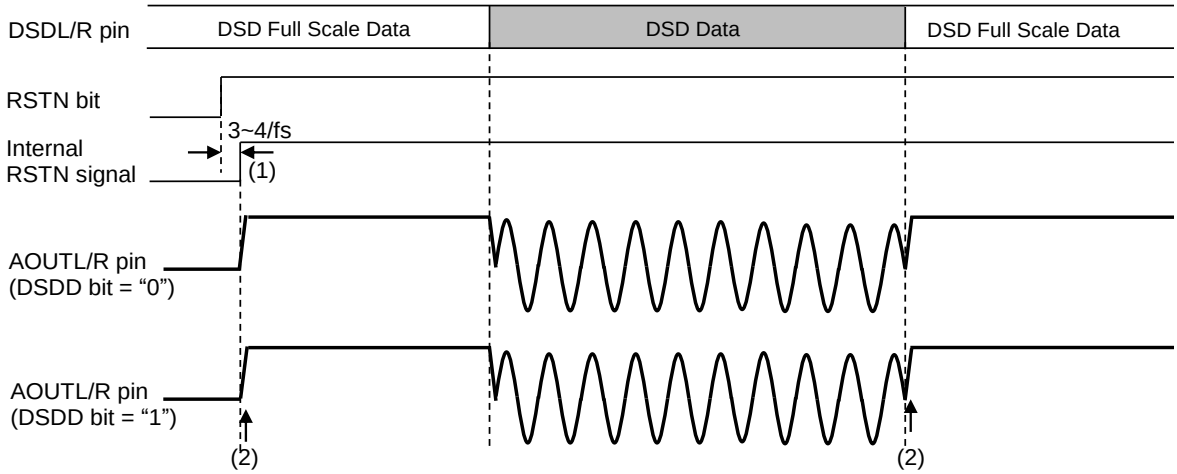
Table 28. DSD Full-scale Detection Time Setting

DDMT bit	Detection Time	Register Delay	
0	256 DCLK cycle	264 DCLK cycle	(default)
1	128 DCLK cycle	136 DCLK cycle	

Table 29. Relationship between Output Signal Transition Time and DSDD bit (DDM bit = “1”)

DSDD bit	Mode	Mute Transition time	Mute Release time	
0	Normal Path	Rapidly	As ATS[1:0] bits	(default)
1	Volume Bypass	Rapidly		

Full-scale detection signal can also be output from the DZF pin by setting DDMOE bit = “1”. If only one of L1/2/3/4 and R1/2/3/4 bits is set to “1”, DSD full-scale detection flag of selected channel is output from the DZF pin. If multiple bits are set to “1” or all L1/2/3/4 and R1/2/3/4 bits are set to “0”, OR’ed signal of DSD full-scale detection of all power-on channels (PWx bit = “1”) is output from the DZF pin.

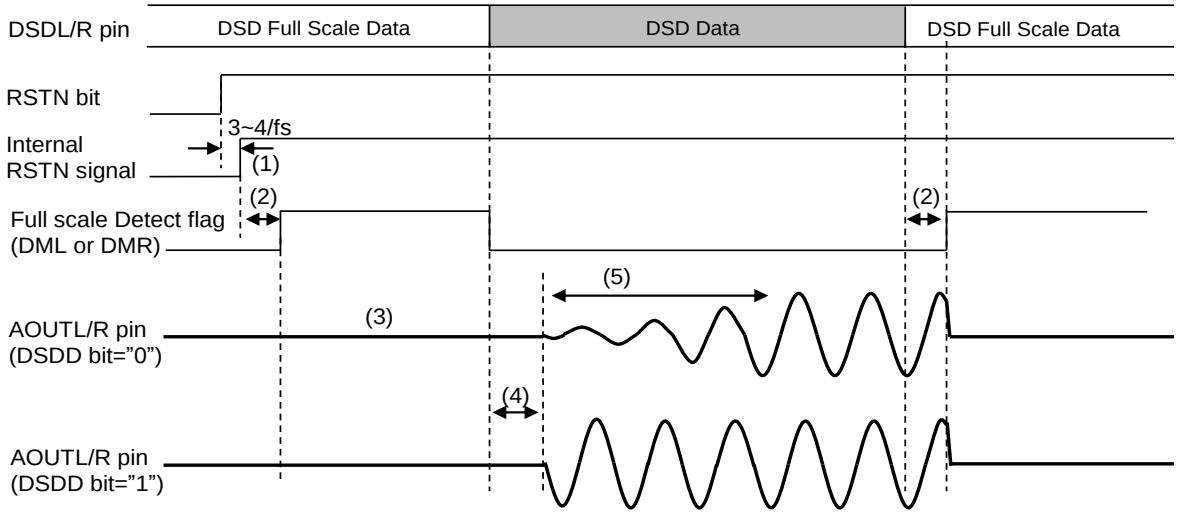


Notes:

(1) Internal reset is released after 3-4/fs by setting RSTN bit = "1".

(2) Excessive signals will be output from the analog output if full-scale signal is input after releasing internal reset. This behavior does not depend on DSDD bit setting.

Figure 50. Analog Output Waveform with DSD Full-scale Input (DDM bit = "0")



Notes:

(1) Internal reset is released after 3-4/fs by setting RSTN bit = "1".

(2) The internal detection flag becomes "1" if the input data is full-scale for a period set by DDMT bit after releasing internal reset.

(3) Analog output is forced to (VREFL + VERFR)/2 when full-scale signal is detected. No clicking noise occurs during a period from digital data input until full-scale detection since the analog output data delays for Register delay time (Table 28) if DDM bit is set to "1".

(4) Full-scale detection state is cleared when normal signal is input when the AK4468 is in full-scale detection state. Analog signal output starts after the Register delay time (Table 28) by clearing the full-scale detection state.

(5) Analog output transition time is different according to DSDD bit setting. When DSDD bit = "0", analog output transition time is set by ATS[1:0] bits (Table 25). When DSDD bit = "1", analog output recovers immediately.

Figure 51. Analog Output Waveform with DSD Full-scale Input (DDM bit = "1")

9.9. LR Channel Output Signal Select, Phase Inversion Function

In register control mode, input and output combination of the AK4468 can be changed by MONO1/2/3/4 bits and SELLR1/2/3/4 bits. In addition, the output signal phase can be inverted by INVL1/2/3/4 bits and INVR1/2/3/4 bits (Table 30). These functions are available on all audio formats.

Table 30. Output Select for DAC1/2/3/4 (Register Control Mode)

MONO1 bit	SELLR1 bit	INVL1 bit	INVR1 bit	L1 (AOUTL1N, AOUTL1P pins)	R1 (AOUTR1N, AOUTR1P pins)
0	0	0	0	L1ch in	R1ch in
		1	0	L1ch in Invert	R1ch in
		0	1	L1ch in	R1ch in Invert
		1	1	L1ch in Invert	R1ch in Invert
0	1	0	0	R1ch in	L1ch in
		1	0	R1ch in Invert	L1ch in
		0	1	R1ch in	L1ch in Invert
		1	1	R1ch in Invert	L1ch in Invert
1	0	0	0	L1ch in	L1ch in
		1	0	L1ch in Invert	L1ch in
		0	1	L1ch in	L1ch in Invert
		1	1	L1ch in Invert	L1ch in Invert
1	1	0	0	R1ch in	R1ch in
		1	0	R1ch in Invert	R1ch in
		0	1	R1ch in	R1ch in Invert
		1	1	R1ch in Invert	R1ch in Invert

MONO2 bit	SELLR2 bit	INVL2 bit	INVR2 bit	L2 (AOUTL2N, AOUTL2P pins)	R2 (AOUTR2N, AOUTR2P pins)
0	0	0	0	L2ch in	R2ch in
		1	0	L2ch in Invert	R2ch in
		0	1	L2ch in	R2ch in Invert
		1	1	L2ch in Invert	R2ch in Invert
0	1	0	0	R2ch in	L2ch in
		1	0	R2ch in Invert	L2ch in
		0	1	R2ch in	L2ch in Invert
		1	1	R2ch in Invert	L2ch in Invert
1	0	0	0	L2ch in	L2ch in
		1	0	L2ch in Invert	L2ch in
		0	1	L2ch in	L2ch in Invert
		1	1	L2ch in Invert	L2ch in Invert
1	1	0	0	R2ch in	R2ch in
		1	0	R2ch in Invert	R2ch in
		0	1	R2ch in	R2ch in Invert
		1	1	R2ch in Invert	R2ch in Invert

MONO3 bit	SELLR3 bit	INVL3 bit	INVR3 bit	L3 (AOUTL3N, AOUTL3P pins)	R3 (AOUTR3N, AOUTR3P pins)
0	0	0	0	L3ch in	R3ch in
		1	0	L3ch in Invert	R3ch in
		0	1	L3ch in	R3ch in Invert
		1	1	L3ch in Invert	R3ch in Invert
0	1	0	0	R3ch in	L3ch in
		1	0	R3ch in Invert	L3ch in
		0	1	R3ch in	L3ch in Invert
		1	1	R3ch in Invert	L3ch in Invert
1	0	0	0	L3ch in	L3ch in
		1	0	L3ch in Invert	L3ch in
		0	1	L3ch in	L3ch in Invert
		1	1	L3ch in Invert	L3ch in Invert
1	1	0	0	R3ch in	R3ch in
		1	0	R3ch in Invert	R3ch in
		0	1	R3ch in	R3ch in Invert
		1	1	R3ch in Invert	R3ch in Invert

MONO4 bit	SELLR4 bit	INVL4 bit	INVR4 bit	L4 (AOUTL4N, AOUTL4P pins)	R4 (AOUTR4N, AOUTR4P pins)
0	0	0	0	L4ch in	R4ch in
		1	0	L4ch in Invert	R4ch in
		0	1	L4ch in	R4ch in Invert
		1	1	L4ch in Invert	R4ch in Invert
0	1	0	0	R4ch in	L4ch in
		1	0	R4ch in Invert	L4ch in
		0	1	R4ch in	L4ch in Invert
		1	1	R4ch in Invert	L4ch in Invert
1	0	0	0	L4ch in	L4ch in
		1	0	L4ch in Invert	L4ch in
		0	1	L4ch in	L4ch in Invert
		1	1	L4ch in Invert	L4ch in Invert
1	1	0	0	R4ch in	R4ch in
		1	0	R4ch in Invert	R4ch in
		0	1	R4ch in	R4ch in Invert
		1	1	R4ch in Invert	R4ch in Invert

9.10. PCM/DSD Automatic Mode Switching Function

The AK4468 has automatic mode switching function that determines DSD or PCM mode from input signals of the BICK/DCLK pin (#2) and LRCK/DSDL1 pin (#3). This function is available by setting ADPE bit = “1” when the PDN pin = “H” in register control mode. DP bit is for manual setting. It will be ignored when ADPE bit is “1”. ADPE bit must be set while PW bit or RSTN bit = “0”.

To prevent clicking noises on mode switching, the mute function of DSD full-scale detection should be enabled by setting DDM bit = “1” when using this automatic mode switching function. DDM bit must be set while PW bit or RSTN bit = “0”.

Group delay will be 18/fs longer in PCM mode when setting ADPE bit = “1”, and 136-264 DCLK cycle longer according to full-scale detection time setting by DDMT bit in DSD mode when setting DDM bit = “1” (Table 28).

Automatic detection result can be read out by ADP bit. ADP bit outputs “0” in PCM mode and “1” in DSD mode if ADPE bit = “1”. The readout function of ADP bit is disabled if ADPE bit = “0” and “0” data is read out.

This function does not support DSD phase modulation format and edge inversion function of DSD receiving data (DCKB bit = “1”).

9.10.1. Mode Judgement Start Condition

If one of the five conditions shown below is satisfied, the AK4468 executes mode detection. The AK4468 keeps previous mode instead of executing mode detection if any condition is not satisfied.

1. Input data of all channels are zero for a period set by ADPT[1:0] bits (Table 31).
2. Output data of all channels are zero for a period set by ADPT[1:0] bits because of attenuation (Table 31).
3. Input data of all channels are full-scale for a period set by DDMT bit in DSD mode (Table 28).
4. PW1 bit = PW2 bit = PW3 bit = PW4 bit = “0”
5. RSTN bit = “0”

Table 31. Time Until Mode Detection after Input Data Becomes Zero

ADPT[1:0] bits	Wait Time	
00	8192/fs+18/fs	(default)
01	4096/fs+18/fs	
10	2048/fs+18/fs	
11	1024/fs+18/fs	

Note: fs = 30-48 kHz in DSD mode

9.10.2. Mode Detection

The AK4468 executes mode detection by comparing the input signal to the LRCK/DSDL1 pin (#3) to fixed code pattern. Input one of “01101001 01101001”, “01010101 01010101”, “00110011 00110011” code continuously to the LRCK/DSDL1 pin to transition to DSD mode from PCM mode (Table 32). Input a clock toggles in N*16BICK cycles (N must be an integral number greater than or equal to one) or a clock that keeps “L” or “H” for 32BICK cycles to the LRCK/DSDL1 pin (#3) to transition to PCM mode from DSD mode (Table 32). Refer to Figure 52 and Figure 53 for the operation sequence.

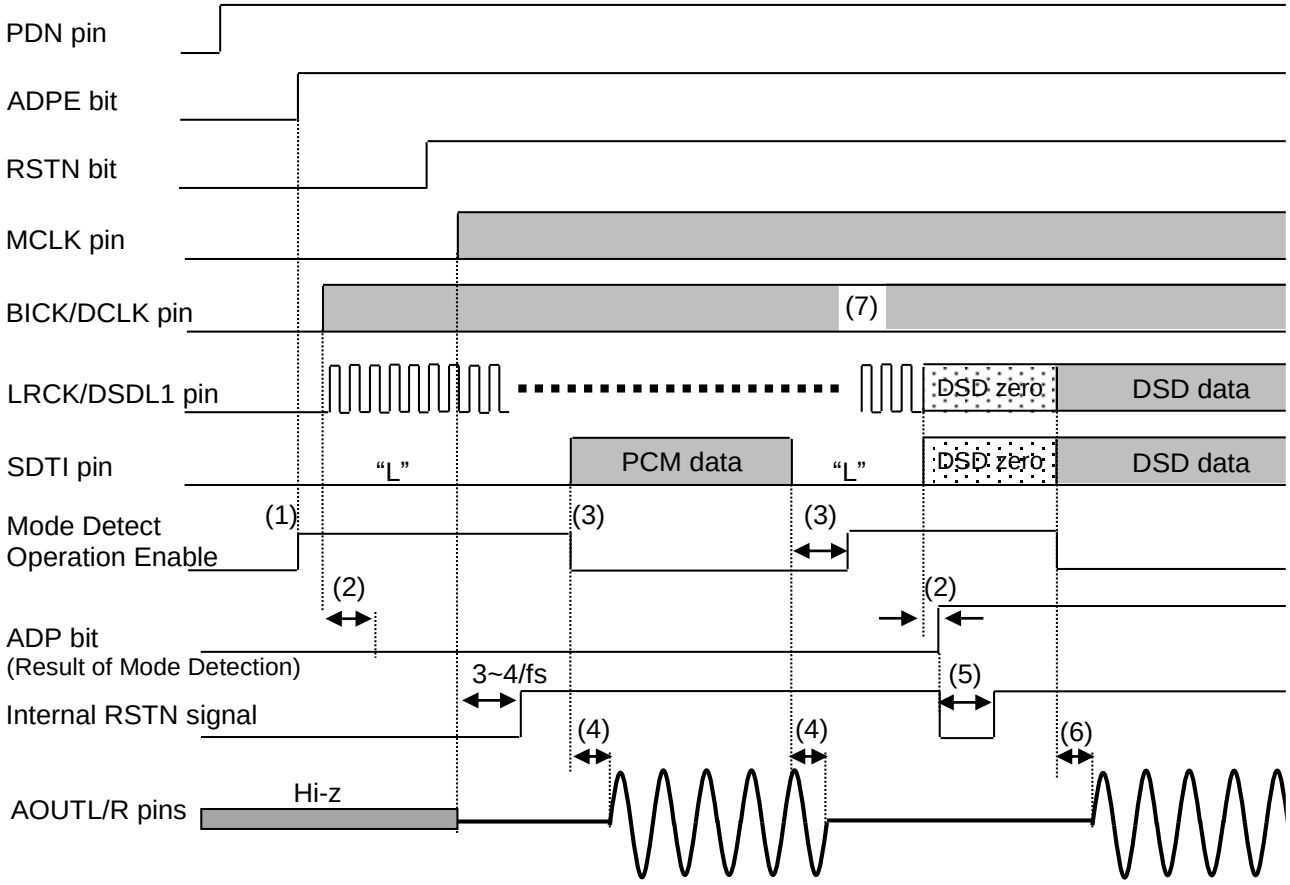
The AK4468 keeps previous mode instead of executing mode detection if any condition is not satisfied.

Table 32. Input Signal when Switching PCM/DSD Modes

#3 LRCK/DSDL1 Pin Input Signal	Detection Result
One of zero code pattern below is input twice consecutively “01101001 01101001” or “01010101 01010101” or “00110011 00110011”	DSD mode
Clock toggles in N*16BICK cycles (N ≥ 1) or Clock that keeps “L” or “H” for 32BICK cycles	PCM mode

The AK4468 executes data mode detection even if there is no MCLK input. However, the analog output becomes Hi-Z and the AK4468 enters standby state when MCLK is stopped. The AK4468 resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BICK/DCLK pin (#2) is stopped.

The AK4468 executes internal reset for 3-4/fs automatically when transition the data mode from DSD mode and resumes operation.



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(2) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDL1 pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDL1 pin. Mode detection is executed even when there is no MCLK input.

(3) The AK4468 finishes data mode detection when a data that is not zero is input. Then the AK4468 restarts the mode detection when input data of all channels are continuously zero for the period set by ADPT[1:0] bits.

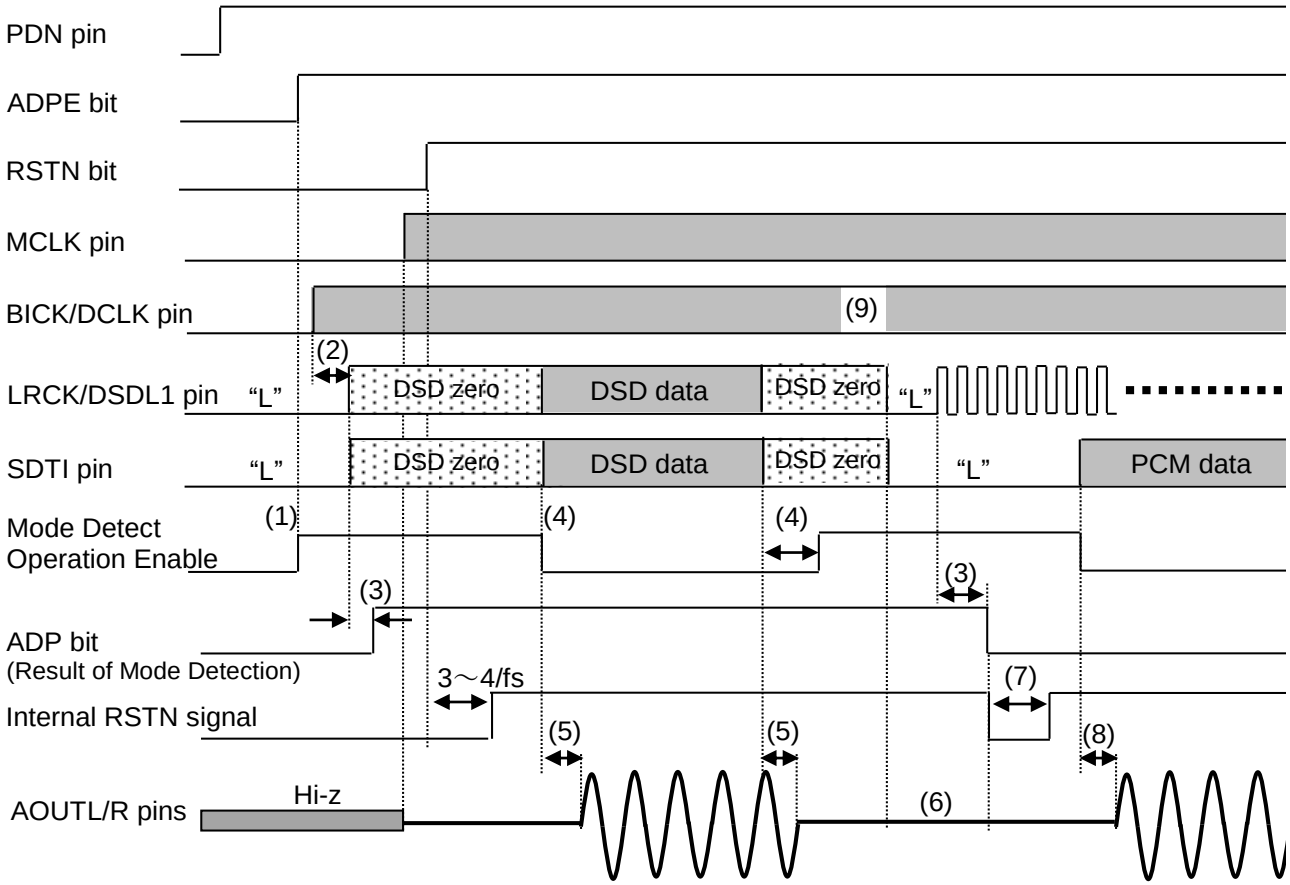
(4) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".

(5) When data mode is changed, the AK4468 executes internal reset for 3-4/fs automatically.

(6) In DSD mode, analog output delay time becomes longer comparing with when setting DDM bit = "0". In this case, delay time depends on DDMT bit setting.

(7) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin (#2) is stopped.

Figure 52. Changing to DSD mode after Power-up in PCM mode



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting ADPE bit = "1" after setting the PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(2) Upon power up the AK4468, the AK4468 operates in PCM mode if DCLK is input and DSDL1 is not input.

(3) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDL1 pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDL1 pin. ADP bit outputs "0" in PCM mode and "1" in DSD mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4468 finishes data mode detection when a data that is not zero is input. Then the AK4468 restarts the mode detection when input data of all channels are continuously zero for the period set by ADPT[1:0] bits.

(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(6) If DSD data input is stopped in DSD mode, the AK4468 stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4468. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

(7) When data mode is changed, the AK4468 executes internal reset for 3-4/fs automatically.

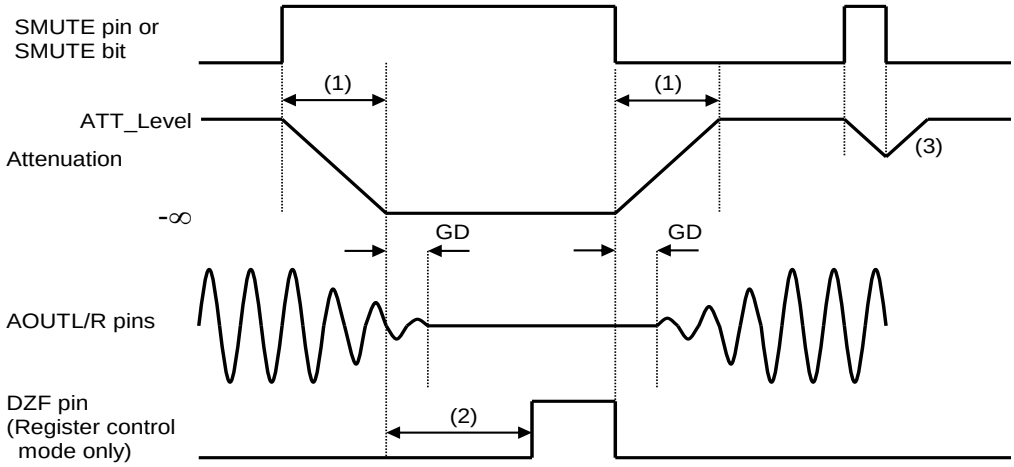
(8) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting DDM bit = "0".

(9) A clock input to the BICK/DSLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin (#2) is stopped.

Figure 53. Changing to PCM Mode after Power-up in DSD Mode

9.11. Soft Mute Operation

The soft mute operation is performed at digital domain. When setting the SMUTE pin to “H” or SMUTE bit to “1”, the output signal is attenuated by −∞ during ATT_DATA × ATT transition time of 1 code shift from the current ATT level. (Refer to Table 25 for ATT)
When setting back the SMUTE pin to “L” or SMUTE bit to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time of 1 code shift. If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time of 1 code shift. For example, this time is 4080/fs when ATT setting value is “FFH” and ATS[1:0] bits = “00”.
(2) When the input data for set channels (by L1/2/3/4 bits, R1/2/3/4 bits) is continuously zeros for a detection time shown in Table 27, the DZF pin goes to “H”. The DZF pin immediately returns to “L” if the input data is not zero.
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 54. Soft Mute Function

9.12. LDO

When TVDD = 3.0-3.6 V, the power for digital core circuit (VDD18) is supplied by the internal LDO by setting the LDOE pin to "H". Table 33 shows the VDD18 pin statuses with the PDN and LDOE pins setting. The internal LDO is powered up by setting the PDN pin from "L" to "H" (power down release) and it starts supplying 1.8 V to the VDD18 pin. Connect a 1 µF (±50%) capacitor to the VDD18 pin when using the LDO. To ensure reliable operation of the internal LDO, do not deviate more than ±50% from the recommended capacitor value. It takes 2 ms (max.) to power-up the internal LDO.

Table 33. LDO Select Mode (x: Do not care)

PDN	LDOE	TVDD	VDD18
x	L	1.7-3.6 V	LDO OFF: Supply 1.7-1.98 V to VDD18.
L	H	3.0-3.6 V	500 Ω Pull-down
H	H	3.0-3.6 V	LDO ON: LDO outputs 1.8 V (Do not connect with other device loads)

The AK4468 has error detect function, as shown in Table 34 for LDO operation (LDOE pin = "H"). The internal LDO will be powered down and stop supplying the power to the digital core when an error is detected. In this case, the analog signal output and the SDA pin becomes Hi-z state (In I^2C-Bus control mode, ACK is not output). The AK4468 must be reset by setting the PDN pin = "L" → "H" to recover from the error detection status.

Table 34. LDO Error Detection

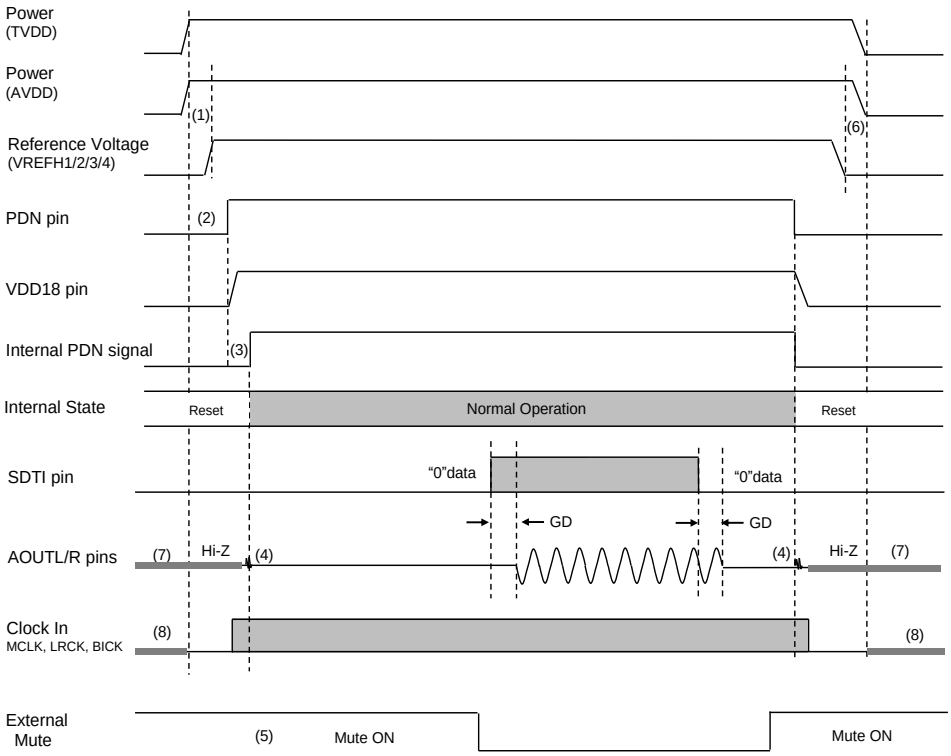
No	Error Detection	Error Detection Condition
1	LDO Overvoltage Detection	The AK4468 detects an error when the output voltage of the LDO pin exceeds overvoltage threshold. Threshold: 2.35 V (typ)
2	LDO Overcurrent Detection	The AK4468 detects an error when the current flows from LDO output exceeds overcurrent threshold. Threshold: 108 mA(typ)

9.13. Power Up/Down Sequence

The AK4468 is powered down when the PDN pin is “L”. In power down state, all circuits stop operation and initialized, and the analog output becomes floating (Hi-z) state. The PDN pin must held “L” for more than 150 ns for a certain reset after all power supplies are on. There is a possibility of malfunctions with the “L” pulse less than 150 ns. Power down is released by setting the PDN pin to “H” from “L”. In this time LDO (if LDOE pin = “H”) are powered up and the analog output becomes floating (Hi-z) state until all clocks are input.

9.13.1. Pin Control Mode (PS pin = “H” and I2C pin = “H”)

All circuits will be powered up by inputting MCLK, LRCK and BICK clocks after the PDN pin = “H”. Figure 55 shows system timing example of power down/up when using the internal LDO (LDOE pin = “H”).

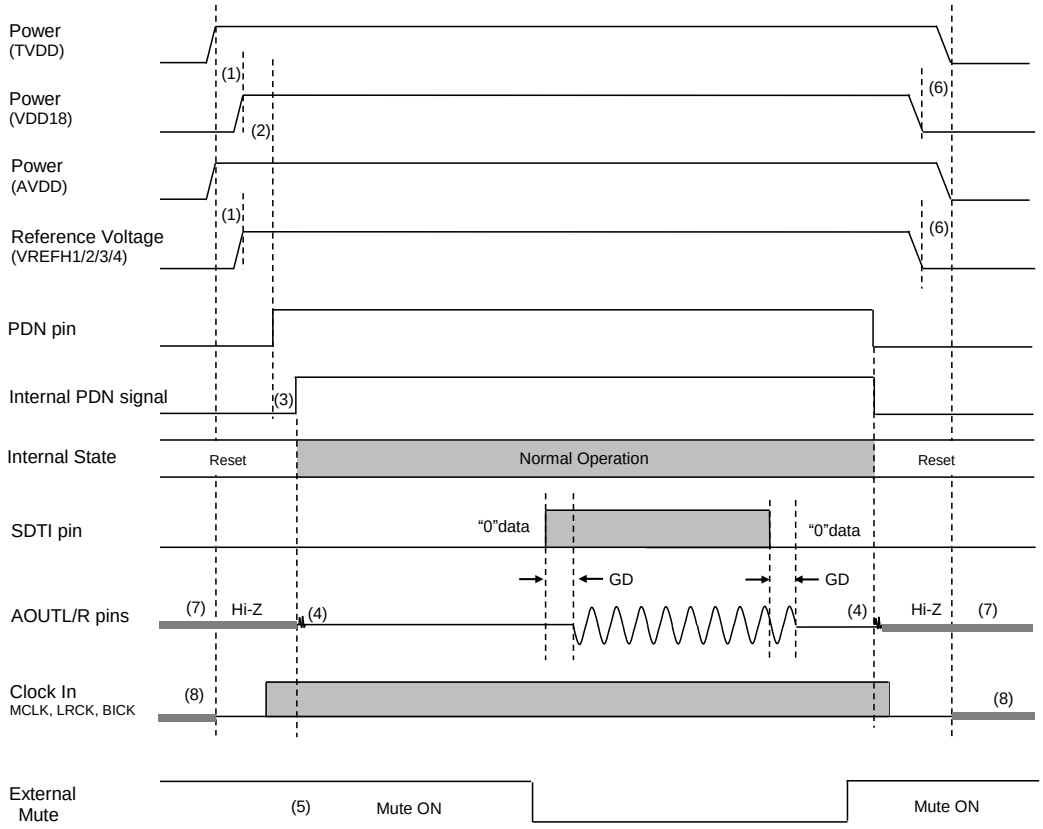


Notes:

(1) VREFH1/2/3/4 reference voltages should be input after AVDD is powered up or at the same time. Power up sequence between AVDD and TVDD are not critical.
(2) The PDN pin must be “L” when start supplying AVDD and TVDD. It must be held “L” for more than 150 ns after AVDD and TVDD are powered up.
(3) VDD18 output voltage (generated by Internal LDO) is powered up by setting the PDN pin = “H” if the LDOE pin = “H”. The internal PDN signal will rise in 2 ms (max.) after the PDN pin = “H” and the internal circuit will start operation.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) VREFH1/2/3/4 reference voltages should be stopped before AVDD is powered down or at the same time. Power down sequence between AVDD and TVDD are not critical.
(7) Analog outputs are floating (Hi-Z) in power down state.
(8) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 55. Power-up/down Sequence Example (Pin Control Mode, LDOE pin = “H”)

The timing example when not using the internal LDO (LDOE pin = “L”) is shown in Figure 56.



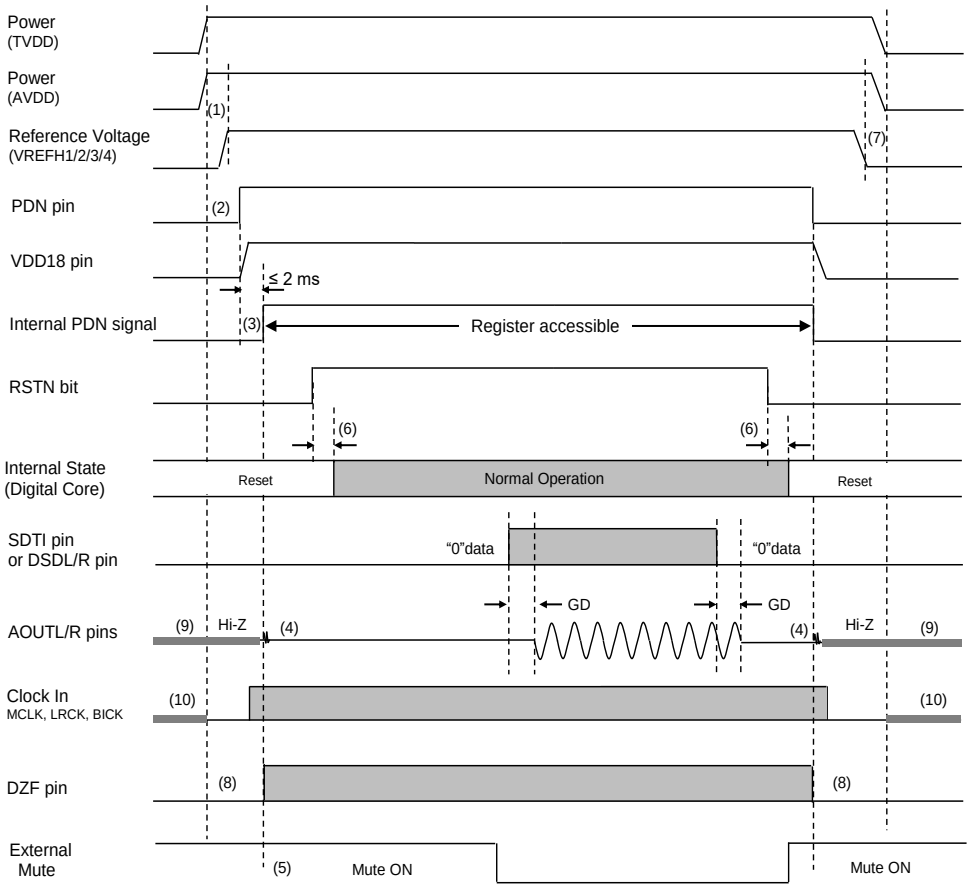
Notes:

(1) TVDD must be powered up before VDD18 is powered up or at the same time. Power up sequence between AVDD and TVDD, AVDD and VDD18 are not critical. VREFH1/2/3/4 reference voltages should be input after AVDD is powered up or at the same time.
(2) The PDN pin must be “L” when start supplying AVDD, TVDD and VDD18. It must be held “L” for more than 150 ns after AVDD, TVDD and VDD18 are powered up.
(3) When the LDOE pin = “L”, the internal PDN signal is on in 1 μs (max.) after the PDN pin is set to “H”, and the internal circuit will start operation.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) TVDD must be powered down after or at the same time of VDD18. Power down sequence between AVDD and TVDD, AVDD and VDD18 are not critical. VREFH1/2/3/4 reference voltages should be stopped before AVDD is powered down or at the same time.
(7) Analog outputs are floating (Hi-Z) in power down state.
(8) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 56. Power-up/down Sequence Example (Pin Control Mode, LDOE pin = “L”)

9.13.2. Register Control Mode (PS pin = “L” and I2C pin = “H”, or I2C pin = “L”)

Figure 57 shows system timing example of power down/up when using the internal LDO (LDOE pin = “H”). Register access becomes available and internal LDO is powered up after setting the PDN pin = “H”. The analog circuit starts operation by supplying necessary clocks (MCLK, LRCK and BICK for PCM mode, MCLK and DCLK for DSD mode). In this time, the analog output pins output analog common voltage (VREFH1/2/3/4 + VREFL1/2/3/4)/2. Then the AK4468 transitions to normal operation by setting RSTN bit = “1”.

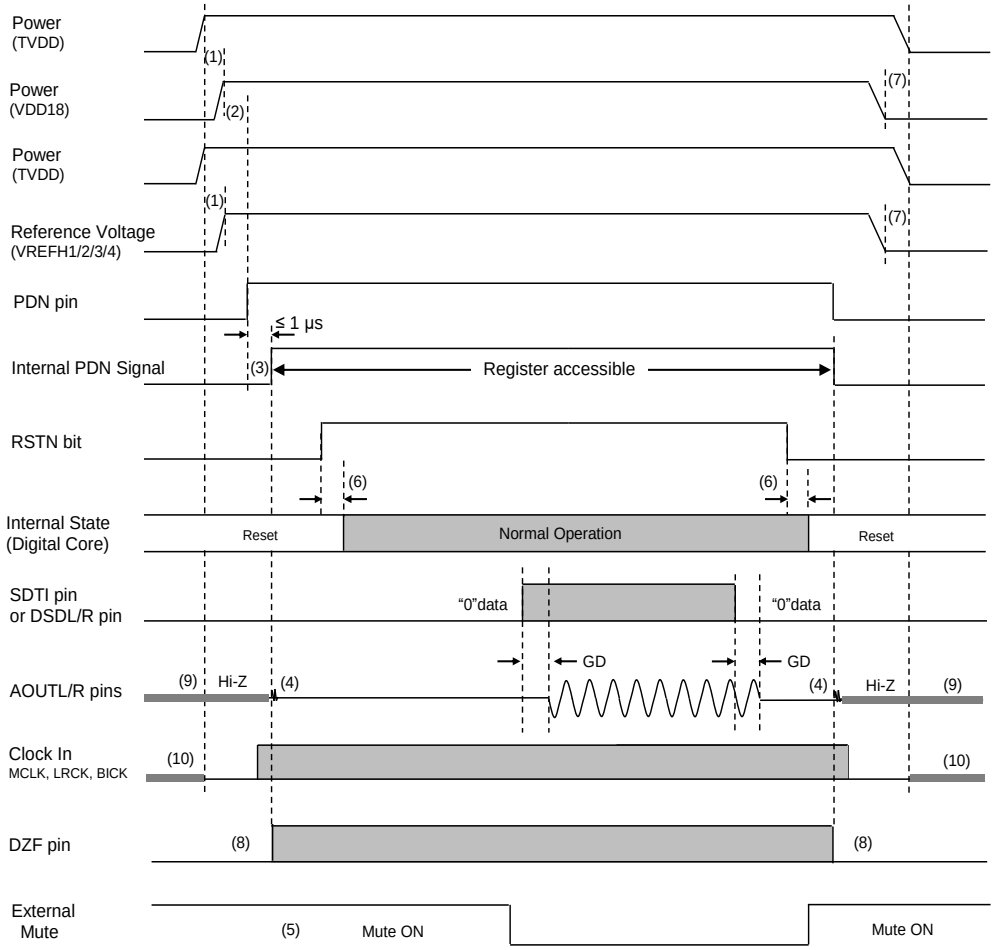


Notes:

(1) VREFH1/2/3/4 reference voltages should be input after AVDD is powered up or at the same time. Power up sequence between AVDD and TVDD are not critical.
(2) The PDN pin must be “L” when start supplying AVDD and TVDD. It must be held “L” for more than 150 ns after AVDD and TVDD are powered up.
(3) VDD18 output voltage (generated by Internal LDO) is powered up by setting the PDN pin = “H” if the LDOE pin = “H”. The internal PDN signal will rise in 2 ms (max.) after the PDN pin = “H” and control register access becomes available.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) It takes 3-4/fs until a reset instruction is valid when writing “0” to RSTN bit and it takes 3-4/fs when releasing the reset.
(7) VREFH1/2/3/4 reference voltages should be stopped before AVDD is powered down or at the same time. Power down sequence between AVDD and TVDD are not critical.
(8) The DZF pin outputs “L” in power down state.
(9) Analog outputs are floating (Hi-Z) in power down state.
(10) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 57. Power-up/down Sequence Example (Register Control Mode, LDOE pin = “H”)

The system timing example of power up/down when not using LDO (LODE pin = “L”) is shown in Figure 58.



Notes:

(1) TVDD must be powered up before VDD18 is powered up or at the same time. Power up sequence between AVDD and TVDD, AVDD and VDD18 are not critical. VREFH1/2/3/4 reference voltages should be input after AVDD is powered up or at the same time.
(2) The PDN pin must be “L” when start supplying AVDD, TVDD and VDD18. It must be held “L” for more than 150 ns after AVDD, TVDD and VDD18 are powered up.
(3) When the LDOE pin = “L”, the internal PDN signal is on in 1 μs (max.) after the PDN pin is set to “H”, and control register access becomes available.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) It takes 3-4/fs until a reset instruction is valid when writing “0” to RSTN bit and it takes 3-4/fs when releasing the reset.
(7) TVDD must be powered down after or at the same time of VDD18. Power down sequence between AVDD and TVDD, AVDD and VDD18 are not critical. VREFH1/2/3/4 reference voltages should be stopped before AVDD is powered down or at the same time.
(8) The DZF pin outputs “L” in power down state.
(9) Analog outputs are floating (Hi-Z) in power down state.
(10) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 58. Power-up/down Sequence Example (Register Control Mode, LDOE pin = “L”)

9.14. Power Down, Standby and Reset Function

Power Down, Standby and Reset functions of the AK4468 are controlled by PDN pin, PW bit, MCLK, and RSTN bit(Table 35, Table 36).

Table 35. Power Down, Standby and Reset Function (×: do not care)

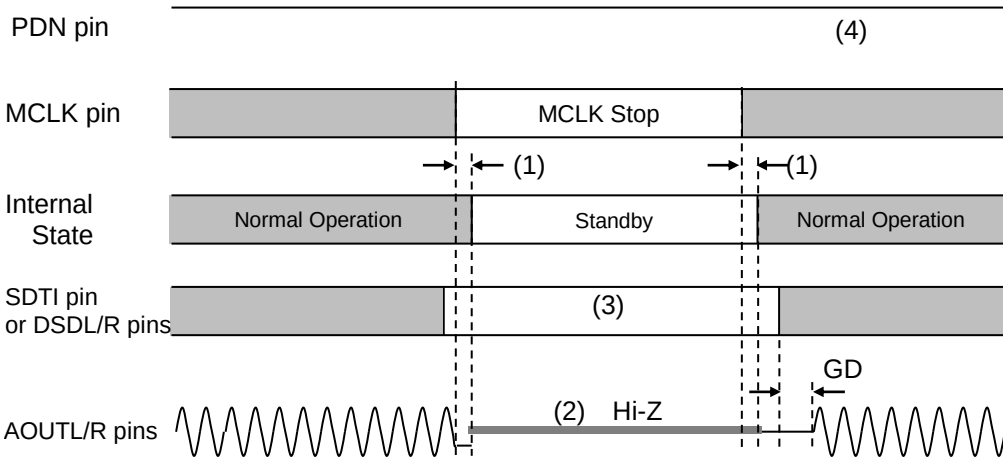
State	PDN pin	MCLK Input	PW1/2/3/4 bits	RSTN bit	DIGITAL Block	ANALOG Block	LDO / Register	Analog Output
Power Down	L	×	×	×	OFF	OFF	OFF	Hi-Z
Standby	H	No	×	×	OFF	OFF	ON	Hi-Z
	H	Yes	0	×	OFF	OFF	ON	Hi-Z
Reset	H	Yes	1	0	OFF	ON	ON	(VREFH1/2/3/4 +VREFL1/2/3/4)/ 2
Normal Operation	H	Yes	1	1	ON	ON	ON	Signal output

Table 36. Power Down, Standby and Reset function (detail)

PW1/2/3/4 bits	RSTN bit	Analog Output			
		DAC1	DAC2	DAC3	DAC4
0000	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1000	1	Signal output	Hi-Z	Hi-Z	Hi-Z
	0	(VREFH1+VR EFL1)/2	Hi-Z	Hi-Z	Hi-Z
0100	1	Hi-Z	Signal output	Hi-Z	Hi-Z
	0	Hi-Z	(VREFH2+VR EFL2)/2	Hi-Z	Hi-Z
0010	1	Hi-Z	Hi-Z	Signal output	Hi-Z
	0	Hi-Z	Hi-Z	(VREFH3+VR EFL3)/2	Hi-Z
0001	1	Hi-Z	Hi-Z	Hi-Z	Signal output
	0	Hi-Z	Hi-Z	Hi-Z	(VREFH4+VR EFL4)/2
1111	1	Signal output	Signal output	Signal output	Signal output
	0	(VREFH1+VR EFL1)/2	(VREFH2+VR EFL2)/2	(VREFH3+VR EFL3)/2	(VREFH4+VR EFL4)/2

9.14.1. Standby Sequence by MCLK

The AK4468 detects a clock stop and all circuits except MCLK stop detection circuit, control register and LDO (only when the LDOE pin = “H”) stop operation if MCLK is not input for 1 μs (min.) during operation (PDN pin = “H”). In this case, the analog output goes floating state (Hi-Z). The AK4468 returns to normal operation if PW bit and RSTN bit are “1” after starting to supply MCLK again. The zero detection function is disabled when MCLK is stopped.



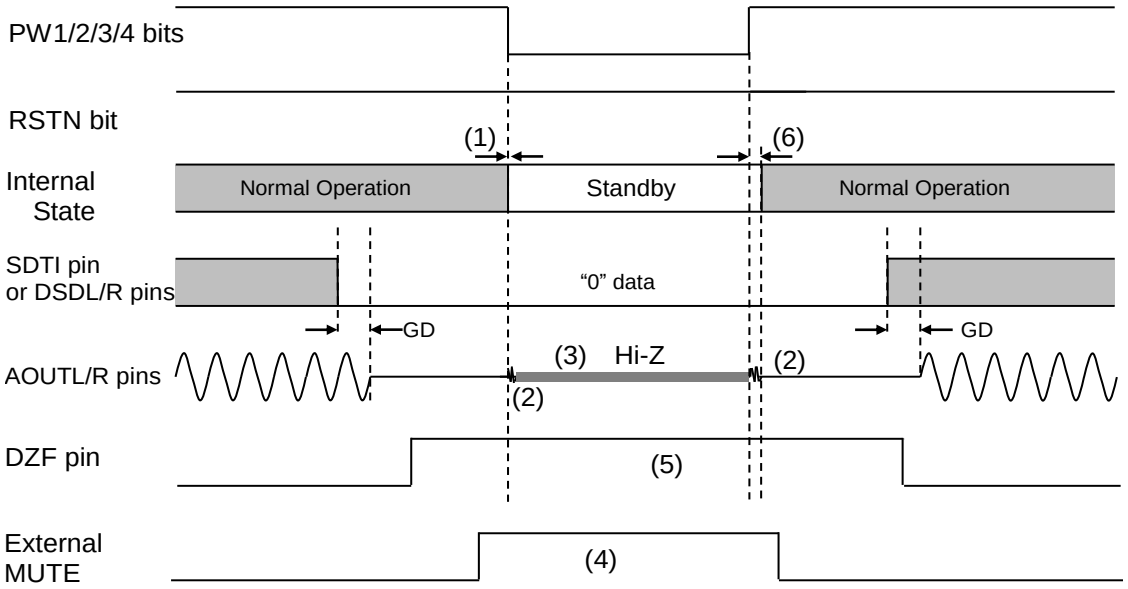
Notes:

(1) The AK4468 detects MCLK stop and becomes standby state when MCLK edge is not detected for 1 μs (min.) during operation.
(2) The analog output goes to floating state (Hi-Z) in standby state.
(3) Click noise can be reduced by inputting “0” data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the standby state by MCLK. In this case, power-up sequence by the PDN pin is not necessary.

Figure 59. Standby Sequence by MCLK

9.14.2. Standby Sequence by PW1/2/3/4 bits

All circuits except control register and LDO (only when the LDOE pin = “H”) stop operation by setting PW1/2/3/4 bits to “0”. In this case, control register access is available. The analog output goes to floating state (Hi-Z). Figure 60 shows standby sequence by PW1/2/3/4 bits.



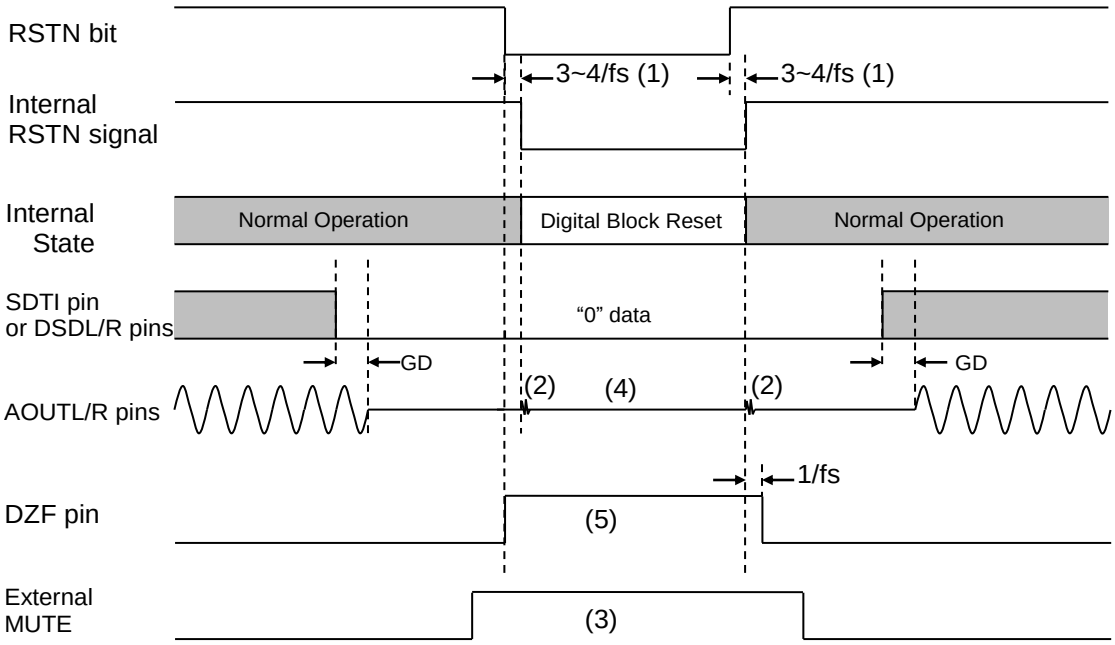
Notes:

(1) The corresponding channels become standby state immediately when writing “0” to PW1/2/3/4 bits.
(2) Click noise occurs on an edge of PW1/2/3/4 bits (“↓ ↑”). This noise is output even if “0” data is input.
(3) The analog output is floating (Hi-Z) state when PW1/2/3/4 bits = “0”.
(4) Mute the analog output externally if click noise (2) or Hi-z output (3) adversely affect system performance.
(5) The zero detection function is enable when the AK4468 is in standby state (PW1/2/3/4 bits = “0”). This figure shows the seuqnece when L1/2/3/4 bits = “1111”, R1/2/3/4 bits = “1111”, DZFB bit = “0” and DDMOE bit = “0”.
(6) It takes 2-3/fs until standby state is released when writing “1” to PW1/2/3/4 bits.

Figure 60. Standby Sequence by PW1/2/3/4 bits (Register Control Mode)

9.14.3. Reset by RSTN bit

Digital circuits except control registers and clock divider are reset by setting RSTN bit to “0”. In this case, control register settings are held, the analog output becomes (VREFH1/2/3/4+VREFL1/2/3/4)/2 V and the DZF pin outputs “H” (refer to “9.8.1 Zero Detection” for details). Figure 61 shows reset sequence by RSTN bit.



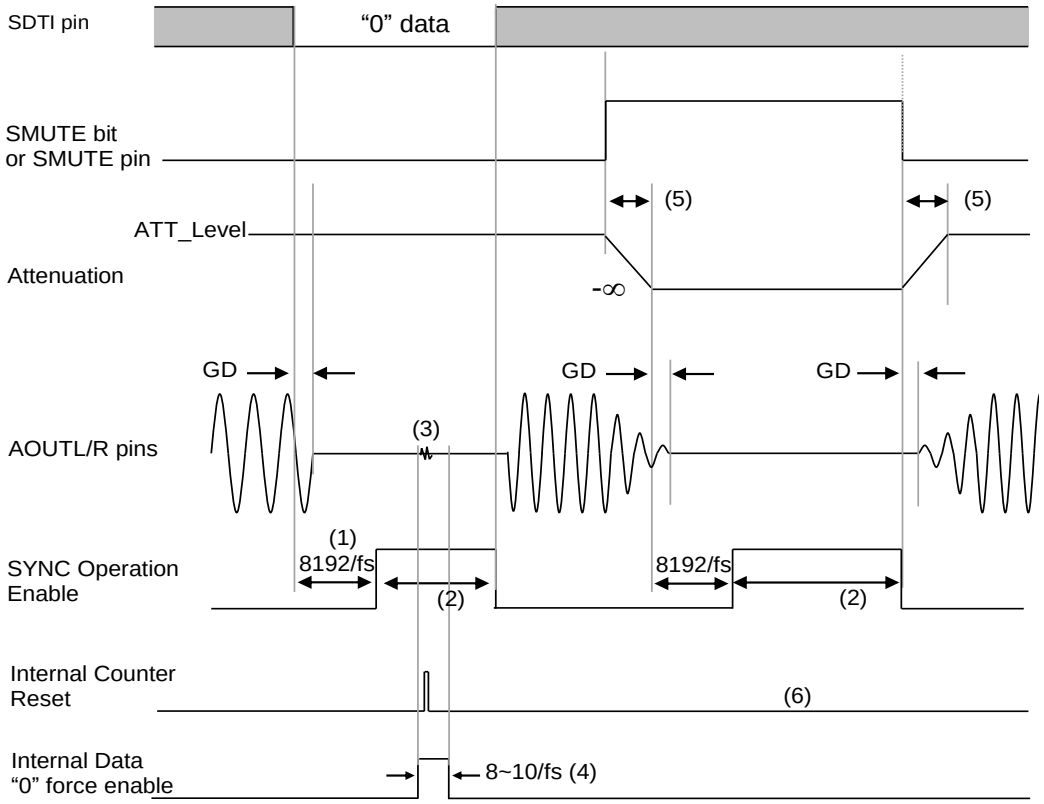
Notes:

(1) It takes 3-4/fs until a reset instruction is valid when changing RSTN bit to “0” and it takes 3-4/fs when releasing the reset.
(2) Click noise occurs on an edge of internal RSTN signal. This noise is output even if “0” data is input.
(3) Mute the analog output externally if click noise (2) adversely affect system performance.
(4) The analog output is (VREFH1/2/3/4+VREFL1/2/3/4)/2 V when RSTN bit = “0”.
(5) This figure shows the sequnece when DZFB bit = “0”, DDMOE bit = “0” and more than one bit among L1/2/3/4 bits and R1/2/3/4 bits is “1”. The DZF pin goes “H” on a falling edge of RSTN bit and goes “L” 1/fs after a rising edge of internal RSTN bit.

Figure 61. Reset Timing Example (Register Control Mode)

9.15. Synchronize Function (PCM mode)

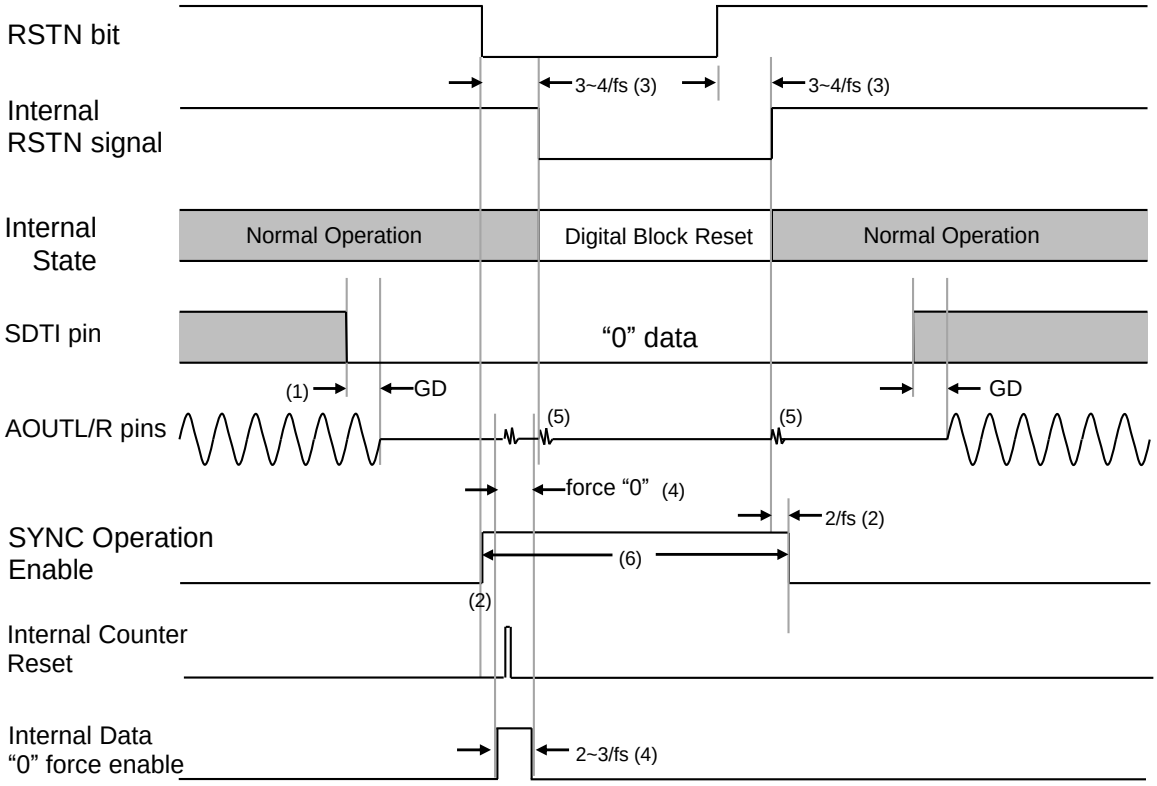
The AK4468 has a synchronize function. With this synchronize function, group delays between each device can be kept within 4/256 fs when using multiple AK4468's.
Clock synchronize function becomes valid when input data of all channels are "0" for 8192 times continuously in PCM mode, when all channels data become "0" and kept for 8192 times continuously by attenuation, or when RSTN bit = "0". In PCM mode, the internal counter is synchronized with a rising edge of LRCK (falling edge of LRCK when the data format is I²S compatible). In this case, the analog output becomes (VREFH1/2/3/4+VREFL1/2/3/4)/2 V.
This function is disabled by setting SYNCE bit = "0" in register control mode. Figure 62 shows a synchronizing sequence when the input data is "0" for 8192 times continuously. Figure 63 shows a synchronizing sequence by RSTN bit.



Notes:
(1) When all channels data are "0" for 8192 times continuously, the synchronize function is enabled.
(2) To ensure the synchronization, zero data input should be kept for 500 μs at least after the synchronize function is enabled.
(3) Input data of ΔΣ Modulator is fixed to "0" forcibly for 8 to 10/fs when internal counter is reset.
(4) Click noise may occur when the internal counter is reset. This noise is output even if "0" data is input. Mute the analog output externally if this click noise affects the system performance.
(5) Refer to "9.7 Digital Attenuation" for ATT transition time.
(6) When the internal clock and external input clock are in synchronization, the internal counter is not reset even if the synchronize function is valid.

Figure 62. Synchronization Sequence by Continuous "0" Data Input for 8192 Times

If RSTN bit is set to “0”, digital circuit is reset in 3-4/fs and the synchronization function becomes valid.



Notes:

(1) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing “0” to RSTN bit.

(2) The synchronization function becomes valid on a falling edge of RSTN bit. It takes 2-3/fs to become invalid after the internal RSTN is changed when changing RSTN bit to “1”.

(3) It takes 3-4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 3-4/fs when changing RSTN bit to “1”. The synchronization function becomes valid immediately when writing “0” to RSTN bit. Therefore, there is a case that the internal counter is reset before internal RSTN signal of the LSI is changed.

(4) Input data of ΔΣ Modulator is fixed to “0” forcibly for 2 to 3/fs when the internal counter is reset.

(5) Click noise occurs on rising and falling edges of the internal RSTN signal and when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this click noise affects the system performance.

(6) To ensure the synchronization, reset state should be kept for 500 μs at least after the synchronize function is enabled.

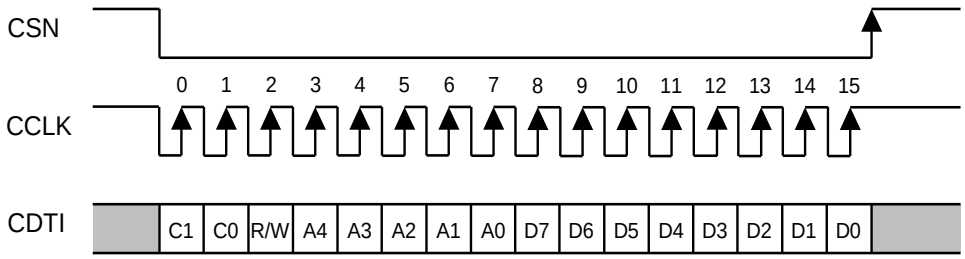
Figure 63. Synchronization Sequence by RSTN bit (Register Control Mode)

9.16. Register Control Interface

9.16.1. 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written to through 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2 bits, C1/0), Read/Write (1 bit; fixed to "1", write only), Register address (MSB first, 5 bits) and Control data (MSB first, 8 bits). The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The writing of data is valid when CSN "↑". The clock speed of CCLK is 5 MHz (max).

Setting the PDN pin to "L" resets the registers to their default values. In register control mode, the digital block except control registers and clock divider is reset by setting RSTN bit to "0". In this case, the register values are not initialized.



C1/C0:	Chip Address (C1 bit = CAD1 pin, C0 bit = CAD0_SPI pin)
R/W:	READ/WRITE (Fixed to "1", Write only)
A4/A3/A2/A1/A0:	Register Address
D7/D6/D5/D4/D3/D2/D1/D0:	Control Data

Figure 64. Control I/F Timing

Notes:
(1) The AK4468 does not support read commands in 3-wire serial control mode.
(2) When the PDN pin = "L", writing into control registers is prohibited.
(3) The control data cannot be written when the CCLK rising edge is 15 times or less, or 17 times or more during CSN is "L".

9.16.2. I²C-Bus Control Mode (I2C pin = "H", PS pin = "L")

The AK4468 supports the fast-mode I²C-Bus (max: 400 kHz, Ver. 1.0).

9.16.2.1. WRITE Operation

Figure 65 shows the data transfer sequence for the I²C-Bus control mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 71). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0_I2C pin) sets these device address bits (Figure 66). If the slave address matches that of the AK4468, the AK4468 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 72). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4468 and the format is MSB first. The most significant three bits are fixed as "000" (Figure 67). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 68). The AK4468 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 71).

The AK4468 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4468 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "15H" prior to generating a stop condition, the address counter will "roll over" to "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 73) except for the START and STOP conditions.

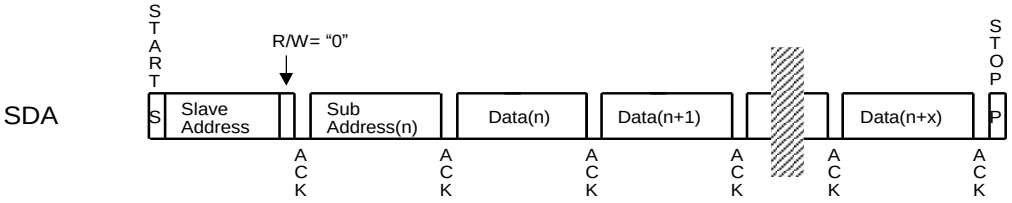


Figure 65. Data Transfer Sequence in I²C-Bus control mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1, CAD0 are set by pin)

Figure 66. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 67. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 68. Byte Structure after The Second Byte

9.16.2.2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4468. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.
The AK4468 supports two basic read operations: Current Address Read and Random Address Read.

9.16.2.2.1. Current Address Read

The AK4468 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4468 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4468 ceases the transmission.

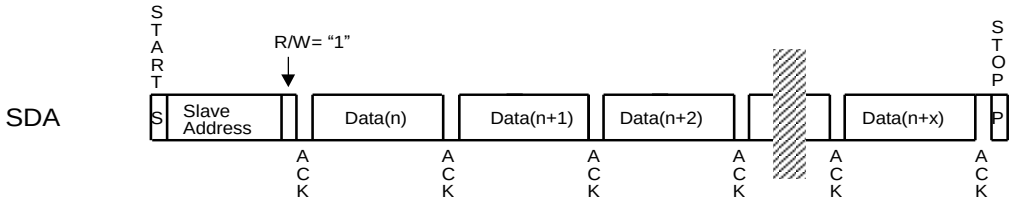


Figure 69. Current Address Read

9.16.2.2.2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4468 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4468 ceases the transmission.

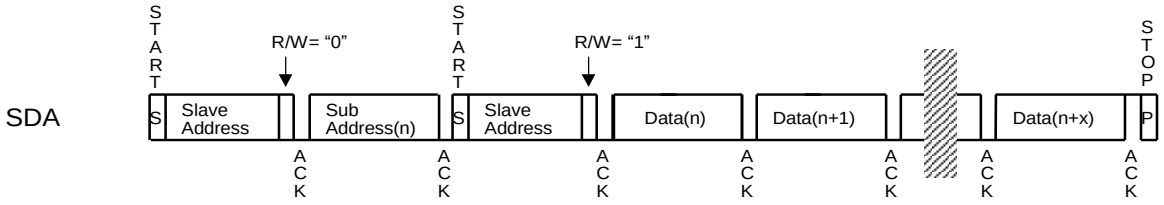


Figure 70. Random Address Read

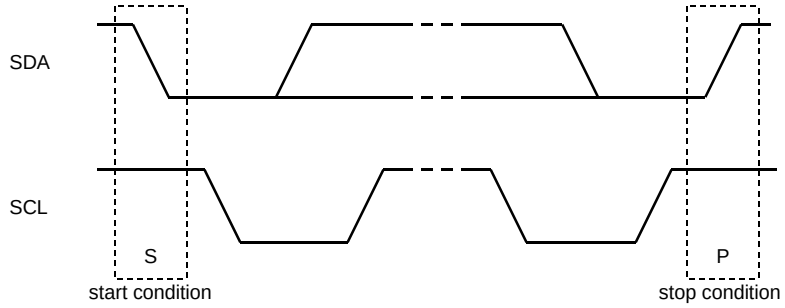


Figure 71. Start Condition and Stop Condition

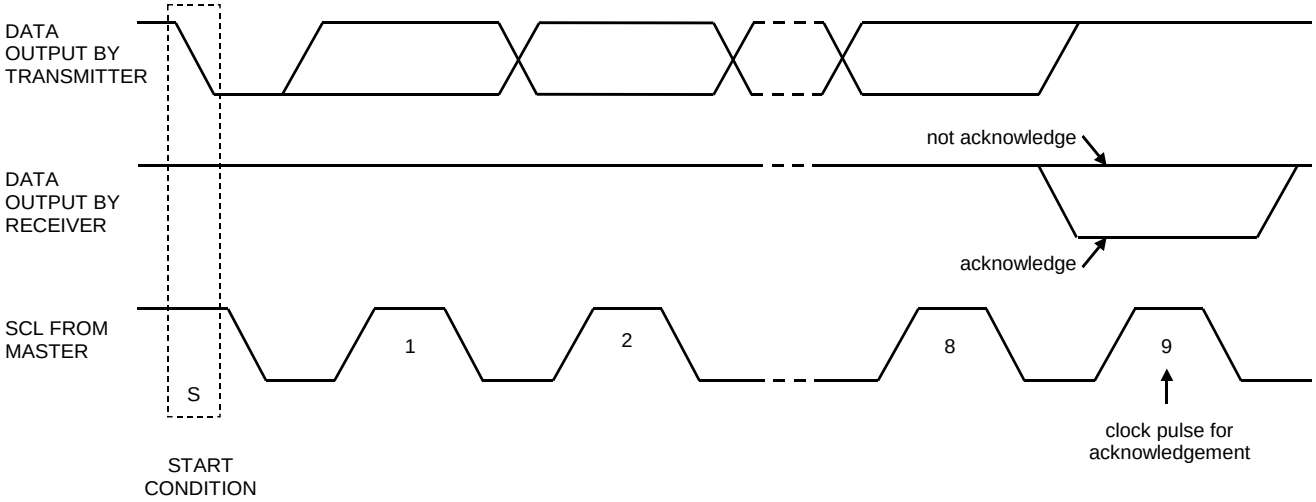


Figure 72. Acknowledge (I^2C-Bus)

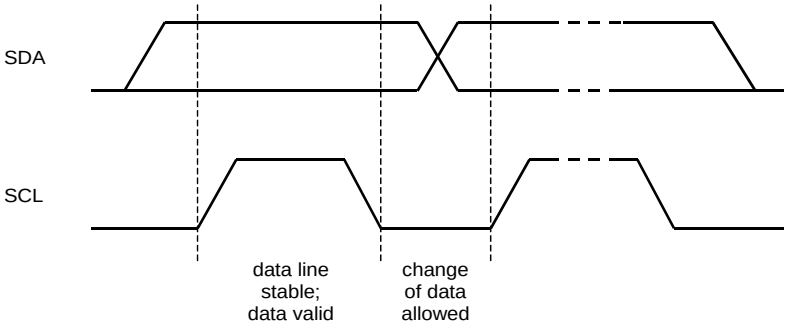


Figure 73. Bit Transfer (I^2C-Bus)

9.17. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	default
00H	Control 1	ACKS	0	0	0	DIF[2]	DIF[1]	DIF[0]	RSTN	0CH
01H	Control 2	0	0	SD	DFS[1]	DFS[0]	DEM1[1]	DEM1[0]	SMUTE	22H
02H	Control 3	DP	ADP	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW	00H
03H	L1ch ATT	ATTL1[7]	ATTL1[6]	ATTL1[5]	ATTL1[4]	ATTL1[3]	ATTL1[2]	ATTL1[1]	ATTL1[0]	FFH
04H	R1ch ATT	ATTR1[7]	ATTR1[6]	ATTR1[5]	ATTR1[4]	ATTR1[3]	ATTR1[2]	ATTR1[1]	ATTR1[0]	FFH
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS[2]	SSLOW	00H
06H	DSD1	DDM	DML1	DMR1	DDMOE	0	DDMT	DSDD	DSDSEL[0]	00H
07H	Control 5	L3	R3	L4	R4	0	0	1	SYNCE	03H
08H	Control 6	L1	R1	L2	R2	0	0	0	0	00H
09H	DSD2	DML2	DMR2	DML3	DMR3	DML4	DMR4	DSDF	DSDSEL[1]	00H
0AH	Control 7	TDM[1]	TDM[0]	SDS[1]	SDS[2]	PW2	PW1	DEM2[1]	DEM2[0]	0DH
0BH	Control 8	ATS[1]	ATS[0]	0	SDS[0]	PW4	PW3	DCHAIN	0	0CH
0CH	Control 9	INVL4	INVR4	INVL3	INVR3	0	0	0	0	00H
0DH	Control 10	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0	00H
0EH	Control 11	DEM4[1]	DEM4[0]	DEM3[1]	DEM3[0]	0	0	0	0	50H
0FH	L2ch ATT	ATTL2[7]	ATTL2[6]	ATTL2[5]	ATTL2[4]	ATTL2[3]	ATTL2[2]	ATTL2[1]	ATTL2[0]	FFH
10H	R2ch ATT	ATTR2[7]	ATTR2[6]	ATTR2[5]	ATTR2[4]	ATTR2[3]	ATTR2[2]	ATTR2[1]	ATTR2[0]	FFH
11H	L3ch ATT	ATTL3[7]	ATTL3[6]	ATTL3[5]	ATTL3[4]	ATTL3[3]	ATTL3[2]	ATTL3[1]	ATTL3[0]	FFH
12H	R3ch ATT	ATTR3[7]	ATTR3[6]	ATTR3[5]	ATTR3[4]	ATTR3[3]	ATTR3[2]	ATTR3[1]	ATTR3[0]	FFH
13H	L4ch ATT	ATTL4[7]	ATTL4[6]	ATTL4[5]	ATTL4[4]	ATTL4[3]	ATTL4[2]	ATTL4[1]	ATTL4[0]	FFH
14H	R4ch ATT	ATTR4[7]	ATTR4[6]	ATTR4[5]	ATTR4[4]	ATTR4[3]	ATTR4[2]	ATTR4[1]	ATTR4[0]	FFH
15H	Control 12	ADPE	ADPT[1]	ADPT[0]	0	0	0	0	0	00H

Notes:

(1) In 3-wire serial control mode, the AK4468 does not support read commands.
(2) The AK4468 supports read command in I^2C-Bus control mode.
(3) If the address exceeds “15H”, the address counter will “roll over” to “00H” and the next write/read address will be “00H” by automatic increment function in I^2C-Bus control mode.
(4) Bits indicated as 0 in each address must contain a “0” value. Malfunctions may occur if writing “1” to these bits.
(5) Writing data to addresses after 15H is forbidden. Malfunctions may also occur by this action.
(6) When the PDN pin goes to “L”, the registers are initialized to their default values.
(7) When RSTN bit is set to “0”, the digital block except control registers and clock divider is reset, and the registers are not initialized to their default values.

9.18. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF[2]	DIF[1]	DIF[0]	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized. (default)
1: Normal Operation

DIF[2:0]: Audio Data Interface Modes Select (Table 17)
The default value is “110” (Mode6: 32-bit MSB justified).

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM mode only). (Table 5, Table 6, Table 9)
0: Disable: Manual Setting Mode (default)
1: Enable: Auto Setting Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SD	DFS[1]	DFS[0]	DEM1[1]	DEM1[0]	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC Outputs Soft-muted.

DEM1[1:0]: DAC1 De-emphasis Filter Control (Table 23)
The default value is “01” (OFF).

DFS[2:0]: Sampling Speed Control (Table 6)
The default value is “000” (Normal Speed). Click noise occurs when DFS[2:0] bits are changed. See also Addr. 05H.

SD: Short Delay Filter Enable (Table 21)
0: Traditional Filter (SSLOW = “0”)
Super Slow Roll-off Filter (SSLOW = “1”)
1: Short delay Filter (SSLOW = “0”, default)
Low Dispersion Filter (SSLOW = “1”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	ADP	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable (Table 21)
0: Slow Roll-off Filter Disable (default)
1: Slow Roll-off Filter

SELLR1: DAC1 Data Selection of L channel and R channel (Table 30)

DZFB: Inverting Enable of DZF (Table 26)
0: DZF pin goes “H” at Zero Detection (default)
1: DZF pin goes “L” at Zero Detection

MONO1: DAC1 MONO/Stereo Mode Select (Table 30)
0: Stereo Mode (default)
1: Mono Mode

DCKB: Polarity of DCLK (DSD Mode Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD Mode (DSD mode only)
0: 512fs (default)
1: 768fs

ADP: Read Back Register for Internal Operation Mode. This bit is valid when ADPE bit = “1”.
It is invalid when ADPE bit = “0” and readouts “0” when read.
0: PCM Mode
1: DSD Mode

DP: DSD/PCM Mode Select
0: PCM Mode (default)
1: DSD Mode
∗When DP bit is changed, the AK4468 should be reset by RSTN bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	L1ch ATT	ATTL1[7]	ATTL1[6]	ATTL1[5]	ATTL1[4]	ATTL1[3]	ATTL1[2]	ATTL1[1]	ATTL1[0]
04H	R1ch ATT	ATTR1[7]	ATTR1[6]	ATTR1[5]	ATTR1[4]	ATTR1[3]	ATTR1[2]	ATTR1[1]	ATTR1[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL1[7:0]: DAC1 L-channel Attenuation Level Setting (Table 24)
ATTR1[7:0]: DAC1 R-channel Attenuation Level Setting (Table 24)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS[2]	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SSLOW: Super Slow Roll-off (Digital filter bypass mode) or Low Dispersion Filter Enable (Table 21)
0: Disable (default)
1: Enable (see also SD)

DFS[2:0]: Sampling Speed Control (Table 6)
The default value is “000” (Normal Speed). Click noise occurs when DFS[2:0] bits are changed. See also Addr. 01H.

SELLR2: DAC2 Data Selection of L-channel and R-channel (Table 30)

INVR2: DAC2 AOUTR2 Output Phase Inverting Mode
0: Disable (default)
1: Enable

INVL2: DAC2 AOUTL2 Output Phase Inverting Mode
0: Disable (default)
1: Enable

INVR1: DAC1 AOUTR1 Output Phase Inverting Mode
0: Disable (default)
1: Enable

INVL1: DAC1 AOUTL1 Output Phase Inverting Mode
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DSD1	DDM	DML1	DMR1	DDMOE	0	DDMT	DSDD	DSDSEL[0]
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL[1:0]: DSD Sampling Speed Control (Table 14). See also Addr. 09H.

DSDD: DSD Playback Path Control
0: Normal Path (default)
1: Volume Bypass

DDMT: DSD Signal Full-scale Detection Time Setting (Table 28)

DDMOE: Output Setting of the DMR/L Pins for DSD Full-scale Detection (Table 26)

DML1/R1: This register outputs detection flag when a full-scale signal is detected at DSDL1/R1 channel.

DDM: DSD Data Mute
The AK4468 has an internal mute function that mutes the output when DSD input data becomes all “1” or all “0” for 2048 samples (1/fs) continuously. DDM bit controls this function.
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	L3	R3	L4	R4	0	0	1	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

SYNCE: SYNC Mode Enable
0: SYNC Mode Disable
1: SYNC Mode Enable (default)

L3/4, R3/4: Zero Detection Flag Enable Bit for the DZF pin
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Control 6	L1	R1	L2	R2	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

L1/2, R1/2: Zero Detection Flag Enable Bit for the DZF pin
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DSD2	DML2	DMR2	DML3	DMR3	DML4	DMR4	DSDF	DSDSEL[1]
R/W		R	R	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL[1:0]: DSD Sampling Speed Control (Table 14). See also Addr. 06H.

DSDF: Cut-off Frequency of DSD Filter Control (Table 22)

DML2/3/4, DMR2/3/4: This register outputs detection flag when a full-scale signal is detected at DSDL2/3/4 pins and DSDR2/3/4 pins.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control7	TDM[1]	TDM[0]	SDS[1]	SDS[2]	PW2	PW1	DEM2[1]	DEM2[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

DEM2[1:0]: DAC2 De-emphasis Filter Control (Table 23)
The default value is “01” (OFF).

PW1: DAC1 Power Control (Table 36)

PW2: DAC2 Power Control (Table 36)

SDS[2:0]: Output Data Slot Selection of Each Channel (Table 18)
The default value is “000”. See also Addr. 0BH.

TDM[1:0]: TDM Mode Select
00: Normal (default)
01: TDM128
10: TDM256
11: TDM512

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 8	ATS[1]	ATS[0]	0	SDS[0]	PW4	PW3	DCHAIN	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

DCHAIN: Daisy Chain Mode Enable
0: Daisy Chain Mode Disable (default)
1: Daisy Chain Mode Enable

PW3: DAC3 Power Control (Table 36)

PW4: DAC4 Power Control (Table 36)

SDS[2:0]: Output Data Slot Selection for Each Channel (Table 18)
The default value is “000”. See also Addr. 0AH.

ATS[1:0]: Transition time between set values of ATTL/R[7:0] bits (Table 25)
The default value is “00”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Control 9	INVL4	INVR4	INVL3	INVR3	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INVR3: DAC3 AOUTR3 Output Phase Inverting Mode
INVL3: DAC3 AOUTL3 Output Phase Inverting Mode
INVR4: DAC3 AOUTR4 Output Phase Inverting Mode
INVL4: DAC3 AOUTL4 Output Phase Inverting Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Control 10	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SELLR3: DAC3 Data Selection of L-channel and R-channel (Table 30)

SELLR4: DAC4 Data Selection of L-channel and R-channel (Table 30)

MONO2: DAC2 MONO/Stereo Mode Select (Table 30)
0: Stereo Mode (default)
1: Mono Mode

MONO3: DAC3 MONO/Stereo Mode Select (Table 30)
0: Stereo Mode (default)
1: Mono Mode

MONO4: DAC4 MONO/Stereo Mode Select (Table 30)
0: Stereo Mode (default)
1: Mono Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Control 11	DEM4[1]	DEM4[0]	DEM3[1]	DEM3[0]	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	0	0

DEM3[1:0]: DAC3 De-emphasis Filter Control (Table 23)
DEM4[1:0]: DAC4 De-emphasis Filter Control (Table 23)
The default value is “01” (OFF).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	L2ch ATT	ATTL2[7]	ATTL2[6]	ATTL2[5]	ATTL2[4]	ATTL2[3]	ATTL2[2]	ATTL2[1]	ATTL2[0]
10H	R2ch ATT	ATTR2[7]	ATTR2[6]	ATTR2[5]	ATTR2[4]	ATTR2[3]	ATTR2[2]	ATTR2[1]	ATTR2[0]
11H	L3ch ATT	ATTL3[7]	ATTL3[6]	ATTL3[5]	ATTL3[4]	ATTL3[3]	ATTL3[2]	ATTL3[1]	ATTL3[0]
12H	R3ch ATT	ATTR3[7]	ATTR3[6]	ATTR3[5]	ATTR3[4]	ATTR3[3]	ATTR3[2]	ATTR3[1]	ATTR3[0]
13H	L4ch ATT	ATTL4[7]	ATTL4[6]	ATTL4[5]	ATTL4[4]	ATTL4[3]	ATTL4[2]	ATTL4[1]	ATTL4[0]
14H	R4ch ATT	ATTR4[7]	ATTR4[6]	ATTR4[5]	ATTR4[4]	ATTR4[3]	ATTR4[2]	ATTR4[1]	ATTR4[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL2/3/4[7:0]: DAC2/3/4 L-channel Attenuation Level Setting (Table 24)
ATTR2/3/4[7:0]: DAC2/3/4 R-channel Attenuation Level Setting (Table 24)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Control 12	ADPE	ADPT[1]	ADPT[0]	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

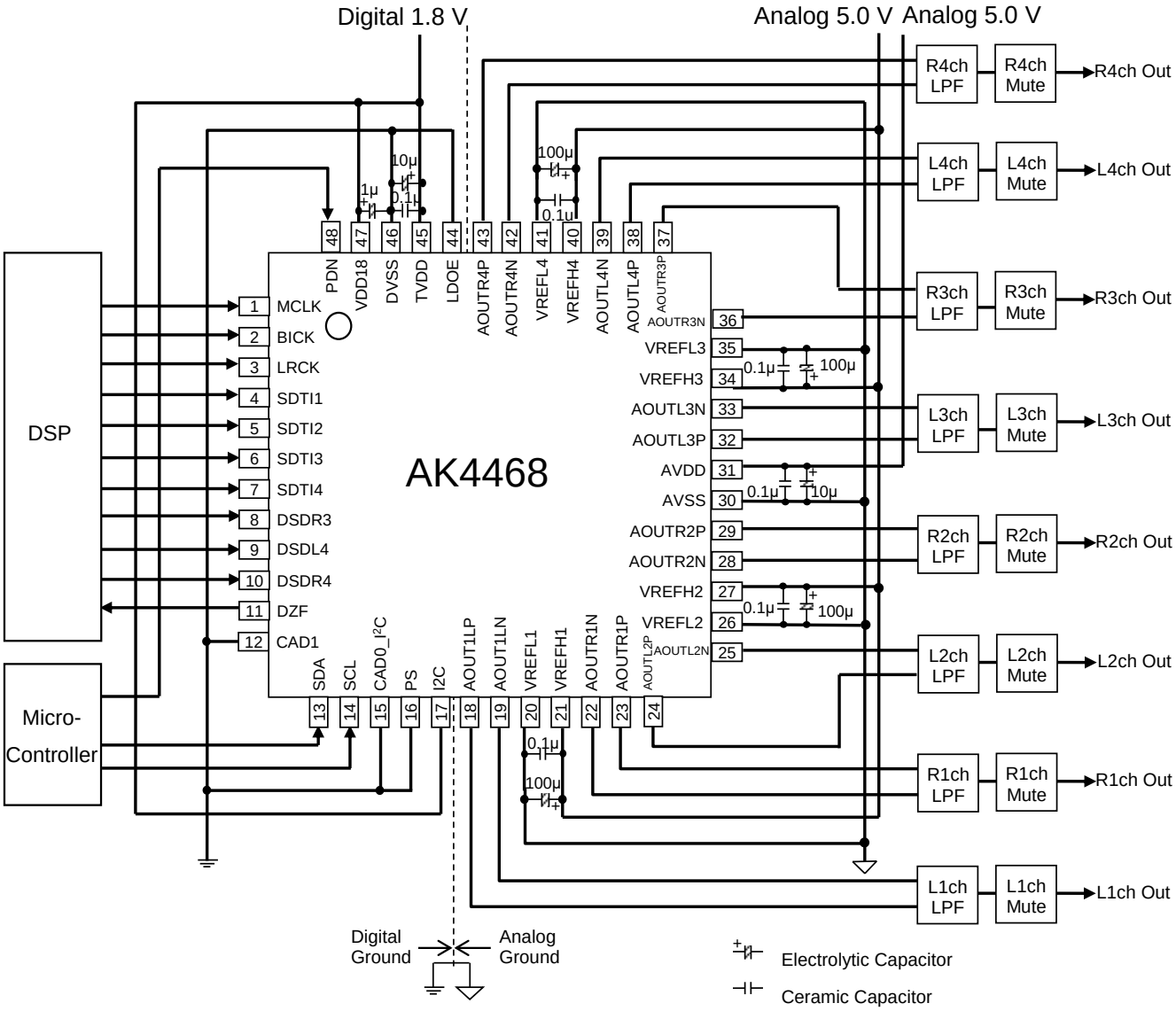
ADPT[1:0]: Time until PCM/DSD mode detection when input data becomes zero (Table 31)

ADPE: PCM/DSD Automatic Mode Switching Function Enable Bit
0: Disable (default)
1: Enable

10. Recommended External Circuits

10.1. Recommended External Circuits

10.1.1. Register Control Mode, LDO Disable.



Notes:

(1) Power lines of AVDD and TVDD should be distributed separately with low impedance of regulators, etc. maintained.

(2) AVSS and DVSS must be connected to the same analog ground plane. (Analog ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)

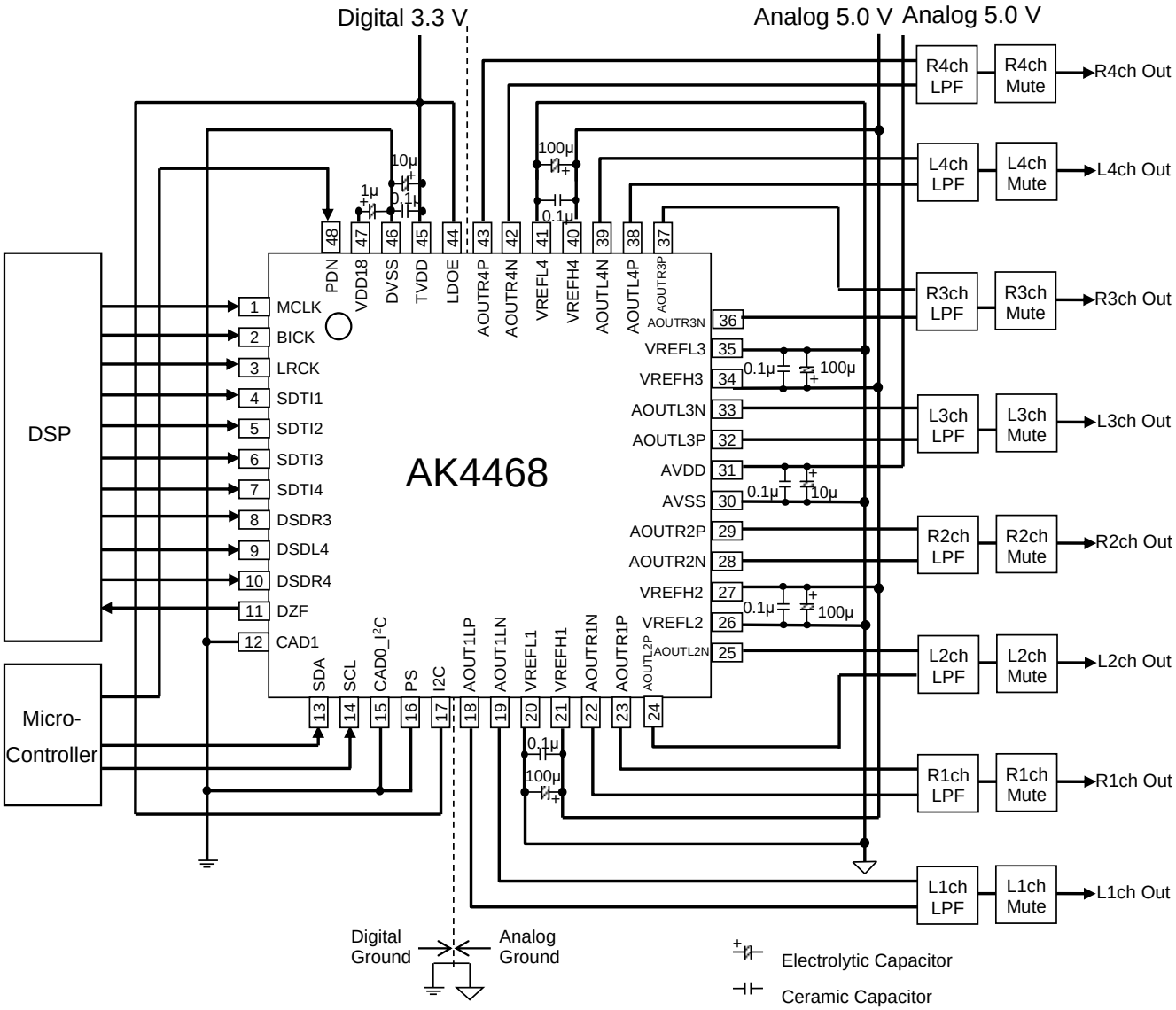
(3) It is recommended to input MCLK via a damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of MCLK.

(4) Power lines of AVDD and VREFH1/2/3/4 should be distributed separately with low impedance of regulators, etc. maintained. It is recommended to separate the wiring of AVDD and VREFH1/2/3/4. It is also recommended to connect a 0.1 µF and a 100 µF capacitors between VREFL1/2/3/4 and VREFH1/2/3/4.

(5) All digital input pins except pull-down/pull-up pins should not be allowed to float.

Figure 74. Typical Connection Diagram
(AVDD = 5.0 V, TVDD = 1.8 V, VDD18 = 1.8 V, LDOE pin = “L”, Register Control Mode)

10.1.2. Register control mode, LDO enable



Notes:

(1) Power lines of AVDD and TVDD should be distributed separately with low impedance of regulators, etc. maintained.

(2) AVSS and DVSS must be connected to the same analog ground plane. (Analog ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)

(3) It is recommended to input MCLK via a damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of MCLK.

(4) Power lines of AVDD and VREFH1/2/3/4 should be distributed separately with low impedance of regulators, etc. maintained. It is recommended to separate the wiring of AVDD and VREFH1/2/3/4. It is also recommended to connect a 0.1 µF and a 100 µF capacitors between VREFL1/2/3/4 and VREFH1/2/3/4.

(5) All digital input pins except pull-down/pull-up pins should not be allowed to float.

(6) A 1 µF capacitor (±50%, including temperature characteristics) must be connected to the VDD18 pin.

Figure 75. Typical Connection Diagram
(AVDD = 5.0 V, TVDD = 3.3 V, LDOE pin = “H”, Register Control Mode)

10.2. Grounding and Power Supply Decoupling

To minimize coupling of digital noise, decoupling capacitors should be connected to AVDD, TVDD and VDD18. AVDD is supplied from analog supply in system, and TVDD and VDD18 are supplied from digital supply in system. Power line of AVDD should be distributed separately, from the point with low impedance of regulators or other parts. When not using the LDO (LDOE pin = “L”), TVDD must be powered up before or at the same time of VDD18.
AVSS and DVSS must be connected to the same analog ground plane. Decoupling capacitors for high frequency should be placed as near as possible to the AK4468.

10.3. Reference Voltage

The VREFH1/2/3/4 pin is normally connected to 5.0 V reference voltage, and the VREFL1/2/3/4 pin is normally connected to the analog ground. Connect a 0.1 μF ceramic and a 100 μF electrolytic capacitors between VREFH1/2/3/4 and VREFL1/2/3/4. Especially the ceramic capacitors should be connected as near as possible to the pin.

The potential difference between VREFH1/2/3/4 and VREFL1/2/3/4 set the full-scale of the analog output range. Therefore, the VREFH1/2/3/4 and VREFL1/2/3/4 pins should avoid noises from other power supplies. When it is difficult to obtain expected analog characteristics because of noises from other power supplies, connect the VREFH1/2/3/4 pin to the analog 5.0 V via a 10 Ω resistor, and the VREFL1/2/3/4 pin to the analog ground via a 10 Ω resistor. In addition, connect a 220 μF electrolytic capacitor between VREFH1/2/3/4 and VREFL1/2/3/4. A low pass filter of fc = 36 Hz will be composed with the 220 μF capacitor and the 10 Ω resistor. It removes differential noise between VREFH1/2/3/4 and VREFL1/2/3/4.

All digital signals, especially clocks, should be kept away from the VREFH1/2/3/4 and VREFL1/2/3/4 pins in order to avoid unwanted coupling into the AK4468.

10.4. Analog Output

The analog outputs are full differential outputs. The differential outputs are summed externally. When the summing gain is 1 and VREFH1/2/3/4 – VREFL1/2/3/4 = 5 V, the output range is 5.6 Vpp (typ.). The bias voltage of the external summing circuit is supplied externally.

Figure 76 and Figure 77 show examples of external LPF circuit summing the differential outputs by a single op-amp. Figure 78 shows an example of external LPF with two op-amps and differential output circuits.

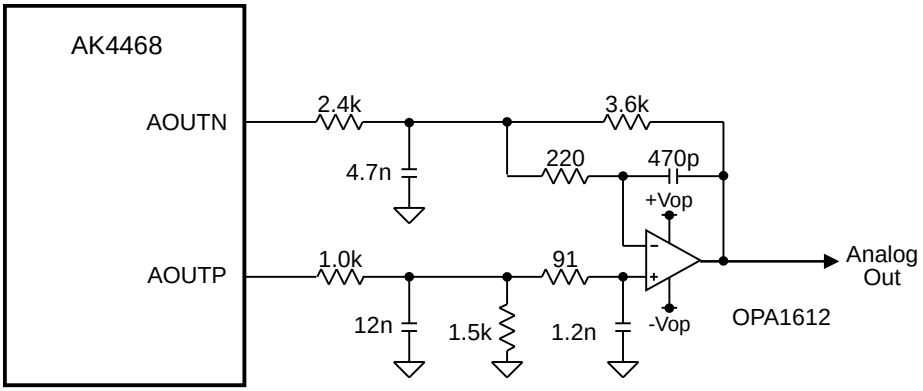


Figure 76. External LPF Circuit Example 1 (fc = 111 kHz (Typ), Q = 0.677 (Typ))

Table 37. Frequency Response of External LPF Circuit Example 1

Gain (1 kHz, Typ)		+3.52 dB
Frequency Response (ref:1 kHz, Typ)	20 kHz	-0.16 dB
	40 kHz	-0.35 dB
	80 kHz	-1.31 dB

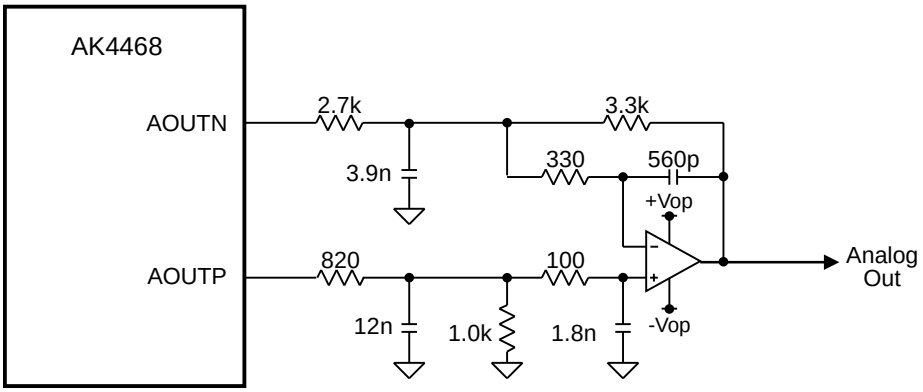


Figure 77. External LPF Circuit Example 2 (fc = 103 kHz (Typ), Q = 0.651 (Typ))

Table 38. Frequency Response of External LPF Circuit Example 2

Gain (1 kHz, Typ)		+1.74 dB
Frequency Response (ref:1 kHz, Typ)	20 kHz	+0.06 dB
	40 kHz	+0.01 dB
	80 kHz	-1.43 dB

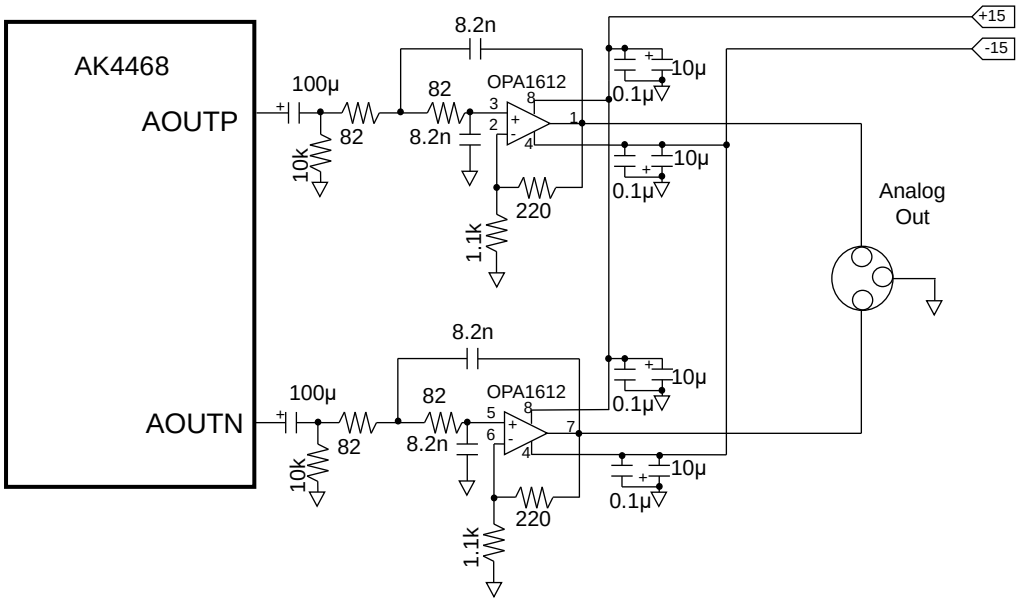


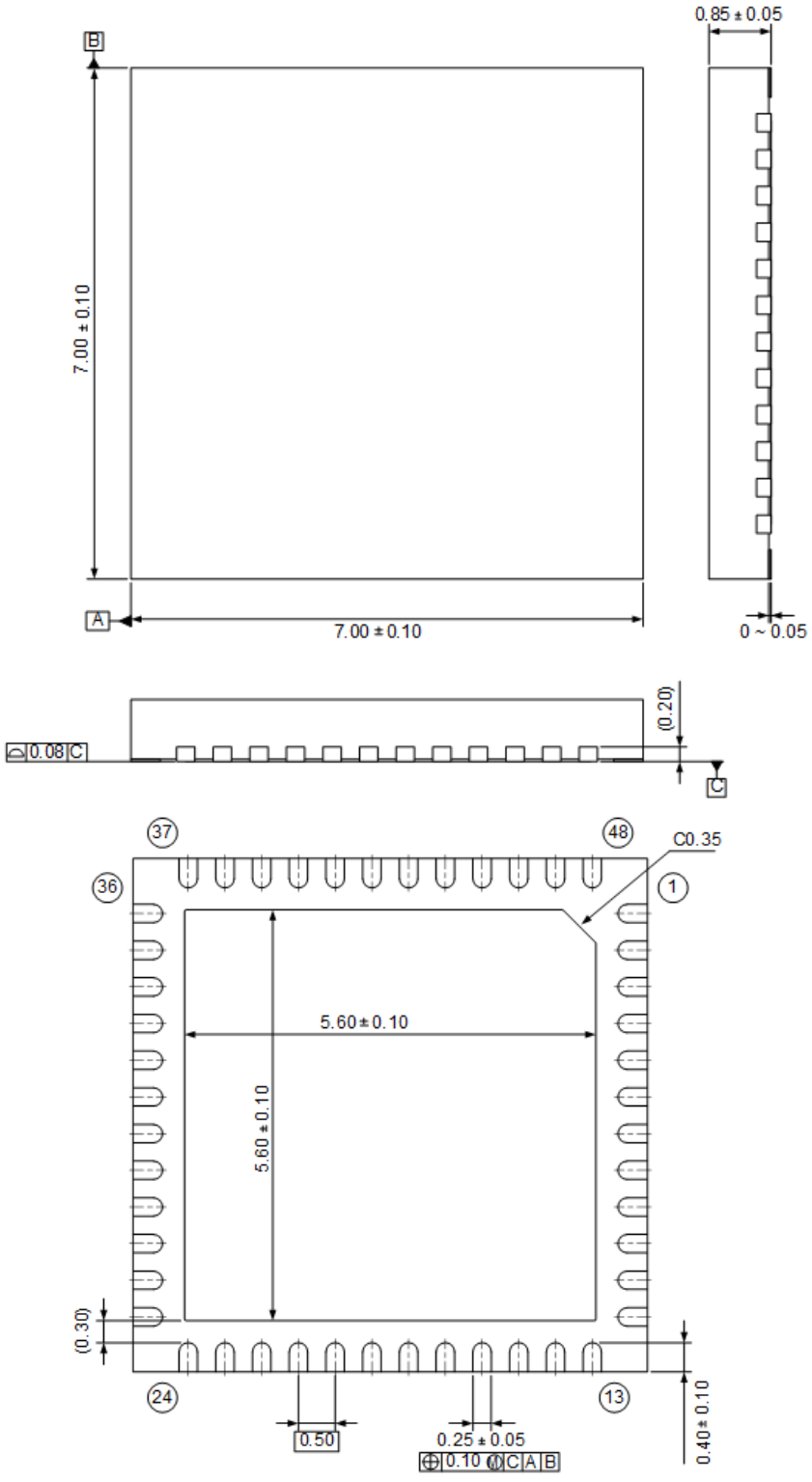
Figure 78. External LPF Circuit Example 3 (fc = 174 kHz (Typ), Q = 0.5 (Typ))

Table 39. Frequency Response of External LPF Circuit Example 3

Gain (1 kHz, Typ)		+1.58 dB
Frequency Response (ref:1 kHz, Typ)	20 kHz	-0.03 dB
	40 kHz	-0.15 dB
	80 kHz	-0.62 dB

11. Package

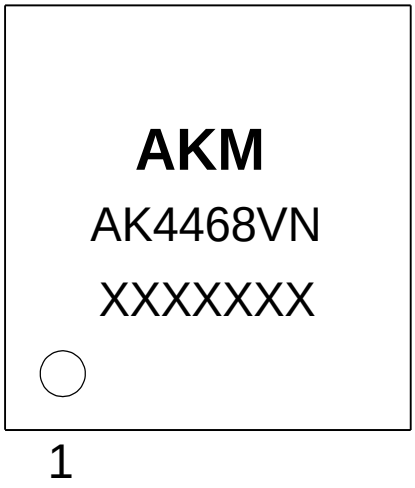
11.1. Outline Dimensions



11.2. Material & Lead Finish

Package molding compound:	Epoxy
Lead frame material:	EFTEC-64T
Pin surface treatment:	Solder (Pb free) plate

11.3. Marking



1) Pin #1 indication
2) AKM Logo
3) Marking Code: AK4468VN
4) Date Code: XXXXXXX (7 digits)

12. Ordering Guide

AK4468VN	-40–105 °C	48-pin QFN
AKD4468	Evaluation Board for AK4468	

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
19/03/08	00	First Edition		
19/06/25	01	Error Correction	10	Absolute Maximum Ratings Low VREF [max] AVDD+0.3 or 6.0 V →[max] AVSS+0.3 V
		Error Correction	15,17,19, 21,23	DEM[2:0] bits → DEM[1:0] bits

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